Logic Requirements Document

Module Name/Internal ID: UARTXRX

Engineer(s):

# Revision

| Rev | Comments | Date | Approval: Team/Date |
| --- | --- | --- | --- |
| 1.0 | Initial Creation |  |  |

# Required Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
| UART | UART SPECIFICATION (https://ieeexplore.ieee.org/document/9227656) | 2.0 |

# Supplemental Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
|  |  |  |

# Acronyms

|  |  |
| --- | --- |
| Abbreviation | Definition |
| UART | Universal Asynchronous Receiver Transmitter |

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# Module Scope

This module transmits and receives buffered serial data according to the UART protocol.

# Functional Requirements

## Interfaces

UARTXRX\_F001: Module shall implement the interfaces described in the following table:

|  |  |  |  |
| --- | --- | --- | --- |
| Port | Direction | Width | Description |
| clk\_50m | input | 1’b1 | Input Clock Signal |
| rst\_i | input | 1’b1 | Input Synchronous Reset Signal |
| Wr\_en | Input | 1’b1 | Write enable |
| Rdy\_clr | input | 1’b1 | Clear ready signal |
| din | input | 8’b1 | 8 bit data into tx side |
| Tx | Output | 1’b1 | Uart transmit signal |
| Tx\_busy | Output | 1’b1 | Transmit busy signal |
| rdy | Output | 1’b1 | Uart rx ready/ valid rx signal |
| dout | Output | 1’b1 | 8bit rx data |

## Parameters

UARTXRX\_F002: module shall implement the parameters described in the following table:

|  |  |  |
| --- | --- | --- |
| Name | Default Value | Description |
| N/A | N/A | N/A |

## 

## Logic requirements

* + - 1. UARTXRX\_F003: Module shall track transactions on it rx signal following the uart protocol.
      2. UARTXRX\_F004: Module shall output received data on dout immediately following a uart rx transaction.
      3. UARTXRX\_F005: Module shall output received data on dout immediately following a uart rx transaction.
      4. UARTXRX\_F006: Module shall deassert rdy one clock cycle after rdy\_clr is asserted.
      5. UARTXRX\_F007: Module shall transmit transactions on it tx signal following the uart protocol.
      6. UARTXRX\_F008: Module shall, when wr\_en is asserted, transmit the data in din on the tx line as a uart tx transaction.
      7. UARTXRX\_F009: Module shall, only while actively transmitting, assert the tx\_busy signal, otherwise deassert tx\_busy.