UART Test Plan Document

Module Name/Internal ID: UARTXRX

Engineer(s):

# Revision

| Rev | Comments | Date | Approval: Team/Date |
| --- | --- | --- | --- |
| 1.0 | Initial Creation |  |  |

# Required Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
| UART | UART SPECIFICATION (https://ieeexplore.ieee.org/document/9227656) | 2.0 |

# Supplemental Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
|  |  |  |

# Acronyms

|  |  |
| --- | --- |
| Abbreviation | Definition |
| UART | Universal Asynchronous Receiver Transmitter |

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# Scope

This document describes in detail the test plan and test results for the UARTTXRX module.

# Functional Verification

UARTXRX\_TP001: Verify that the module implements the interfaces described in the following table:

Verifies: UARTXRX\_F001

Methods: visual inspection, compilation warnings, synthesis.

Results:

|  |  |  |  |
| --- | --- | --- | --- |
| Port | Direction | Width | Description |
| clk\_50m | input | 1’b1 | Input Clock Signal |
| rst\_i | input | 1’b1 | Input Synchronous Reset Signal |
| Wr\_en | Input | 1’b1 | Write enable |
| Rdy\_clr | input | 1’b1 | Clear ready signal |
| din | input | 8’b1 | 8 bit data into tx side |
| Tx | Output | 1’b1 | Uart transmit signal |
| Tx\_busy | Output | 1’b1 | Transmit busy signal |
| rdy | Output | 1’b1 | Uart rx ready/ valid rx signal |
| dout | Output | 1’b1 | 8bit rx data |

UARTXRX\_TP002: Verify that module implements the parameters described in the following table:

Verifies: UARTXRX\_F002

Methods: visual inspection, compilation warnings, synthesis.

Results:

|  |  |  |
| --- | --- | --- |
| Name | Default Value | Description |
| N/A | N/A | N/A |

UARTXRX\_TP003:

Sequence:

1. Set baudrate to a standard rate.
2. Drive RX
3. Verify that dout outputs correct data
4. Verify that rdy is 1 following transfer completion.
5. Assert rdy\_clr .
6. Verify that rdy goes low when rdy\_clr is asserted
7. UARTXRX\_TP003: Module shall track transactions on it rx signal following the uart protocol.

Verifies: UARTXRX\_F003, UARTXRX\_F004, UARTXRX\_F005, UARTTXRX\_F006.

Methods: simulation.

Results:

UARTXRX\_TP004:

Sequence:

* + - 1. Load data into din.
      2. Assert wr\_en
      3. Verify that dout outputs correct data
      4. Verify that rdy is 1 following transfer completion.
      5. Assert rdy\_clr
      6. Verify that rdy goes low when rdy\_clr is asserted

Verifies: UARTXRX\_F003, UARTXRX\_F004, UARTXRX\_F005, UARTTXRX\_F006.

Methods: simulation.

Results: