Logic Requirements Document

Module Name/Internal ID: XXX

Engineer(s):

# Revision

| Rev | Comments | Date | Approval: Team/Date |
| --- | --- | --- | --- |
| 1.0 | Initial Creation |  |  |

# Required Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
|  |  |  |

# Supplemental Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
|  |  |  |

# Acronyms

|  |  |
| --- | --- |
| Abbreviation | Definition |
|  |  |

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# Scope

This document describes in detail, the test plan and test results for the XXX module.

# Functional Verification

XXX\_TP001: Verify that the module implements the interfaces described in the following table:

Verifies: XXX\_F001

Methods: visual inspection, compilation warnings, synthesis.

Results:

|  |  |  |  |
| --- | --- | --- | --- |
| Port | Direction | Width | Description |
| clk\_i | input | 1’b1 | Input Clock Signal |
| rst\_i | input | 1’b1 | Input Synchronous Reset Signal |

XXX\_TP002: Verify that module implements the parameters described in the following table:

Verifies: XXX\_F002

Methods: visual inspection, compilation warnings, synthesis.

Results:

|  |  |  |
| --- | --- | --- |
| Name | Default Value | Description |
| N/A | N/A | N/A |

XXX\_TP003:

Verifies: XXX\_F003.

Methods: simulation.

Results:

XXX\_TP004:

Verifies: XXX\_F004.

Methods: simulation.

Results: