

Work for Digital Electronics Supervision IV

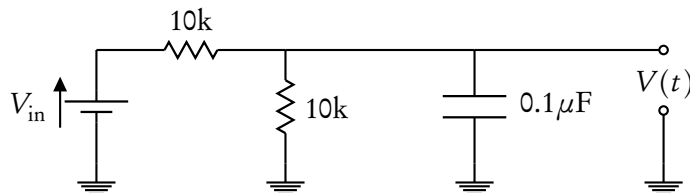
Please attempt all the core items as usual and send your work to me by 1800 on Friday, 4th November. All your answers, working and any additional thoughts should be written up in L^AT_EX and emailed to mti20@cam.ac.uk. Attempting the extension question is optional.

Core questions

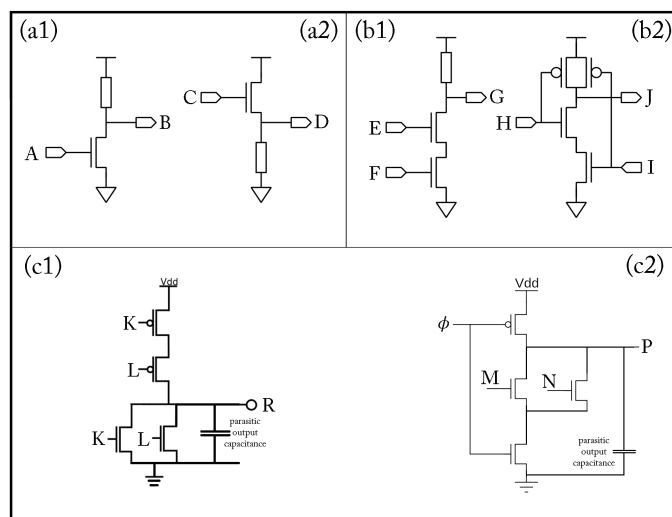
1. Please start by re-attempting either of questions 1 or 2 from last week's supervision work for which you made significant errors. A "significant error" includes forgetting to take account of "don't care" states, or for a state diagram, anything other than a single misplaced arrow. It does not include a heedless error in just one or two of the flip-flop inputs in a state transition table.
2. Derive the familiar equations describing resistors/capacitors in series/parallel:

$$R_{\text{series}} = \sum_i R_i \quad \frac{1}{R_{||}} = \sum_i \frac{1}{R_i} \quad \frac{1}{C_{\text{series}}} = \sum_i \frac{1}{C_i} \quad C_{||} = \sum_i C_i$$

3. Find and sketch $V(t)$ in the following circuit:



4. (a) Give a qualitative explanation of current flow across a *p-n junction* in a semiconductor diode. Why is there a depletion layer in the immediate vicinity of the junction? What is the *barrier potential*? Give its value for both silicon and germanium diodes. Why are silicon diodes now more commonly found than germanium diodes?
 (b) Why is a resistor usually placed in series with a light-emitting diode? Given an LED which is to be driven from a 5V supply, what should be the value of the series resistor? (Give the most suitable standard value that is available.)
5. Examination question: 2012 Paper 2 Question 2 (attached towards the end of this document).
6. Three pairs of circuits (a1, a2), (b1, b2) and (c1, c2) are presented below. What is the operation of each individual circuit, and how does it compare with its pair?

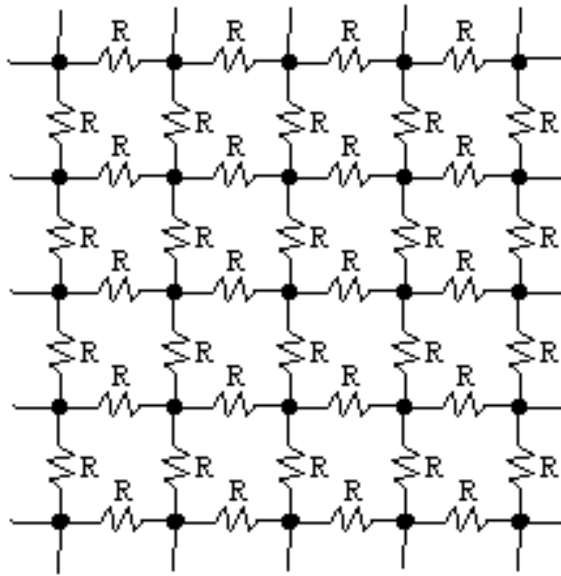


In question 7, consider the relative resistance of the series and parallel transistors in the pull-up and pull-down networks, respectively. The input ϕ may be thought of as clock input. Think about what happens to the output during each half of the clock cycle. During which half of the clock cycle should the output of the gate be read?

7. (a) Sketch a transistor-level circuit for a 2-input AND gate in static CMOS.
- (b) Consider the design of a 16-input AND gate in static CMOS.
 - i. Explain why the 2-input design could not simply be scaled up.
 - ii. Sketch alternative designs using two and four levels of NAND and NOR gates.

Extension questions

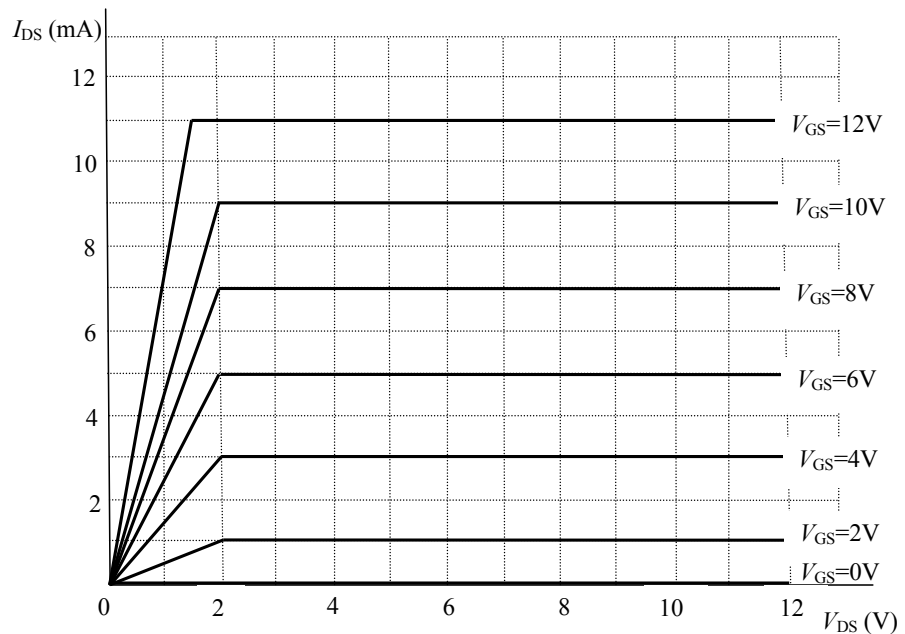
10. Consider an infinite grid of resistors connecting adjacent nodes of a square lattice:



Between every pair of adjacent nodes is a resistance R . The grid extends to infinity in all directions. Determine the effective resistance between any two adjacent nodes in the lattice.

2 Digital Electronics (IJW)

- (a) With the aid of appropriate diagrams, show how the Source–Drain current that flows in a p-channel MOSFET is controlled by the applied Gate–Source voltage. [4 marks]
- (b) (i) Draw the circuit diagram of a NOT gate that comprises an n-channel MOSFET and a resistor R . [2 marks]
- (ii) For the NOT gate in (b)(i), plot the relationship between the input voltage, V_{in} and the output voltage, V_{out} . Assume that the power supply voltage $V_{DD} = 12\text{ V}$, $R = 1\text{ k}\Omega$, and that the MOSFET has the characteristics given in the following figure. [4 marks]



- (c) For the NOT gate in (b), calculate the power dissipated by the entire gate and that by resistor R alone, when $V_{in} = 12\text{ V}$. [4 marks]
- (d) The stray capacitance present at the output of the NOT gate in (b) can be represented by a capacitor, $C = 100\text{ nF}$ connected between the gate output and 0 V . Also assume that the MOSFET has an ON resistance $R_{on} = 100\text{ }\Omega$. The input signal, V_{in} , is a 1 kHz square wave with minimum and maximum amplitudes of 0 V and 12 V respectively.
- (i) Sketch the output signal waveform, V_{out} , of the NOT gate being sure to include indicative rise and fall times and voltage levels. [4 marks]
- (ii) How could the rise-time of V_{out} be reduced and what would be the impact of your proposed solution on the power dissipation of the circuit?