Work for Digital Electronics Supervision II

The questions below are partitioned into two sets: the *core* questions and the *extension* questions. The core questions are based on material that the course should have covered by the end of lecture 6, material with which you should be familiar. Nevertheless, they will likely take a bit of thought. This supervision features the greatest number of core questions: start them early!

The extension questions are based on the same material, but will take longer, and require a lot more thought. Attempting them is optional. The more of the extension questions that you try, the better you will become at Digital Electronics and the easier you will find the work in future weeks. However, do not sacrifice your progress in other subjects or your health for the sake of completing them.

Please attempt all 13 core items and as many of the extension questions as you can, and hand in your work to me by 1500 on Friday, 21st October.

Core questions

1. Show how an 8:1 multiplexor may be constructed using 2:1 multiplexors.
2. For the following Boolean function,

$$F = \overline{A}.\overline{B}.\overline{C} + A.\overline{C}.\overline{D} + \overline{A}.C.D + B.C.\overline{D} + \overline{B}.C.D$$

   show how it may be implemented using:

   (a) one 16:1 multiplexor
   (b) one 8:1 multiplexor and a single NOT gate.

   For (b), try both of the two reasonable methods: first use Boolean algebra, and then use a method based on the function's truth table. Compare/contrast the answers that you obtain. Is the choice of control variable important, in each case?

3. Noting that $a.\overline{b} = a.\overline{(a.b)}$ and $\overline{a}.b = \overline{(a.b)}.b$, use common sub-expression elimination to implement a full-adder using only 9 NAND gates or fewer.
4. A number of possible Boolean functions conform to the map shown below:

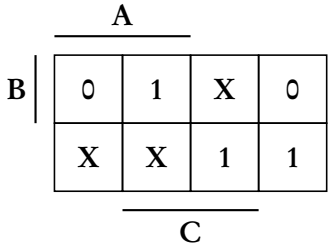


   Exhibit maps and sum-of-product expressions for the following particular functions:

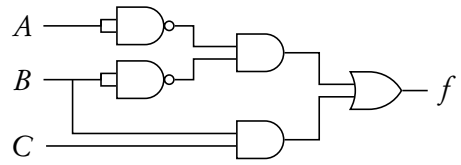
   (a) f_1, being a function of two variables
   (b) f_2, having four minterms
   (c) f_3, having two prime implicants
   (d) f_4, having a prime implicant that cannot appear in the minimum sum-of-products representation.

5. Design a circuit that implements a (4×4)-bit binary multiplier. If you wish, you may abstract to large functional blocks such as "1-bit left shift" and "n-bit adder" (where n is specified), instead of giving the low-level circuit details in full. Prioritise speed over chip area in your design.

6. For an $m \times n$ ROM, what is the meaning of the letters "m" and "n"? What is the total number of bits that can be stored? Illustrate the difference between a ROM and a PAL by using each to implement a 2-bit subtractor. In each case, show the circuit diagram (that is, a diagram showing how the AND and OR planes are connected together).

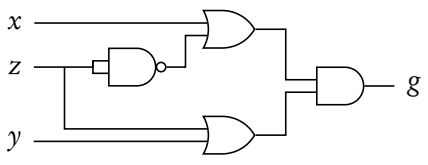
7. For each of the following circuits, write down the propagation delay and contamination delay,[1] and draw a timing diagram showing the output of each gate when the inputs change as indicated. Each gate has a propagation delay of τ. If a static hazard exists, identify its type (static 1 or static 0), and propose a solution. Draw your amended circuit, that does not suffer from the glitch.

(i)



A is a constant 0, C is a constant 1, and B switches from 1 to 0.

(ii)



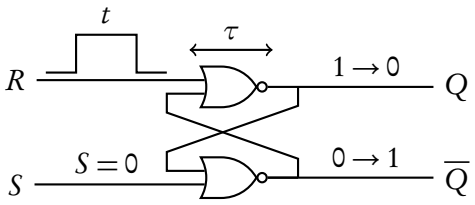
x and y are constant 0s. z is initially 0, switches to 1 for a time $t \gg \tau$, and then returns to 0.

What name is commonly given to the function g?

8. (a) What is the difference between a flip flop and a latch? How might a flip flop be constructed from a latch? Give an example (or two) of the use of each, including timing diagrams to show how and when the signals change.

   (b) How might one use an SR latch to debounce a SPDT switch? Draw timing diagrams to illustrate your answer.

   (c) Suppose a NOR gate has a propagation delay equal to τ. Further suppose that a particular SR latch is in state $Q = 1$, and a clean pulse of length t appears on the R input in order to reset the latch to state $Q = 0$. What is the minimum possible t, expressed in terms of τ, in order for the intended state change to be effected? Support your answer with timing diagrams.



   (d) Explain the operation of an edge-triggered D-type flip flop. Please include a schematic diagram and ensure to include thorough explanations of the setup time, hold time and the delay from a clock edge to the output. What happens if the setup time or hold time are violated? How could such violations occur?

   (e) Suppose I design a new D-type flip flop circuit, which advertises a setup time of zero. Why would it be undesirable to use such a D-type flip flop in a shift register design?

9. Explain the operation of a tristate output. How are such outputs used?

[1] The contamination delay is defined as the minimum time between the input changing and the first subsequent transition in the output.

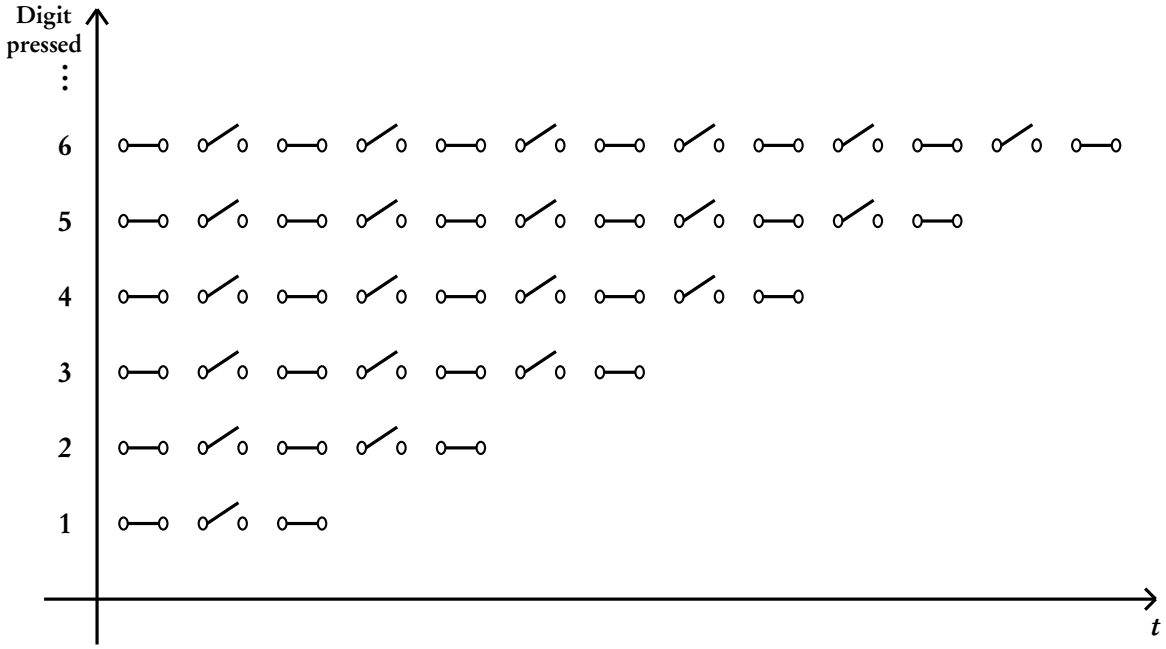
10. Examples sheet question 14 [AM].

    Draw the circuit diagram of the system described before attempting the question. In addition to binary and denary, also write out the output sequence in octal and hexadecimal. Do persevere; the result is important and revealing.

    Don't ignore the second paragraph in the question.

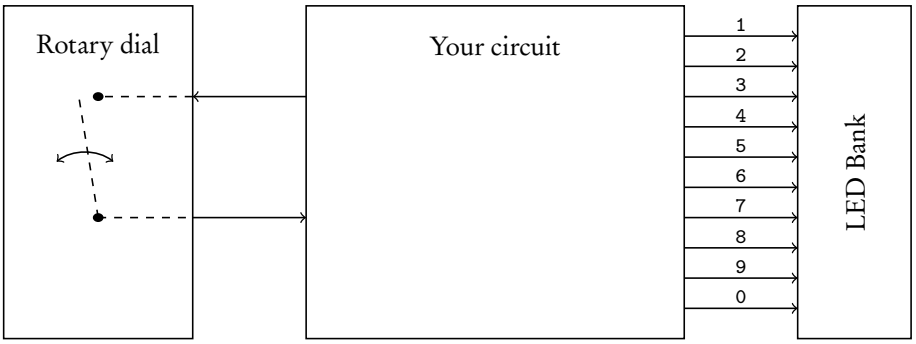
11.

    A problem engineers often face is how to enable humans to enter data into the systems that they design. Until DTMF was widely deployed the 1970s, telephone networks primarily used *pulse dialling* for humans to enter the number of the persons to whom they wished to speak. The person making a telephone call would turn a *rotary dial* to enter each digit of the recipient's telephone number. Supposing the person entered the number n ($n \in \{0, \ldots, 9\}$), the rotary dial would correspondingly interrupt a direct current local loop circuit n times. Essentially, the operation can be thought of as opening and closing a switch to generate a train of pulses as follows:



    For x-axis scale, pulse rates on the edge (consumer) network were—and indeed still are when pulse dial telephones are used—around 10 pulses per second.

    Your task is to design a circuit to convert these switch operations into a parallel output, with one wire for each digit. The rotary dial should plug directly in to your circuit. The signal on the output wire corresponding to a particular digit should be high if, and only if, that digit was dialled on the rotary dial (perhaps after some initial transient period—your circuit need not be free of hazards—although you should identify any hazards that exist). The circuit need only deal with a single digit being pressed: there is no need to consider multiple digits, or an entire telephone number. You might like to include a RESET input that can be pressed after a particular input has been decoded, and the circuit is ready to accept the next input.

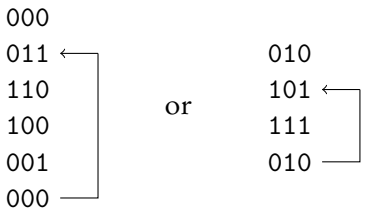


12. Examples sheet questions 15 [AM] and 17.

    In 15, do ensure that your transition logic is minimal.

    For 17, also choose encodings for each state, write them on the state diagram, and explain the reasons behind your choice of encodings.

13. [AM] A sequential circuit has been built using D-type flip flops. It behaves slightly erratically. When switched on, it produces on its three output wires one of the following patterns:

    Deduce the circuit details by drawing the next-state table and working out a minimised sum-of-products expression for the input to each of the three state registers (CBA). Propose a modification that ensures that in due course the circuit will always settle into the cycle shown in the first pattern. Show a Karnaugh map for each flip-flop input before and after your modification, and use them to highlight the change.

Extension questions

14. In general, how many 2^m:1 multiplexors are required to build a 2^n:1 multiplexor ($n \geq m$, $m \geq 2$)?

15. Design an asynchronous circuit with inputs A and B and output Y that has the following truth table:

A	B	Y_t
0	0	0
0	1	Y_{t-1}
1	0	Y_{t-1}
1	1	1

    where Y_{t-1} denotes a *don't change* condition.

    That is, use SR latches and other components to design a circuit that:

    (a) reflects its inputs when the states of all the inputs match, and

    (b) whose output should remain in this state until the inputs all make the transition to the other state.

    Redesign your circuit using only NAND gates. How small can you make it?

16. Examination question: 1999 Paper 10 Question 1 (attached towards the end of this document).

17. Examination question: 2002 Paper 2 Question 3 (attached at the end of this document).

18. A scheme is described in lectures for producing *generate*, *propagate* and *kill* signals that can be used to improve the time-domain performance of conventional ripple-carry adders. Research the alternative ways[2] in which these signals can be used, and describe:

    - carry look-ahead
    - carry skip
    - carry select

    Summarise their performance by filling in the following table of their space (chip area) and time complexities using big-O notation, and explain your reasoning:

	Time	**Space**
Ripple		
Carry look-ahead		
Carry skip		
Carry select		

[2] You may find useful the notes for the Part II VLSI Design course (last run in 2006–07), available from `http://www.cl.cam.ac.uk/teaching/0607/VLSI/VLSI.pdf`.

1999 Paper 10 Question 1

Digital Electronics

An $m : 1$ multiplexer has m data inputs, $\log_2 m$ control signals and produces a data output which is equal to the input selected by the control signals. Each different combination of control signals selects a different input. Present an implementation, either as a circuit diagram or as equations, of an $8 : 1$ multiplexer. [5 marks]

Show how $8 : 1$ multiplexers can be cascaded to build a $64 : 1$ multiplexer. [5 marks]

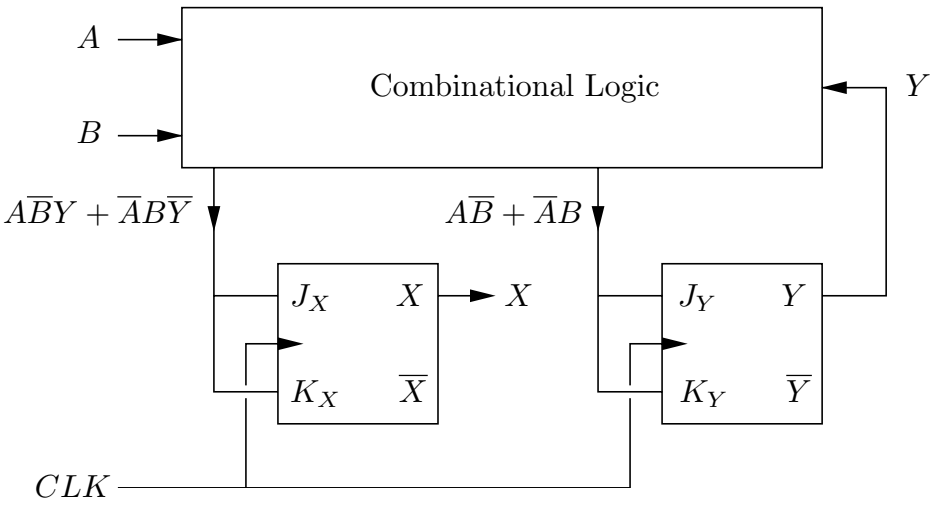
A 2^m-bit decoder has m inputs and 2^m outputs, with only one output taking the value 1 at a time. The particular output which has the value 1 at any given time is determined by the inputs. Each different combination of inputs selects a different output. Present an implementation of an 8-bit decoder. [5 marks]

How might a decoder be used as a functional component of a read-only memory? [5 marks]

2002 Paper 2 Question 3

Digital Electronics

Consider the following circuit with clock CLK, inputs A and B and outputs X and Y.



(a) How many states does this system have? [2 marks]

(b) How many rows will there be in a state transition table? [2 marks]

(c) Provide the state transition table. [8 marks]

(d) Draw a state diagram of the system. [6 marks]

(e) Describe what the circuit does in words. [2 marks]