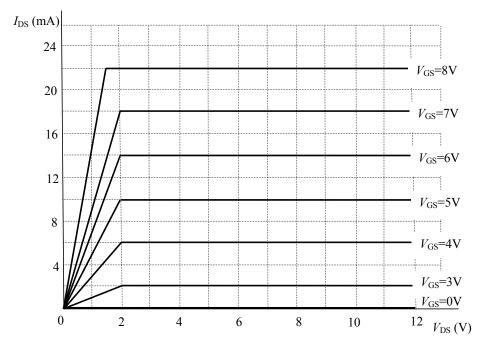
COMPUTER SCIENCE TRIPOS Part IA – 2015 – Paper 2

2 Digital Electronics (IJW)

- (a) Draw a diagram showing the structure of an n-channel MOSFET and describe how the Drain to Source current can be controlled. [4 marks]
- (b) Draw the circuit diagram of a NOT gate that comprises an n-channel MOSFET and a resistor R. [2 marks]
- (c) For the NOT gate in part (b), plot the relationship between the input voltage, $V_{\rm in}$, and the output voltage, $V_{\rm out}$. The power supply voltage, $V_{\rm DD} = 10$ V, $R = 500~\Omega$, and the MOSFET has the characteristics given in the following figure. [6 marks]



- (d) For the NOT gate in part (c), calculate the power dissipated by resistor R when $V_{\text{in}} = 8 \text{ V}$. [3 marks]
- (e) (i) Describe how the power dissipated by resistor R can be reduced. State any potential problems with your proposed solution. [3 marks]
 - (ii) Present a modified circuit for a NOT gate that eliminates the problem of static power dissipation in resistor R. [2 marks]