CST Part IA: Digital Design, SV 4
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1 Exercise 1

SV2.2

(a)

$[Q_1, Q_0]$	$[Q_1', Q_0']$	[D,N]
00	00	00
00	01	x1
00	10	1x
01	01	00
01	10	x1
01	11	1x
10	10	00
10	11	x1
10	11	1x
11	11	xx

(b)

$[Q_1, Q_0]$	$[Q_1', Q_0']$	[D,N]	$[J_1, K_1, J_0, K_0]$
00	00	00	0x0x
00	01	x1	0x1x
00	10	1x	1x0x
01	01	00	0xx0
01	10	x1	1xx1
01	11	1x	1xx0
10	10	00	x00x
10	11	x1	x01x
10	11	1x	x01x
11	11	xx	x0x0

K-Map for J_1

Q_1Q_0 DN	00	01	11	10
00	0	0	x	1
01	0	1	x	1
11	x	x	x	x
10	x	x	x	x

K-Map for K_1

Q_1Q_0 DN	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	0	0	x	0
10	0	0	x	0

K-Map for J_0

Q_1Q_0 DN	00	01	11	10
00	0	1	x	0
01	x	x	x	x
11	x	x	x	x
10	0	1	x	1

K-Map for K_0

Q_1Q_0 DN	00	01	11	10
00	x	x	x	x
01	0	1	x	0
11	0	0	x	0
10	x	x	x	x

$J_1 = D + Q_0N$
$K_1 = 0$
$J_0 = N + Q_1D$
$K_0 = \bar{Q_1}N$

2 Exercise 2

1. Assume the current passes series of resistors is I, then the whole voltage of the circuit will be:
   $V = \sum_i IR_i$
   $R = V/I = \sum_i R_i$

2. Assume the voltage through parallel of resistors is V, then the whole current of the circuit will be:
   $I = \sum_i V/R_i$
   $1/R = I/V = \sum_i 1/R_i$

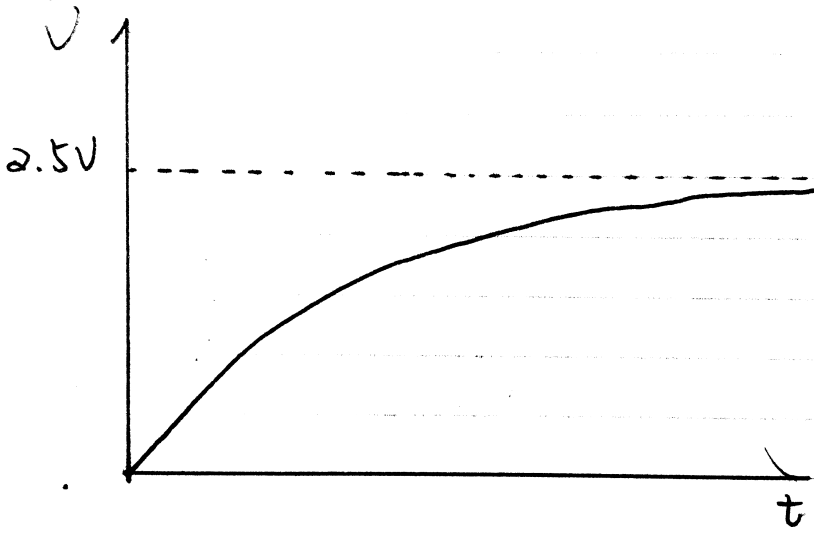
3. Assume the charge stored in series of each capacitors is Q, then the whole voltage of the circuit will be:
   $V = \sum_i Q/C_i$
   $1/C = V/Q = \sum_i 1/C_i$

4. Assume the voltage through in parallel of each capacitors is V, then the whole charge of the circuit will be:
   $Q = \sum_i VC_i$
   $C = Q/V = \sum_i C_i$

3 Exercise 3

For clarity: $R = 10k\Omega$ and $C = 0.1\mu F$
Define the branch with resistor as 1 and the branch with capacitor as 2.
Apply Kirchhoff's current law.
$I = I_1 + I_2$ Apply Kirchhoff's voltage law and characteristic of resistor and capacitor.
$\frac{dCV}{dt} + \frac{V}{R} = \frac{V_{in}-V}{R}$
Solve the equation.
$V = \frac{1}{2}V_{in} + Ae^{-\frac{2}{CR}t}$
As $t = 0$ $V = 0$ so $A = -\frac{1}{2}V_{in}$
$V = \frac{1}{2}V_{in}(1 - e^{-\frac{2}{CR}t})$

If $V_in = 5V$



4 Exercise 4

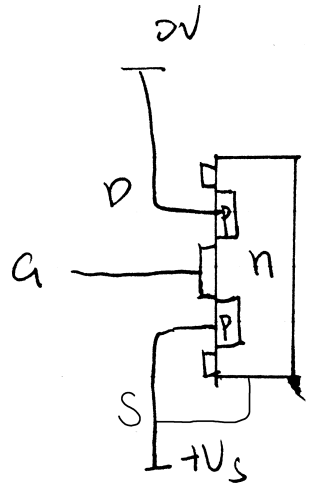
(a) The current will be easier to passes from p to n but harder vice versa because of the existence of the depletion region.
P-type Si is doped with B which has only 3 valence electrons, it accepts an extra electron from one of the adjacent Si atoms to complete its covalent bonds.This leaves a hole.
N-type Si is doped with Ar which has 5 valence electrons and when covalent bonds form, the additional elections will need only a little energy to move free in the lattice.
The depletion region in the vicinity of the junction is form by diffusion of electrons or holes. On N side the diffusion will leave +ve charged donor atoms and on P side which will leave -ve charged acceptor atoms. This leaves a space charge region called depletion region.
The space charge gives rise to electric field that opposes the diffusion. The potential difference associates with the field is barrier potential.
$Pd_{Si} = 0.7V$ and $Pd_{Ge} = 0.3V$
A small barrier potential means a significant current will be allowed to pass the diode easily and this will leave us a smaller error or uncertainty space for the input voltage which makes the circuit has a larger probability of having wrong behaviour.

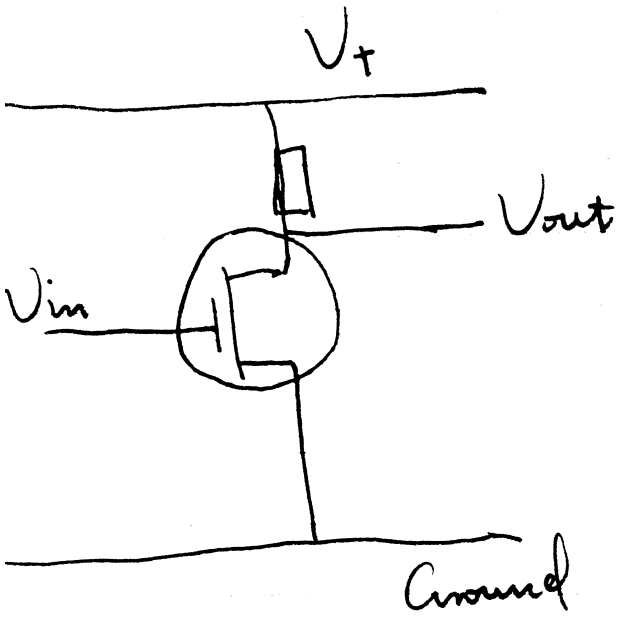
(b) Because the Current-Voltage diagram of the diode will be very steep when V is large so a resistor can protect the circuit under the high voltage through the diode by avoiding large current passing the diode.

I assume the standard current of the diode is $20mA$.
Then $R = \frac{5V-0.7V}{0.02A} = 215\Omega$

5 Exercise 5

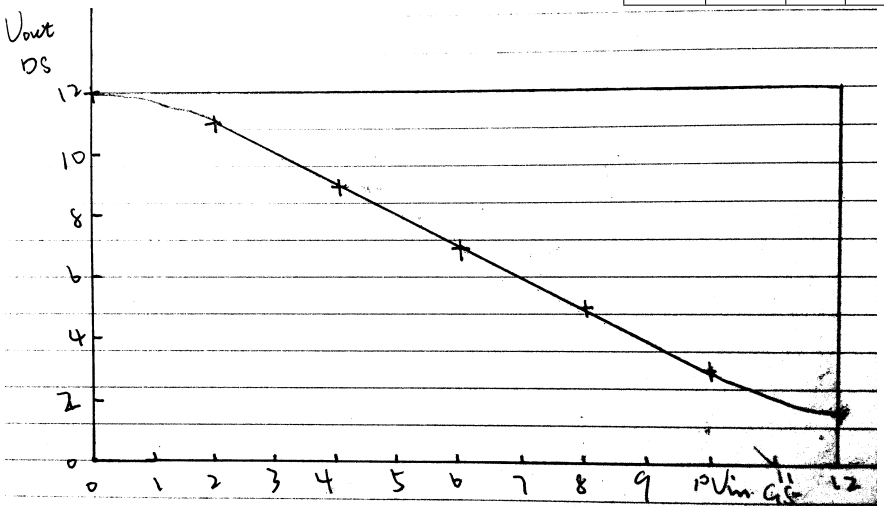
(a) When Gate is grounded then the p-MOSFET will be ON.
When Gate is connected to V_s either then the p-MOSFET will be OFF.





(b)

V_{GS}	12	10	8	6	4	2	0
V_{DS}	1.44	3	5	7	9	11	12

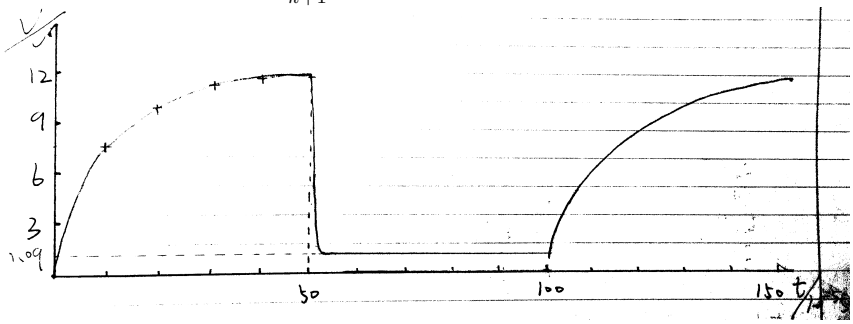


(c) $V_{in} = V_{GS} = 12V$ gives $V_{DS} = 1.44V$

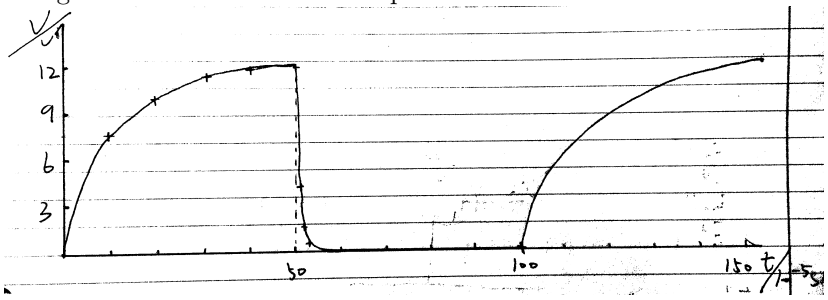
$V_R = 12 - 1.44 = 10.56V$
Power dissipated by resistor:
$P_{Res} = V_R^2/R = 10.56^2/1000 = 112mW$
Total resistance of the circuit:
$R = 1000/10.56 \times 12 = 1136\Omega$
Total power by the whole circuit:
$P = V_R^2/R = 12^2/1136 = 127mW$

(d) The time for charge or discharge will be $5 \times 10^{-4}s$.
When the MOSFET is OFF (charging): $RC = 1 \times 10^{-4}s$
When the MOSFET is ON (discharging): $RC = 1 \times 10^{-5}s$
Because $t_{charge} < t_{discharge} < t$

I guess if I consider the whole circuit when $R_{OFF} = 100\Omega$ then. The LOW voltage should drop to $12/11V$ as $V = \frac{V_{in}}{k+1}$) k is the ratio of the series and parallel resistor.



If I ignore the effect of the other part of the circuit then:



To reduce the rise time for the charging part we will need a smaller time constant so a smaller series resistor. But this will cause 2 drawbacks.

(a) Because the resistance is reduced, when the MOSFET is ON. A smaller resistance will lead to a larger power dissipate. (R is divider in the equation)

(b) From the Exercise 3, a smaller series resistor actually raise the LOW output voltage as $V = \frac{V_{in}}{k+1}$ reducing the k which reduce the noise margin and make the circuit easier to make mistake.

6 Exercise 6

(a) 1. Is a NOT gate. The HIGH output will be V_{in} if I assume the OFF state of the MOSFET has $\infty\Omega$. But I guess the LOW output will really based on the ratio of the

resistance of the resistor and the ON state MOSFET $V = \frac{V_{in}}{k+1}$) (k is the ratio.) So the resistor should be significantly larger than the ON state MOSFET.

2. Returns what it get. The LOW output will be $0V$ if I assume the OFF state of the MOSFET has $\infty\Omega$. But I guess the HIGH output will really based on the ratio of the resistance of the resistor and the ON state MOSFET $V = \frac{kV_{in}}{k+1}$) (k is the ratio.) So the resistor should be significantly larger than the ON state MOSFET. I guess this is used for re-amplify the signal.

(b) 1. Is a NAND gate. The HIGH output will be V_{in} if I assume the OFF state of the MOSFET has $\infty\Omega$. But I guess the LOW output will really based on the ratio of the resistance of the resistor and the ON state MOSFET $V = \frac{2V_{in}}{k+1}$) (k is the ratio.) So the resistor should be significantly larger than the ON state MOSFET.

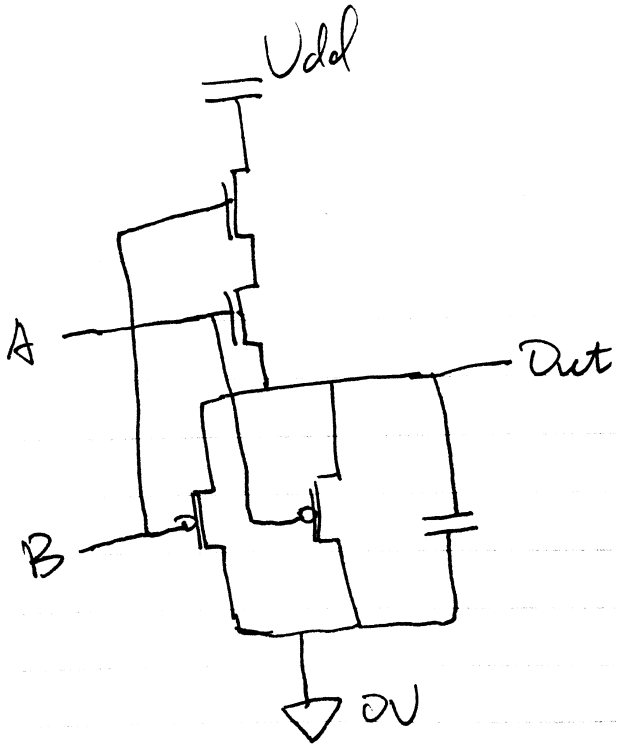
2. Is a NAND gate. If I assume the OFF state of the MOSFET has $\infty\Omega$. The voltage of HIGH output will be the V_{in}. But the Low output will be $0V$ because both of the p-MOSFET is OFF. This is a better version of (b.1).

(c) 1. Is a NOR gate. If I assume the OFF state of the MOSFET has $\infty\Omega$. Then the output should be either $0V$ or V_{dd}.

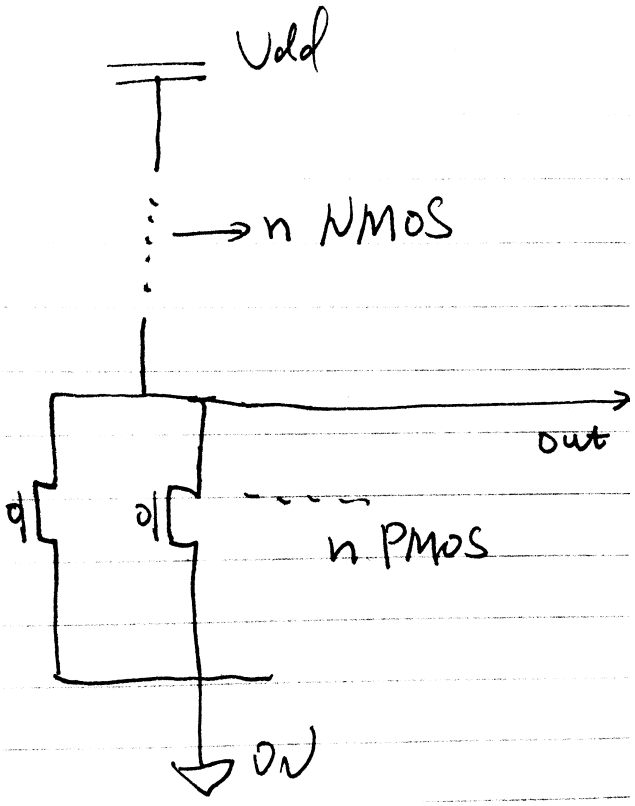
2. Is a 3-input NOR gate. If the ϕ is connected to a clock signal then when $\phi = 0$ the output will be 0. When $\phi = 1$ the output should behaves like a 2-input NOR gate based on M,N. So should be read on high half of the clock signal.

7 Exercise 7

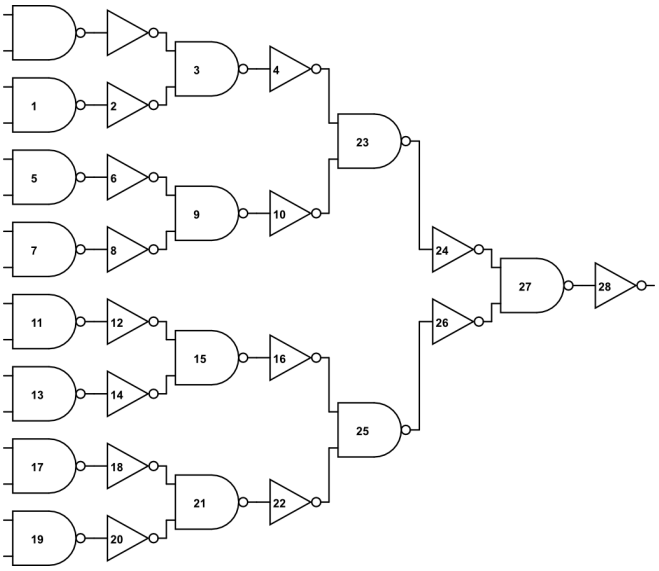
1.



2. I do not get the questions..
Does the scale up means this?


Vdd
n NMOS
out
n PMOS
0N

* n=16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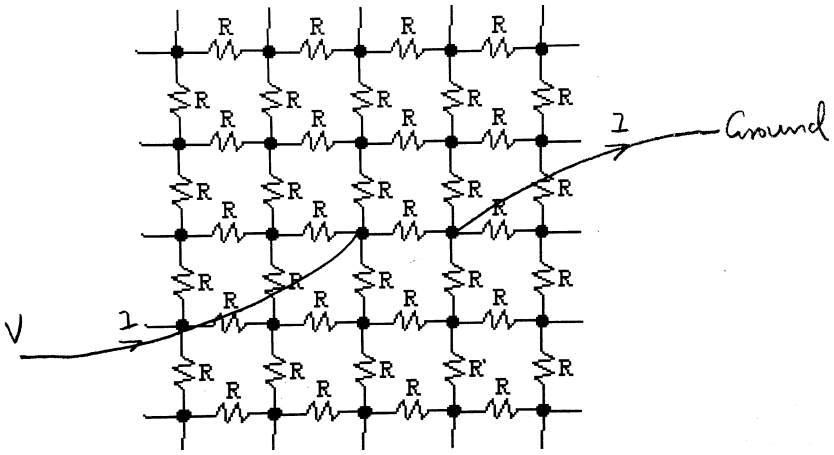
8 Exercise 8



Consider as the diagram then the resistance between two adjacent node will be $\frac{V}{I}$.
Because of the symmetrical structure so there are $\frac{1}{4}I$ current flow out from the V input to ground. Also there will be $\frac{1}{4}I$ current flow back from V back to ground. As I assume the current flow to the infinity and back.
So the current between V and ground is $\frac{1}{2}I$.
So $R = 2\frac{V}{I}$.
Then we know $\frac{V}{I} = \frac{R}{2}$