COMPUTER SCIENCE TRIPOS Part IA – 2016 – Paper 2

2 Digital Electronics (IJW)

(*a*) Briefly describe what is meant by synchronous logic. Show how a Master-Slave D-type Flip-Flop may be constructed from two transparent D-latches and describe its operation with the help of a timing diagram. [7 marks]

(*b*) With the use of appropriate diagrams, briefly explain the operation of Moore and Mealy finite state machines, paying particular regard to their differences. [4 marks]

(*c*) A two-bit synchronous binary Up/Down (U/D) counter is capable of either up-counting (e.g., $0, 1, 2, 3, 0, \ldots$) or down-counting (e.g., $3, 2, 1, 0, 3, \ldots$) and randomly changes between these two modes of operation. It has outputs X and Y, where X is the Most Significant Bit (MSB).

The U/D counter is connected to a count Direction Detection System (DDS) that has two outputs, namely C_U and C_D, where C_U is required to give a binary 1 pulse when the U/D counter up-counts and C_D is required to give a binary 1 pulse when the U/D counter down-counts, otherwise the two outputs are both to remain at binary 0.

Assume that the count DDS has two state registers, each implemented as a D-type Flip-Flop (FF). The next state outputs of each FF, namely Q_X and Q_Y are given by the current inputs to the DDS, i.e., the U/D counter output bits X and Y respectively. Also assume that the FFs in the count DDS are clocked at a much higher rate than the U/D counter.

(*i*) Draw a state diagram for the count DDS, where the arcs connecting the states show the bits X and Y input to the count DDS, and also the output signals C_U and C_D. [4 marks]

(*ii*) Determine the combinational logic required in the count DDS to generate C_U and C_D from the inputs X and Y, and from the two FF outputs, namely Q_X and Q_Y. [5 marks]