CST Part IA: Digital Design, SV 2
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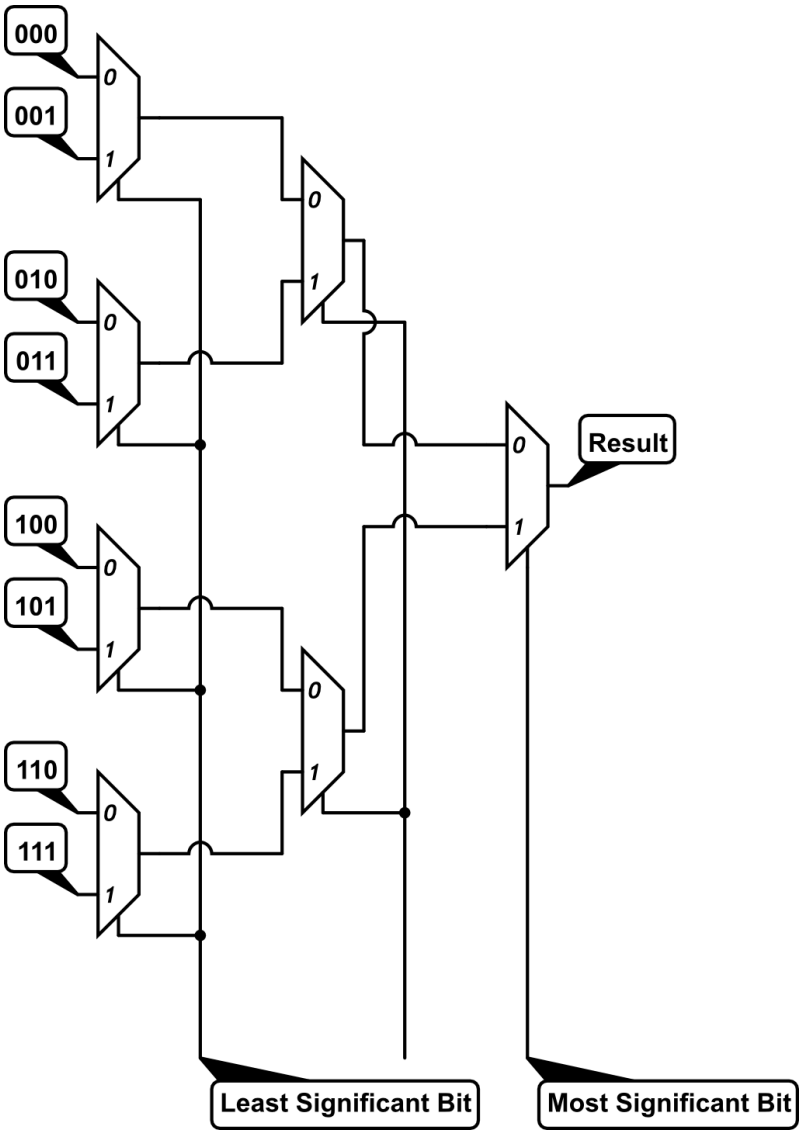
2016-10-17

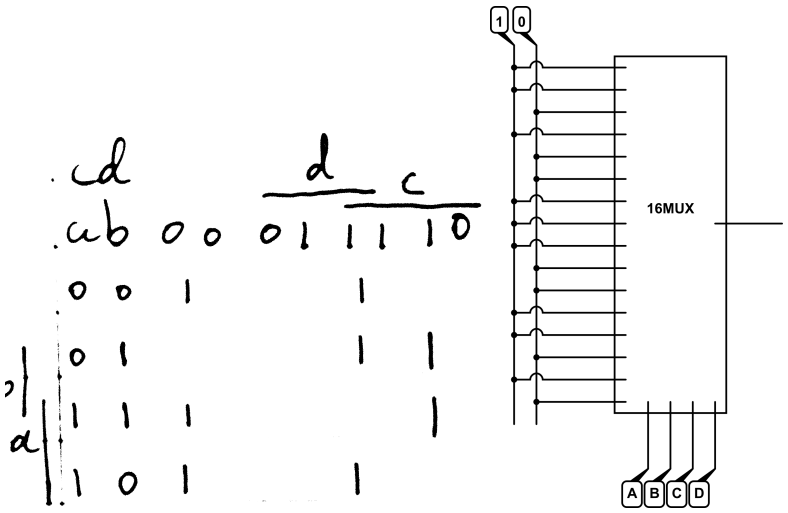
Exercise 1



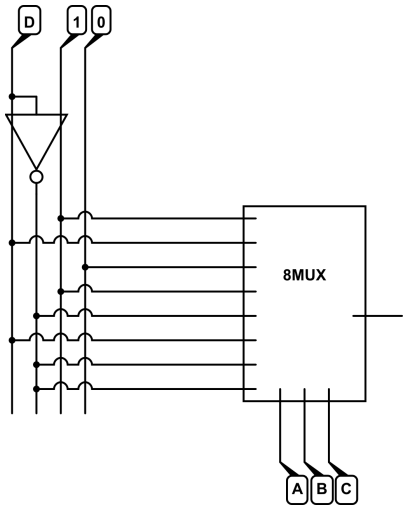
The idea is once a control input of a "higher level" multiplexor is chosen either 0 or 1 then it is actually looking up the corresponding input from a "lower level" multiplexor output. And this idea goes through the whole circuit until get the lowest level multiplexor and take the 1 or 0 from the input. In this way,the control input of the highest level multiplexor is controlling the most significant bit of the truth table and the lowest one is controlling the least significant bit.
And the picture shows how it is built.

Exercise 2

(a)



(b)



A	B	C	D	result	
0	0	0	0	1	1
0	0	0	1	1	
0	0	1	0	0	D
0	0	1	1	1	
0	1	0	0	0	0
0	1	0	1	0	
0	1	1	0	1	1
0	1	1	1	1	
1	0	0	0	1	$\bar{D}$
1	0	0	1	0	
1	0	1	0	0	D
1	0	1	1	1	
1	1	0	0	1	$\bar{D}$
1	1	0	1	0	
1	1	1	0	1	$\bar{D}$
1	1	1	1	0	

* n means not related with D.
Because for specific A,B,C the result is either based on D or $\bar{D}$ or unrelated to D and constrained to 1 or 0. So the D or $\bar{D}$ can be an input instead of control input.

Exercise 3

Exercise 4

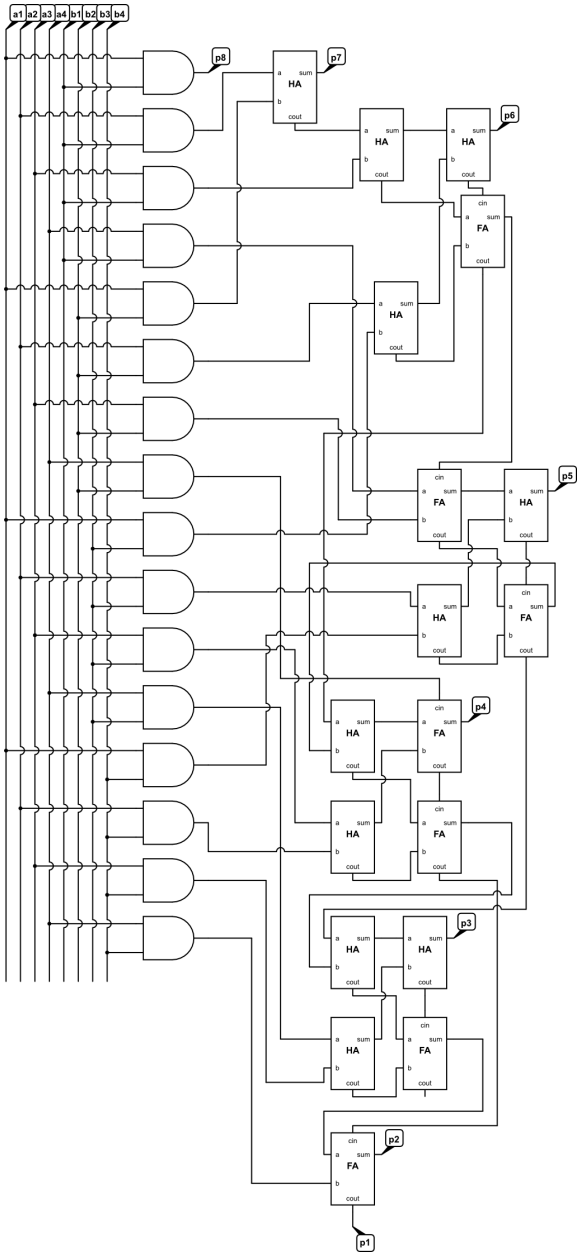
(a) $\bar{B} + C$

(b)

(c) $\bar{B} + C$

(d)

Exercise 5

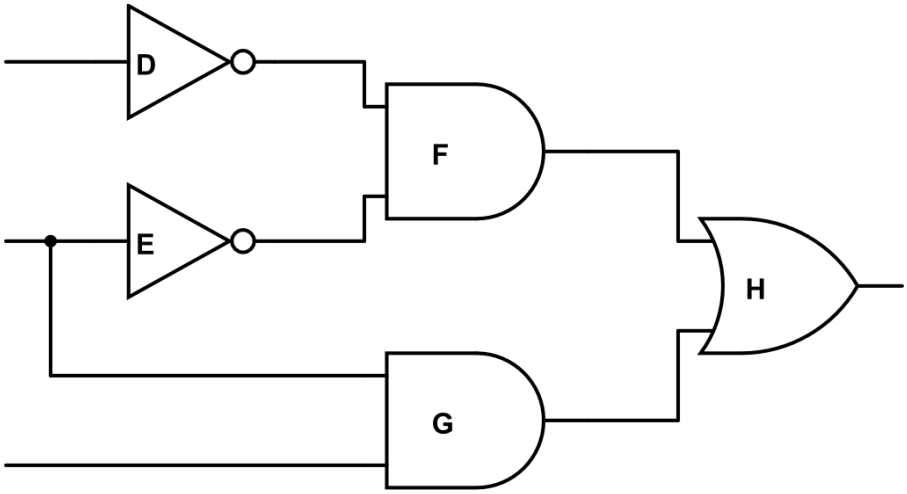


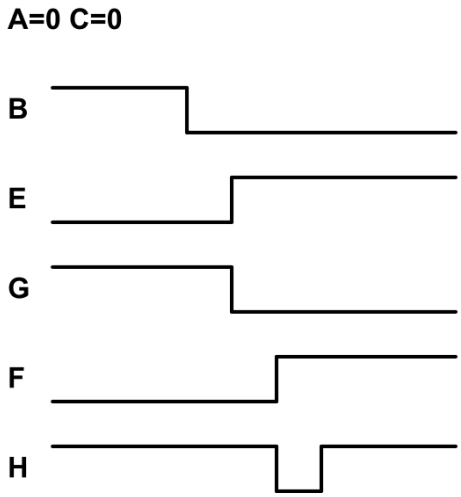
*x_n means the nth number from most significant to least significant of binary number x.
This idea comes from the basic product operation by human. And notice the one of the full adder close to bottom is impossible to have a c_{out} as one.

Exercise 6

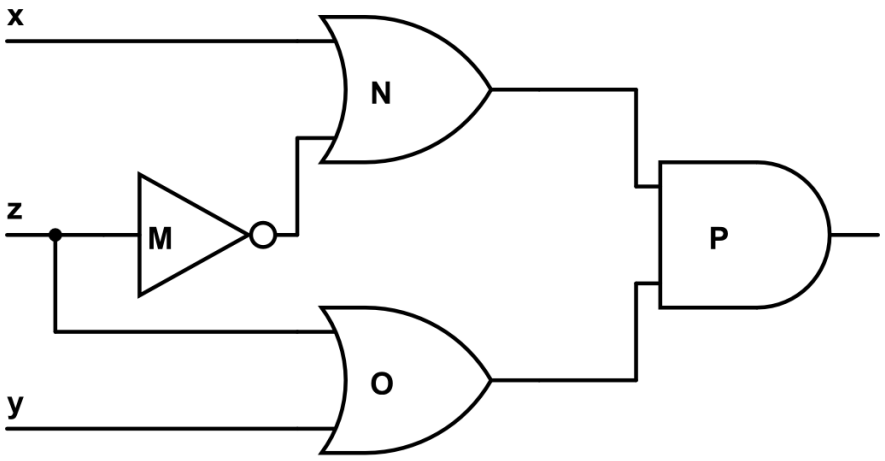
m means the number of bits in each address.
n means the number of input for address looking-up.(So there are 2^n different address)
Number of bit stored: $m \times 2^n$
The ROM is basically a n-input looking-up table for m-bit words. However the implement for PAL is by a SOP formula, the complement or uncomplement of each variable will join in AND gates and then the output of these AND gates will be input to OR gates again to give an output.

Exercise 7

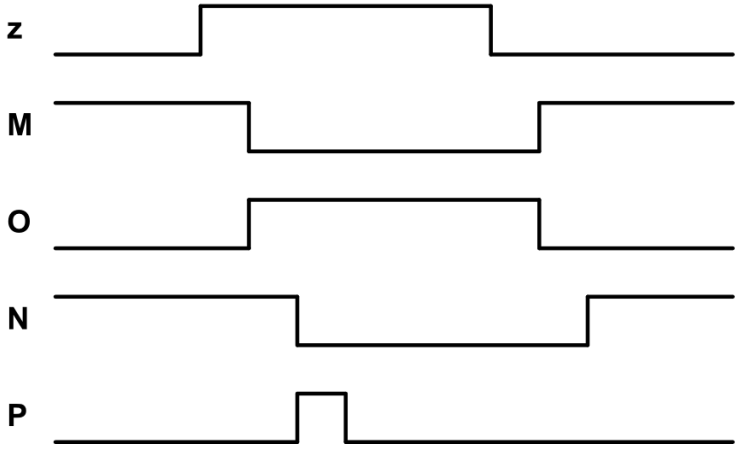




(i)
Propagation delay: $3T$
Contamination delay: $2T$



x=0 y=0



(ii)
Propagation delay: $3T$
Contamination delay: $2T$
g is a 2-multiplexor

Exercise 8

Exercise 9

Exercise 10

Exercise 11

Exercise 12

Exercise 13

Exercise 14

Exercise 15

Exercise 16

Exercise 17

Exercise 18