CST Part IA: Digital Design, SV 2
Joe Yan
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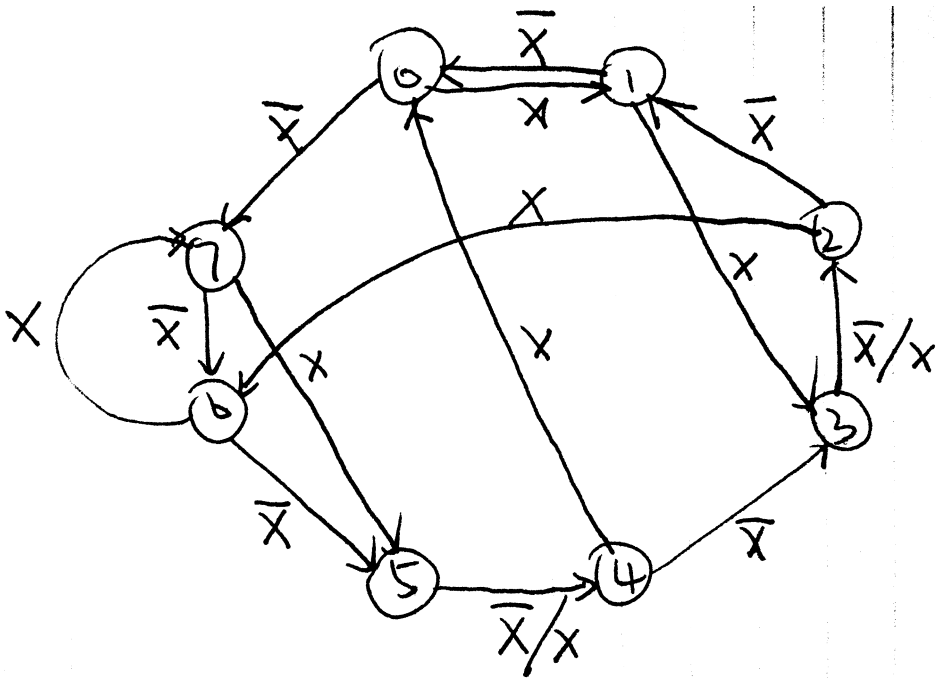
1 Exercise 1



A	B	C	X	A'	B'	C'
1	1	1	1	1	1	0
1	1	0	1	1	0	1
1	0	1	1	1	0	0
1	0	0	1	0	1	1
0	1	1	1	0	1	0
0	1	0	1	0	0	1
0	0	1	1	0	0	0
0	0	0	1	1	1	1
1	1	1	0	1	0	1
1	1	0	0	1	1	1
1	0	1	0	1	0	0
1	0	0	0	0	0	0
0	1	1	0	0	1	0
0	1	0	0	1	1	0
0	0	1	0	0	1	1
0	0	0	0	0	0	1

A' K-Map

XA BC	00	01	11	10
00	0	0	0	1
01	0	1	1	1
11	0	1	1	1
10	1	0	0	0

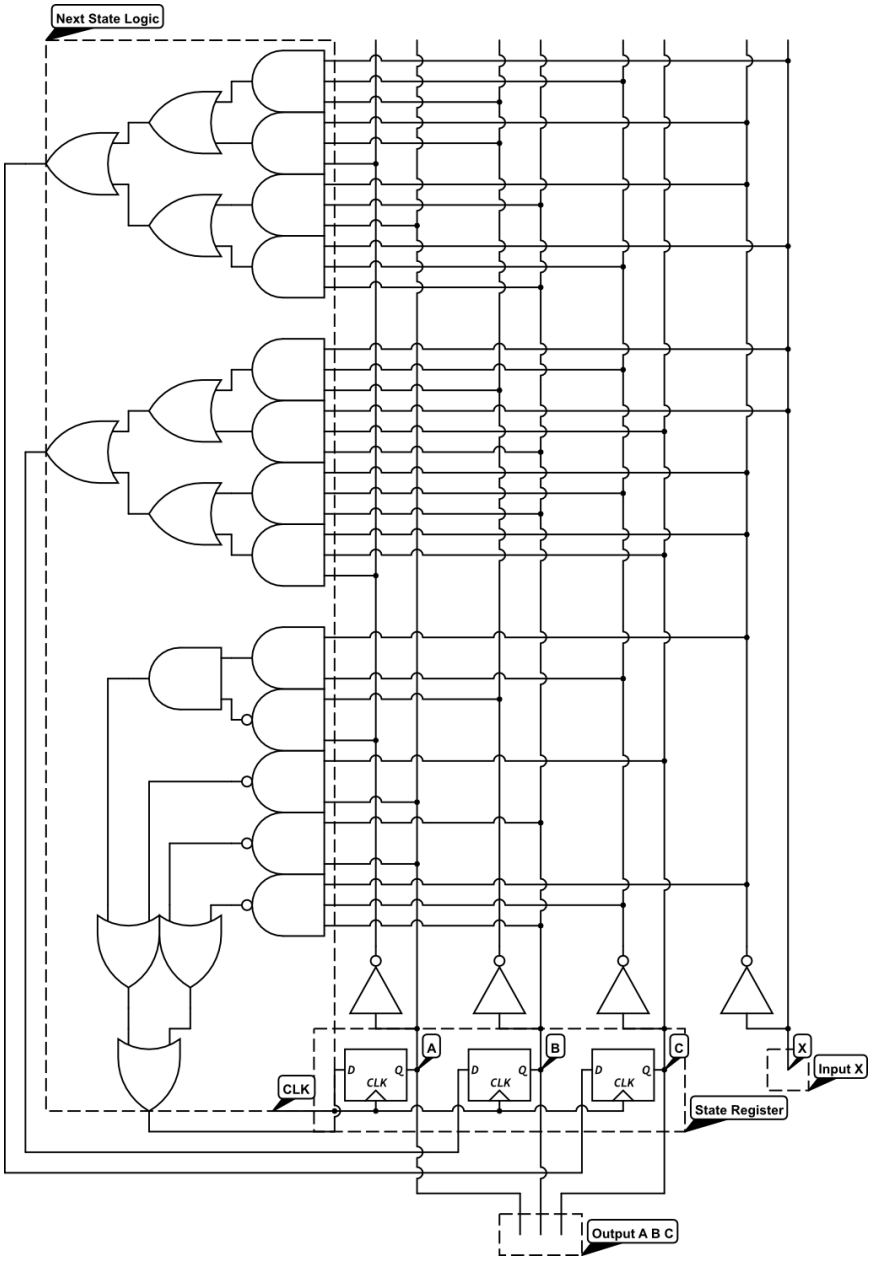
B' K-Map

XA BC	00	01	11	10
00	0	1	1	1
01	0	0	0	1
11	1	0	1	0
10	1	0	1	0

C' K-Map

XA BC	00	01	11	10
00	1	1	0	0
01	0	0	1	1
11	1	0	0	1
10	1	0	0	1

$A' = \bar{X}\bar{A}\bar{B}\bar{C} + AC + AB + \bar{X}B\bar{C}$
$B' = X\bar{B}\bar{C} + XBC + \bar{X}B\bar{C} + \bar{X}\bar{A}C$
$C' = X\bar{B}\bar{C} + \bar{X}\bar{A}\bar{B} + \bar{X}AB + XB\bar{C}$



2 Exercise 2

(a)

$[Q_1, Q_0]$	$[Q_1', Q_0']$	[D,N]
00	00	00
00	01	01
00	10	10
01	01	00
01	10	01
01	11	10
10	10	00
10	11	01
10	11	10
11	11	00
11	11	01
11	11	10

(b)

$[Q_1, Q_0]$	$[Q_1', Q_0']$	[D,N]	$[J_1, K_1, J_0, K_0]$
00	00	00	0000
00	01	01	0011
00	10	10	1100
01	01	00	0000
01	10	01	1111
01	11	10	1100
10	10	00	0000
10	11	01	0011
10	11	10	0011
11	11	00	0000
11	11	01	0000
11	11	10	0000

K-Map for J_1K_1

Q_1Q_0 DN	00	01	11	10
00	0	0	x	1
01	0	1	x	1
11	0	0	x	0
10	0	0	x	0

K-Map for J_0K_0

Q_1Q_0 DN	00	01	11	10
00	0	1	x	0
01	0	1	x	0
11	0	1	x	1
10	0	0	x	0

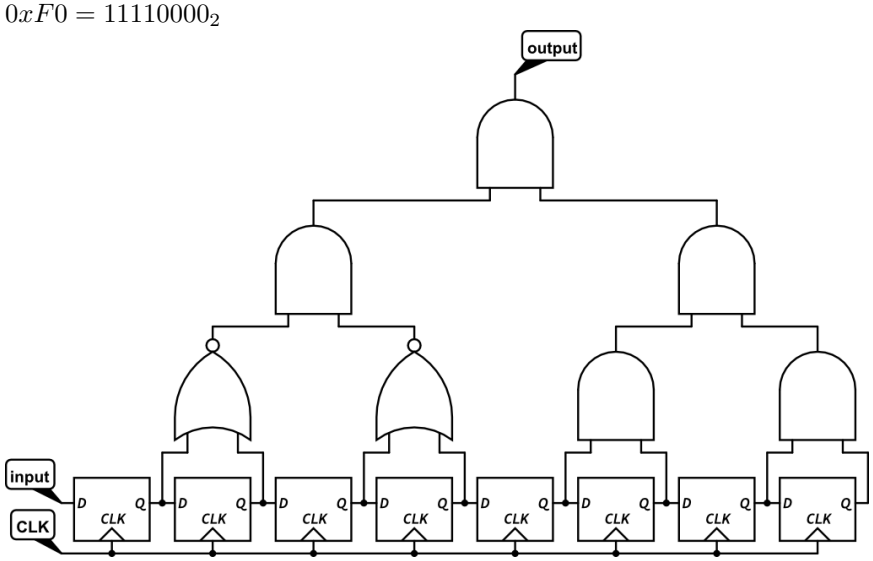
$J_1 = K_1 = \bar{Q_1}D + \bar{Q_1}Q_0N$
$J_0 = K_0 = \bar{Q_1}N + \bar{Q_0}N + Q_1Q_0D$

3 Exercise 3

(a)

$x_0x_1x_2x_3$
0000
1000
0100
1010
0101
1010
1101
1110
0111
0011
0001
0000

(b) $0xF0 = 11110000_2$



(c) The assumption made:

1. The form of input data is in pulse and the length of pulses is equal to a CLK period.
2. The 11-bit counter is synchronous otherwise the edge of the time graph will shift a bit for each CLK period and may cause error Y output.

The circuit should have 3 states is stored in 2 D-FF as (M,N):
A(0,1): Assuming lock.
B(0,0): Maintaining lock.
C(1,0): One missed framing pattern during B or One matched pattern during A.
And two inputs:
X: 11110000 pattern matching circuit output.
Y: 11-bit Counter output when 00000000000 is reached.

Origin	Next	XY
01	01	0x
01	10	1x
00	00	x0,11
00	10	01
10	10	x0
10	00	11
10	01	01

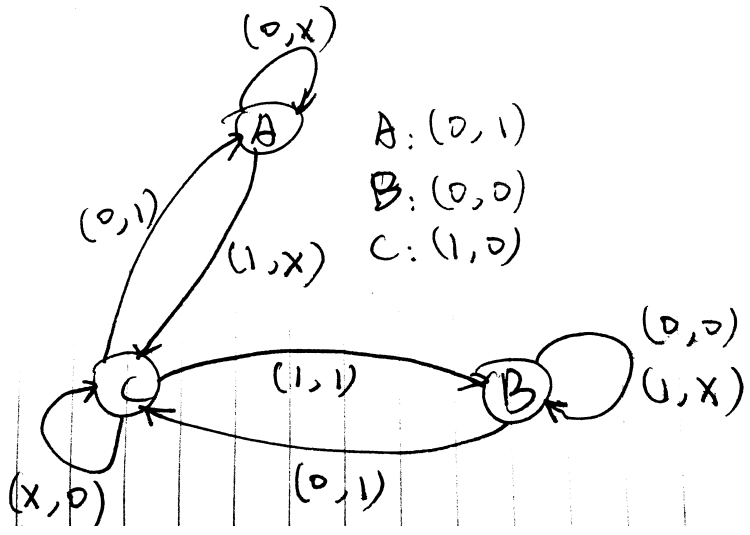
K-Map for M'

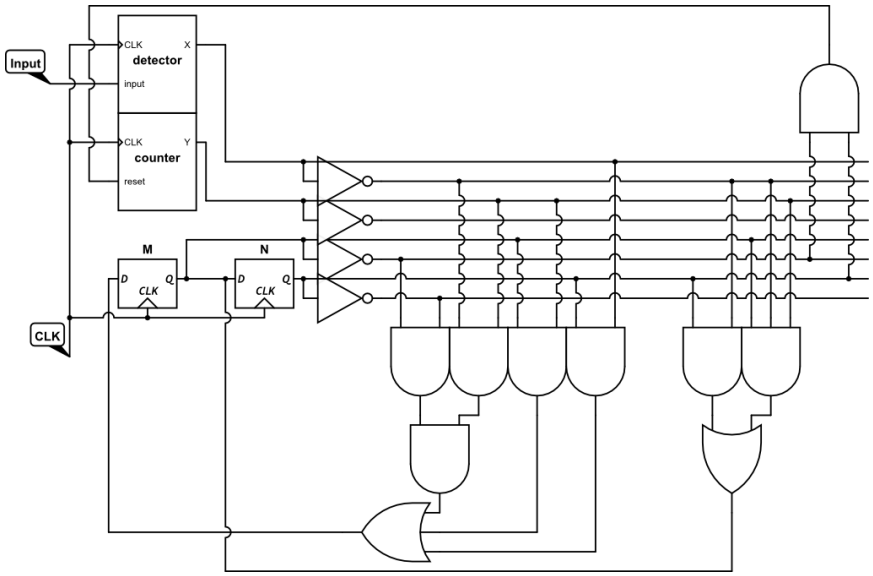
MN XY	00	01	11	10
00	0	1	0	0
01	0	0	1	1
11	x	x	x	x
10	1	0	0	1

K-Map for N'

MN XY	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	x	x	x	x
10	0	1	0	0

$M' = \bar{M}\bar{N}\bar{X}Y + M\bar{Y} + NX$
$N' = N\bar{X} + M\bar{X}Y$
Then consider the reset for counter. When in state A(0,1), the reset will always be true and the counter will stay in 00000000000 and so the Y is always 1. However this does not matter for state changing, because when in state A, Y have no relation with next state. The logic is safe.
When in state B,C, the counter does not need any resets.
reset= $\bar{M}N$





(d) The complexity mainly comes from the combination of three state machine: the state of framing pattern (M,N), the counter and the pattern detector. To make the circuit work properly need to combine the input and output of these three together.
(Do NOT know what to answer for (d)..What does complexity for gates mean?)

4 Exercise 4

current	next X=0	next X=1	Output X=0	Output X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

Notice no difference between E G.

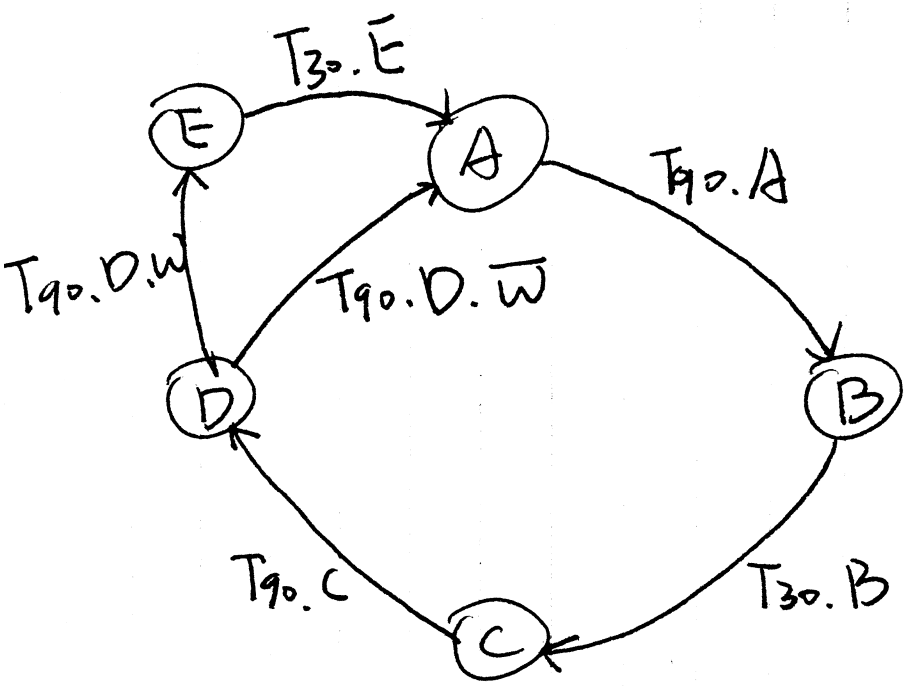
current	next X=0	next X=1	Output X=0	Output X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	E	F	0	1

Notice no difference between F D.

current	next X=0	next X=1	Output X=0	Output X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	D	0	1
E	A	D	0	1

5 Exercise 5

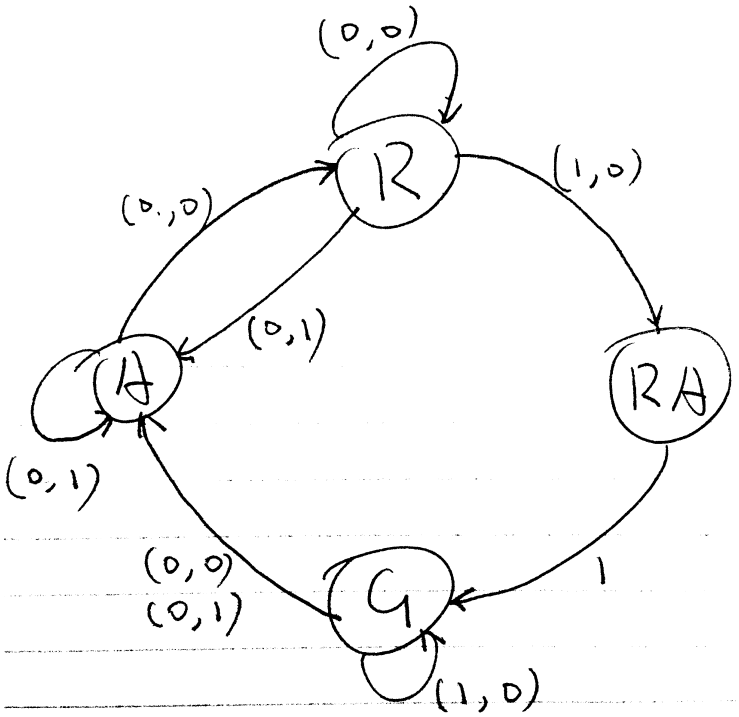
Define:
A,B,C,D: the state of the light A,B,C,D.
E: the state of flashing amber.
W: the state of then button.
M,N: the state of the traffic light Red, Red Amber, Green, Amber.
I want 3 kinds of synchronous state machine from these states define: the main traffic light control logic, the state of button, the traffic logic. And 7-bit counters.



Main control state transition table:

ABCDE	A'B'C'D'E'	30-sec,90-sec	W
10000	10000	x,0	x
10000	01000	x,1	x
01000	01000	0,x	x
01000	00100	1,x	x
00100	00100	x,0	x
00100	00010	x,1	x
00010	00010	x,0	x
00010	10000	x,1	0
00010	00001	x,1	1
00001	00001	0,x	x
00001	10000	1,x	x

R(0,0)RA(0,1)G(1,0)A(1,1)
T is the corresponding state for light T is green from main control state control machine.



MN	M'N'	T,E
00	00	$0, 0$
00	01	$1, x$
00	11	$0, 1$
01	10	x,x
10	10	$1, x$
10	11	$0, x$
11	00	x,0
11	11	$x, 1$

K-Map for M':

$MN\ TE$	00	01	11	10
00	0	1	x	0
01	1	1	x	1
11	0	1	x	0
10	1	1	x	1

K-Map for N':

$MN\ TE$	00	01	11	10
00	0	1	x	1
01	0	0	x	0
11	0	1	x	0
10	1	1	x	0

$M' = E + \bar{M}N + M\bar{N}$
$N' = \bar{M}\bar{N}E + \bar{M}\bar{N}T + ME + M\bar{N}\bar{T}\bar{E}$

Truth Table for Rd,Am,Gr:

MN	RdAmGr
00	100
01	110
10	001
11	010

$Rd = \bar{M}$
$Gr = M\bar{N}$

Because the amber need to flash when the $E = 1$ get Truth Table for Am:

N	E	2nd least significant bit of the counter	Am
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$Am = N\bar{E} + N2_B$

2_B is the state of the 2nd least significant figure of the counter because the system CLK is 1 Hz so the high level of the least significant figure will last 0.5 seconds and so the 2nd will last 1 second which satisfies the requirement 1-sec-on-1-sec-off.

$90|_{10} = 1011010|_2$ $30|_{10} = 11110|_2$
reset logic for the counter (also the next state signal for the main control machine):
define the 30-sec and 90-sec signal as T_{30}, T_{90}
$reset = (B + E)T_{30} + (A + C + D)T_{90}$

Button use a R-S latch to store the state W.

Some other possible methods:

1. The main control circuit:

   (a) The state assignment I choose kind of a shift register assignment. The difference is there is a choose to state A or state E based on W after the machine approach the state D. This is because the change of state always flow to one way of the state diagram which fits property of a shift register well.

   (b) The state encoding I choose one-hot which is easier and clearer to build the logic based on a shift register.

   (c) It is actually possible to design a state digram with a "waiting flash" state. However I choose to use a RS-Latch to store this state and release it to 0 when the flash state(E) is finished. This simplifies the design of the main control machine.
   Also I add a NOT gate on the set input of the latch to avoid (1,1) error input while the machine itself resets the state W.

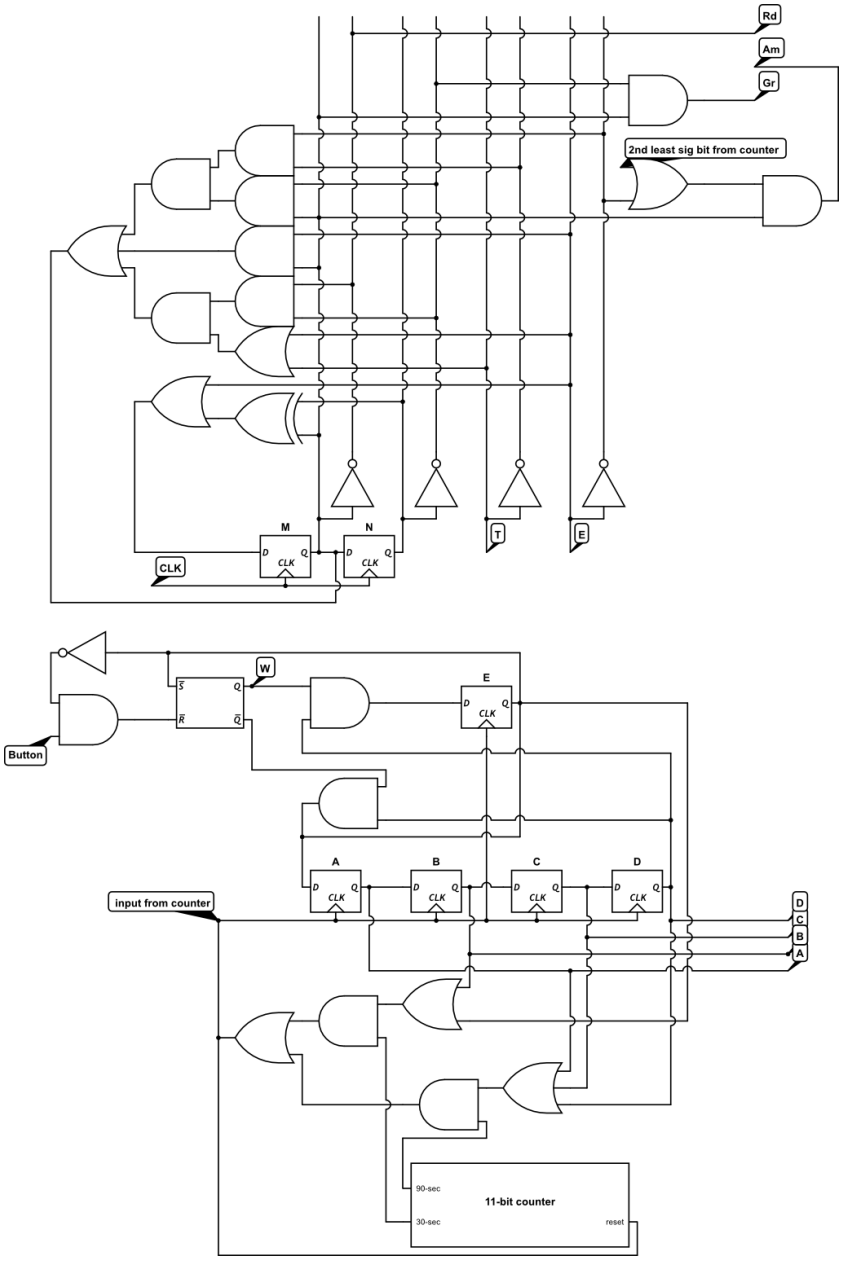
2. The traffic light circuit:

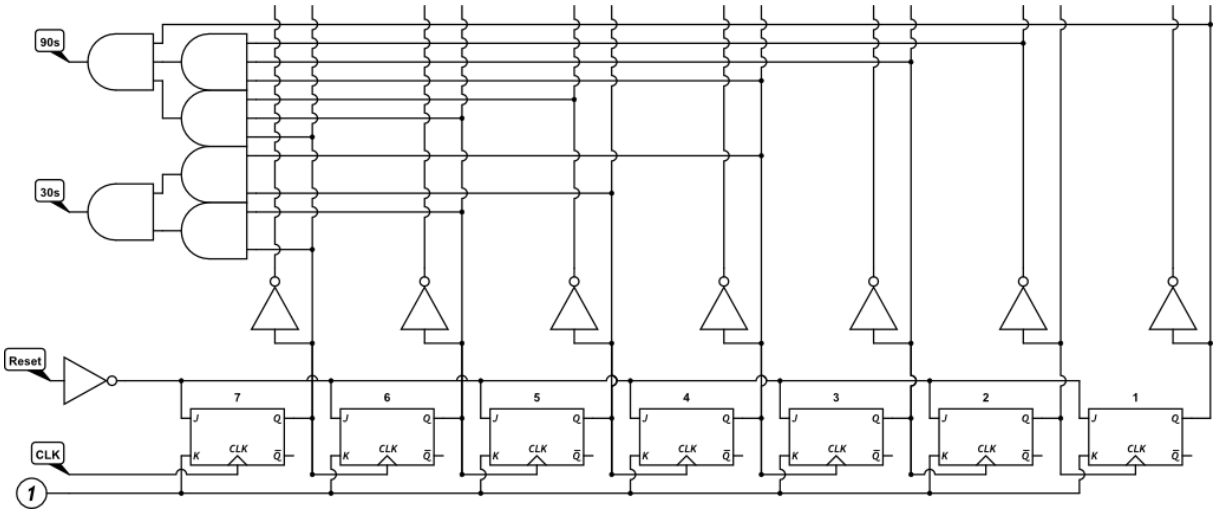
(a) I choose to use 2 state register because the circuit need to take 2 input(THIS MAY BE IMPROVED TO ONE INPUT) and I expect to simplify the circuit transition logic.

(b) This is a Mealy machine because input E and 2_B is in the combination logic output for Am. This is clearer in the logic when output the flash Amber light because I assumed there are only 2 register and so 4 state for the traffic light control machine to make it a Moore machine will need more state register (the flashing state is needed.) and so complicated the circuit.

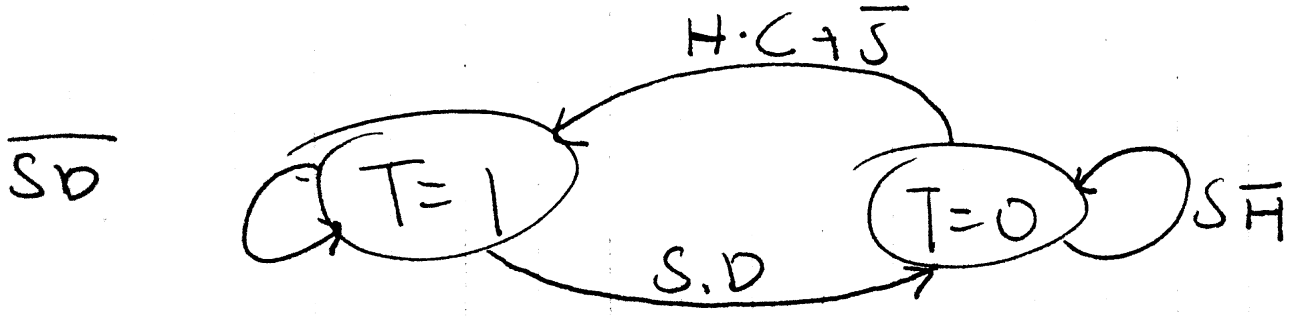
(c) And also I feel it is reasonable to use the second least significant bit from the counter to control the flashing. This avoid adding extra components.

3. The 11-bit counter uses the J-K FF because here we need to apply the toggle and reset two operations to the counter, J-K FF is the best choice for having both of them.





6 Exercise 6



For (b) I can use the hold and toggle logic or set and reset logic of J-K FF. Are they both correct? (The same question for Exercise 2.)

* Mark the first line state 1,2,3 and second line state 4,5,6.

current state	next state	input	output
1	2	11	0
2	3	01	0
2	4	00	1
3	2	11	0
3	6	10	0
4	1	00	0
5	1	01	0
5	2	11	0
6	2	11	0
6	5	10	0

I cannot find any equal states...
I will ask during the supervision.

7 Exercise 7

(a)

current state	next state
000	001
001	010
010	011
011	100
100	101
101	000

A' K-Map

AB C	0	1
00	0	0
01	0	1
11	x	x
10	1	0

B' K-Map

AB C	0	1
00	0	1
01	1	0
11	x	x
10	0	0

C' K-Map

AB C	0	1
00	1	0
01	1	0
11	x	x
10	1	0

$A' = A\bar{C} + BC$
$B' = B\bar{C} + \bar{A}\bar{B}C$
$C' = \bar{C}$

(b)

current state	next state	E
00	00	0
00	01	1
01	01	0
01	11	1
11	11	0
11	10	1
10	10	0
10	00	1

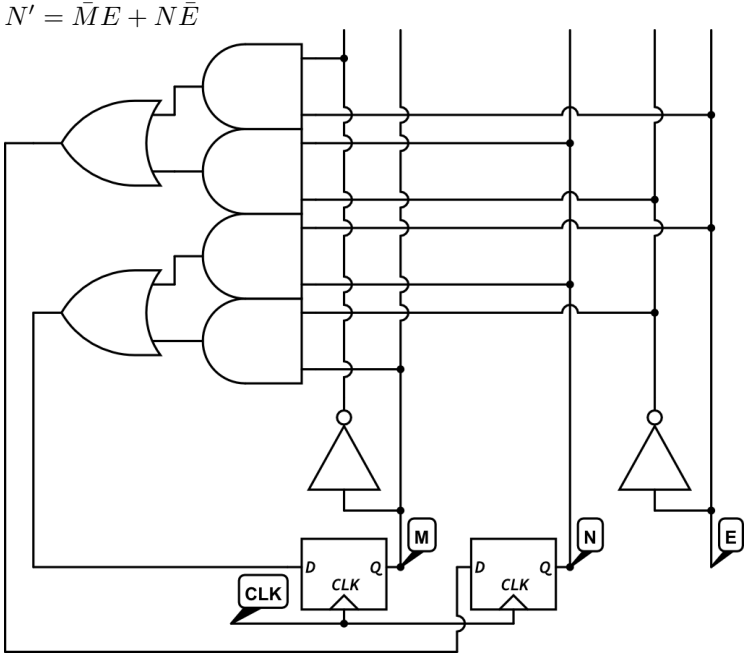
M' K-Map

MN E	0	1
00	0	0
01	0	1
11	1	1
10	1	0

N' K-Map

MN E	0	1
00	0	1
01	1	1
11	1	0
10	0	0

$M' = M\bar{E} + NE$
$N' = \bar{M}E + N\bar{E}$



(c) To pause the counter NM we need to connect $A\bar{B}C$ to the E input of the counter MN in this way MN will only count forward when ABC is 101.

ABC MN	00	01	11	10
000	0	0	1	0
001	1	1	1	1
011	1	1	1	1
010	0	1	0	0
110	x	x	x	x
111	x	x	x	x
101	1	1	1	1
100	0	0	1	0

The logic of signal will be:$C + B\bar{M}N + \bar{B}MN$