LLVM的RVV支持现状和经验

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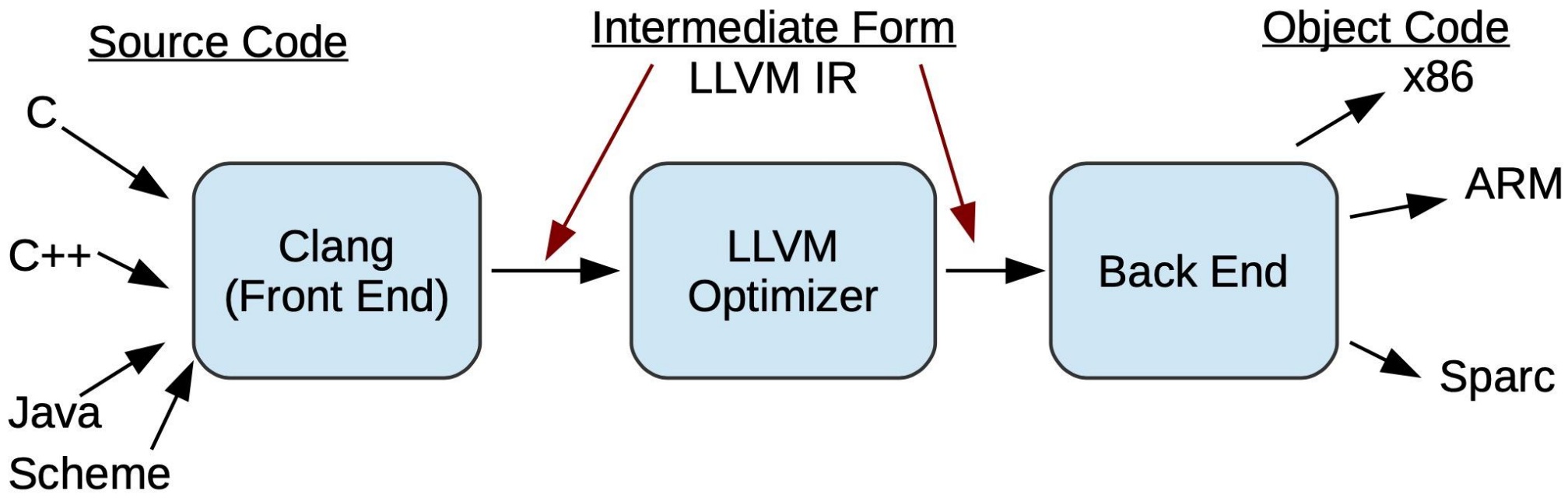
Clang/LLVM简介

- sub-projects
  - Clang：C/C++/Objective-C compiler
  - LLDB：调试器
  - LLD：链接器
  - libc++：C++标准库
  - polly：多面体优化
  - ……

The LLVM Project is a collection of modular and reusable compiler and toolchain technologies. Despite its name, LLVM has little to do with traditional virtual machines. The name "LLVM" itself is not an acronym; it is the full name of the project.

摘自： https://llvm.org

Clang/LLVM简介



RVV简介

- RISC-V “V”Vector Extension
  - https://github.com/riscv/riscv-v-spec
  - 共有5个版本：v1.0-rc1, v0.10, v0.9, v0.8, 0.7.1
  - Vector length 可变
- Intrinsic
  - 向量类型
  - Intrinsic函数
  - https://github.com/riscv/rvv-intrinsic-doc

RVV支持现状

- We would like to announce that the RISC-V V-extension v0.10 has been implemented in LLVM and the work has been committed upstream.
- Barcelona Supercomputing Center (BSC), Codeplay Software, and SiFive have worked together to implement the RVV C API intrinsics for the V-extension and have implemented the foundation of CodeGen for Vector Length Specific (VLS) and Vector Length Agnostic (VLA) autovectorization for RISC-V.
- What we have committed to LLVM upstream:
  - * Support for the v0.10 V-extension specification
  - * Support for the RVV C intrinsics in https://github.com/riscv/rvv-intrinsic-doc/tree/v0.10
  - * Implement the draft vector calling convention in https://github.com/riscv/riscv-elf-psabi-doc/pull/171

来自： https://lists.llvm.org/pipermail/llvm-dev/2021-May/150592.html

RVV支持现状

- We would like Known issues:
  - C intrinsics for Zvlsseg implementation is under discussion:
    - https://lists.llvm.org/pipermail/llvm-dev/2021-March/149518.html
  - What type we should use for fp16 is under discussion:
    - https://github.com/riscv/rvv-intrinsic-doc/issues/18#issuecomment-818472454
  - RISC-V RVV example:
    - https://github.com/riscv/rvv-intrinsic-doc/blob/master/rvv_saxpy.c

- Build command:
  - clang --target=riscv64-unknown-elf -march=rv64gcv0p10 -menable-experimental-extensions rvv_saxpy.c -o rvv_saxpy.elf

来自： https://lists.llvm.org/pipermail/llvm-dev/2021-May/150592.html

RVV支持现状

- Support for the v0.10 V-extension specification
  - 寄存器
    - llvm/lib/Target/RISCV/RISCVRegisterInfo.td
    - llvm/lib/Target/RISCV/RISCVSystemOperands.td
  - 指令
    - llvm/lib/Target/RISCV/RISCVInstrFormatsV.td
    - llvm/lib/Target/RISCV/RISCVInstrInfoV.td
  - 汇编解析
    - llvm/lib/Target/RISCV/AsmParser
  - 反汇编
    - llvm/lib/Target/RISCV/Disassembler

RVV支持现状

- Support for the RVV C intrinsics
  - LLVM
    - Intrinsic接口
      - llvm/include/llvm/IR/IntrinsicsRISCV.td
    - Intrinsic->PseudoInstr->MI
      - llvm/include/llvm/IR/RISCVInstrInfoVPseudos.td
      - llvm/include/llvm/IR/RISCVISelDAGToDAG.cpp
      - llvm/include/llvm/IR/ RISCVFrameLowering.cpp
      - llvm/include/llvm/IR/RISCVMCInstLower.cpp
      - …..

RVV支持现状

- Support for the RVV C intrinsics
  - Clang
    - Builtin Instruction
      - clang/include/clang/Basic/riscv_vector.td
      - clang/utils/TableGen/RISCVVEmitter.cpp
      - clang/lib/CodeGen/CGBuiltin.cpp
      - ……

RVV支持现状

- C intrinsics for Zvlsseg implementation
  - https://github.com/riscv/rvv-intrinsic-doc/issues/95
  - Load/Store接口
    - 现在： void vsseg2e8_v_i8mf8x2 (int8_t *base, vint8mf8x2_t value, size_t vl);
    - 将要修改为： void vsseg2e8_v_i8mf8 (int8_t *base, vint8mf8_t v0, vint8mf8_t v1, size_t vl);
  - 删除vget, vset, vcreate, and vcopy intrinsics.

RVV支持现状

- What type we should use for fp16 is under discussion:
  - https://lists.llvm.org/pipermail/cfe-dev/2021-March/067847.html
  - _float16 vs fp16

RVV支持现状

- RVV-Intrinsic后来就躺平了?
  - 减少llc二进制文件大小：https://reviews.llvm.org/D97033
  - vsetvli insert pass : https://reviews.llvm.org/D102737
  - Reduce impact `riscv_vector.h` when testing: https://reviews.llvm.org/D100529
  - …….

RVV支持现状

- 我们参与的部分
  - LLVM
    - 汇编器
    - 栈分配
    - 自动向量化
    - ……
  - RVV 规范讨论
  - ……

其它扩展我们的一些实现

- Scalar cryptography extensions
  - Spec: https://github.com/riscv/riscv-crypto/
  - Intrinsic: https://github.com/rvkrypto/rvkrypto-fips

  - 我们的实现
    - https://reviews.llvm.org/D98136
    - https://reviews.llvm.org/D102310

其它扩展我们的一些实现

- code-size reduction extension
  - Spec： https://github.com/riscv/riscv-code-size-reduction/blob/master/ISA%20proposals/Huawei/Zce_spec.adoc#zce-configurations
  - 我们的实现
    - https://github.com/plctlab/llvm-project/commits/riscv-zce-extension

其它扩展我们的一些实现

- P Packed SIMD Extension
  - Spec： https://github.com/riscv/riscv-p-spec
  - 我们的实现
    - https://reviews.llvm.org/D94579

其它扩展我们的一些实现

- zfinx
  - Spec： https://github.com/riscv/riscv-zfinx
  - 我们的实现
    - https://reviews.llvm.org/D93298

浅薄的经验

- **一定要关注upstream进展及时更新代码**
  - https://reviews.llvm.org
  - https://github.com/llvm/llvm-project
- **写不出代码时**
  - 开issue或者发给llvm-dev邮件
  - 拆分问题，基本可以找到参考代码（例如：其它target)
  - 打开方式

浅薄的经验

- 一些有用的文档推荐
  - https://llvm.org
  - https://clang.llvm.org/docs/index.html

欢迎加入我们

大佬带队，没问题～

沟通障碍，不存在～

谢谢