



https://gitee.com/shiliupi/shiliupi99







SSH

ZYNQ

7020



RV

ZedBoard

ZYNQ FPGA

HostIO/AXI Convertor

Rocket Chip

System

DRAM

1. Target Application (riscv binary)

2. RISC-V Kernel (RISC-V Linux)

3. Rocket Chip (Core on FPGA <> host ARM on Zyng via AXI)

(RISC-V) Front-end Server (on ARM core <> Rocket Chip)

5. Zyng ARM Core (Linux on Soc)

6. Development Board (ZedBoard/Shiliu PI&SD card)

7. External Communication (PC <> FPGA over Ethernet.)

8. User Interface (SSH Client terminal on PC.)



FSBL UBoot

bbl

Kernel

Shiliu Pi 99 🍐

Root filesystem

A Core
B Cache
C Rocc Tile TileLink L2toIO Network TileLink/AXI4 Bridge

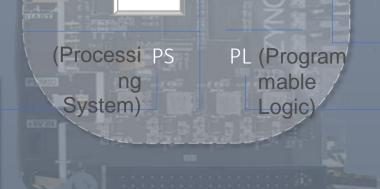
AHB & APB Peripherals

High-Speed IO Device



OpenWrt linux

LuCl



HTIF (4)

(5)

ARM

bbl(UC) Berkeley Bootloader

openEuler(中科) ② linux

GNU Chess



Step1: Project Setup

- Download the files needed
- Project setup

Step2: Genetate the files for zedboard

- Bitstream
- FSBL(first stage boot loader)
- uboot for the Zyng ARM Core
- boot.bin
- Other files

Step3: Test

- SSH root@192.168.1.5
- Booting Up and Interfacting with the RISC-V Rocket Core

(4) The HTIF is the Host/Target interface, which has the front-end server (riscv-fesvr, running on your host compter) communicating with the target design (Sodor). The riscv-fesvr loads the binary into the Sodor memory via the HTIF mem ports, and then uses the Control/Status Registers to bring the core out of reset. Once the program is finished, Sodor tells the riscv-fesvr it is finished via the tohost CSR and simulation ends.



WLAN: Shiliu Pi 99

root @ 99.99.99.99.

** /run-rv-linux.sh

gnuchess

white (1): e4

my move is:?

















1. Model 2. Reconstruct 3. Map 4. 贡献 5. 建立. 6. 丰富

DLP games 1099 + 262 民族棋中国史 = LuckyLudii

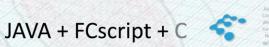




中文 PYthon JS LuaJIT



民族棋 机器博弈





Shiliu Pi 99



- RVWeekly

- PLCT

- B站占

- EEworld

课程: **RV4Kids:**

- 1. 数字系统设计
- 2. 计算机体系结构
- 3. 软硬件接口
- 4. 操作系统
- 5. 计算机软硬件算法

专业:

- 自动化
- 微电子
- 电子信息
- 计算机
- 4. V8 for RISC-V 5. Verilog 入門教學

1. 计算机组成与设计:

RISC-V 2. RISC-V

生态 3. 方舟·编译

指令集开源软件

技术入门与实战

6. 开发一个RISC-V上的操作系统

学习:建立自己的知识地图





Host: Raspberry Pi 4 Model B Rev 1.4

Kernel: 5.10.0-openEuler-21.03-rpi









3. 语音助手



5. 智能网关



QEMU + FPGA => SoC



rv64imafde

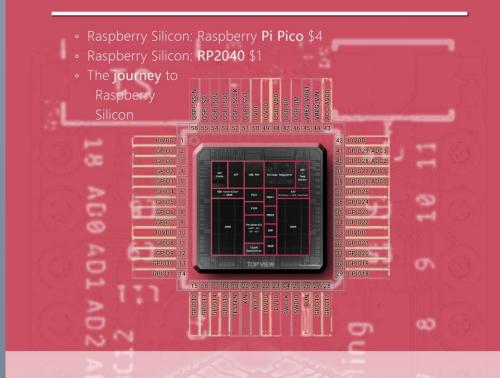














SIGer 学习 27.5% NY4KIDS

• RVWeekly

一青少年开源文化期刊

- = Shiliu Si = 石榴核
- · Shiliu Pl 99 risc-v on FPGA

SIGer 编委会

A microcontroller Datasheet









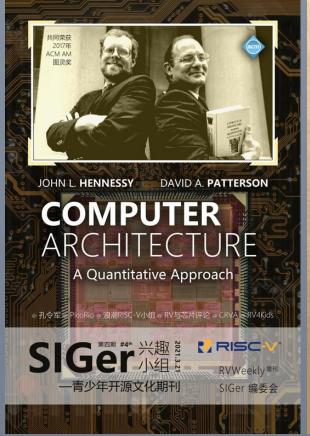


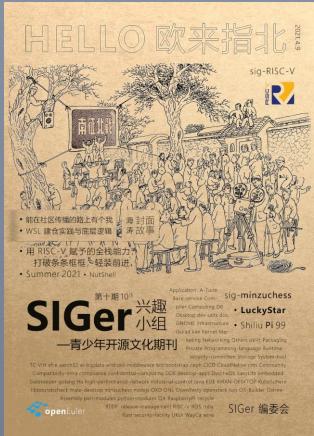


RV4Kids 为科普而生!













RV4kids 开源 🔟



百度一下















