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HW 2 Report

3.1. The value will be Adrs+4: The design move the signal via an adder with '4' in the other edge, and in the next clock outputs it to Tested\_PC\_plus\_4\_pID.

3.2 In our current design, we do branch. In the final pipelined CPU, we don't expect to branch right away. The condition is checked after the decode phase.

3.3.

Yes, we branched.

We see the values of Tested\_PC\_plus\_4\_pID and Tested\_IR\_reg, even though they are in the next instruction, because they are set in the next clock, in which we branch (=change the PC to the branch\_address). In the final Piplelined-CPU design, we can also not to branch, and then these values (the next instructions) need to be executed!

1. PC\_SOURCE = '1', because we want to set the PC to point at the branch address.
2. ALU\_OP = 'x05' since we want to sub the registers in the future.
3. PC\_MUX\_OUT = ' x400020' since this is the addres that we will branch to.
4. Sext\_imm = '2' since we are going to multiply by 4, branch preparing.
5. PC\_REG='x400020' in the next clock, since the branch has happened.