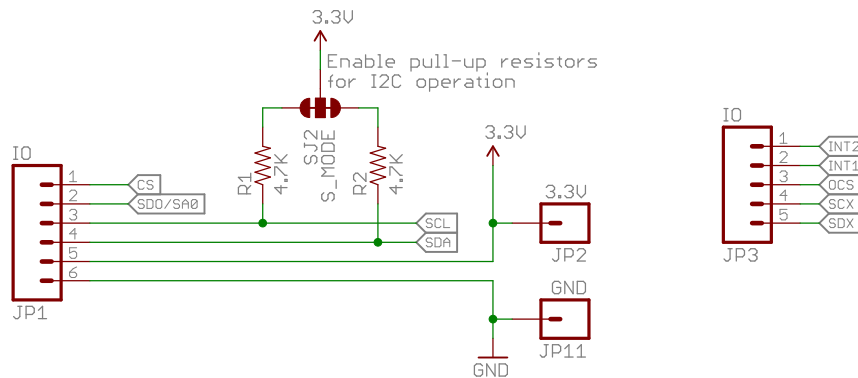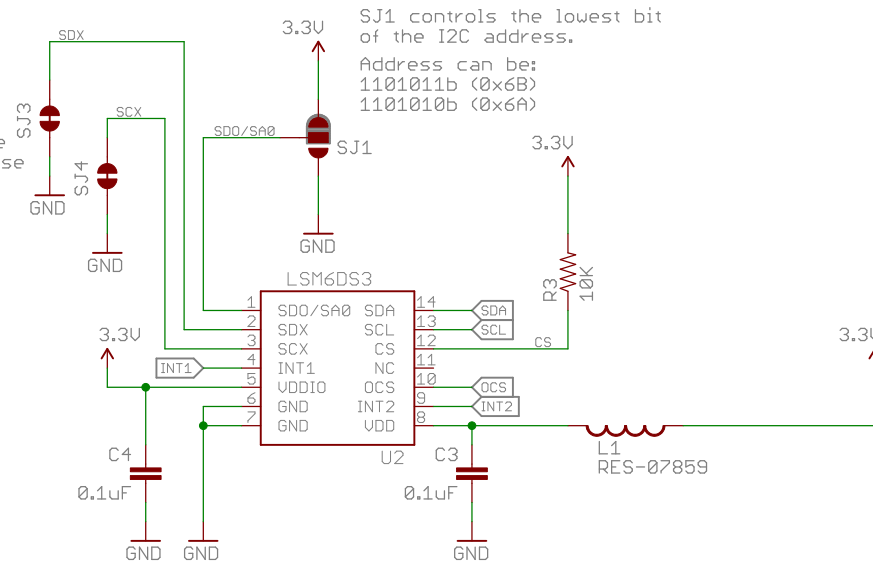# LSM6DS3

SERIAL MODES
MODE1: Slave-only mode
   I2C or SPI
MODE2: Sensor Hub mode
   I2C or SPI with master I2C port
MODE3: AUX SPI mode
   I2C and SPI access (Multi-read)

SJ1 controls the lowest bit of the I2C address.

Address can be:
1101011b (0x6B)
1101010b (0x6A)

If downstream SPI devices are hosted by the LSM6DS3, release SCx and SDx from ground by opening SJ3 and SJ4.

3.3V

SDX

SCX

SDO/SA0

SJ3

SJ4

SJ1

GND

GND

GND

3.3V

R3
10K

CS

3.3V

INT1

3.3V

LSM6DS3

1	SDO/SA0	SDA	14
2	SDX	SCL	13
3	SCX	CS	12
4	INT1	NC	11
5	VDDIO	OCS	10
6	GND	INT2	9
7	GND	VDD	8

U2

SDA
SCL

OCS
INT2

C4
0.1uF

C3
0.1uF

L1
RES-07859

GND

GND

GND

3.3V

Enable pull-up resistors for I2C operation

SJ2
S_MODE

R1
4.7K

R2
4.7K

IO

1	CS
2	SDO/SA0
3	
4	SCL
5	SDA
6	

JP1

SCL
SDA

3.3V

3.3V

JP2

GND

JP11

GND

IO

1	INT2
2	INT1
3	OCS
4	SCX
5	SDX

JP3

TITLE: LSM6DS3_Breakout_v10

Design by: Marshall Taylor

REV:
v10

Date: 8/6/2015 3:20:12 PM

Sheet: 1/1

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