Quiz 4

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Queues

2/2 points (graded)

In this question, consider the differences and similarities between a **first in first out (FIFO) queue** and a **multiple access circular queue (MACQ)**.

In what ways are a MACQ different from a traditional FIFO?. Check all that are True

- [ ] A MACQ is of a finite size whereas a FIFO size is infinite.
- [x] After filling up a MACQ/FIFO, a MACQ is remains always FULL whereas a FIFO can become empty.
- [x] A FIFO read is destructive whereas a MACQ read is non-destructive.
- [x] In a FIFO one cannot access elements out of order whereas a MACQ allows that.

Submit

✔ Correct (2/2 points)

PID Controller

1/1 point (graded)

A **PID Controller** has three components, the proportional, integral and the derivative. The controller attempts to minimize the error over time by adjustment of a control variable u(t), which drives the actuator(s):

u(t) = Kp*e(t) + Ki*integral of {e(t)} + Kd*derivative of {e(t)}

Glossary

Discussion Board

where Kp, Ki, and Kd denote the coefficients for the proportional, integral, and derivative terms, respectively.

Check all statements that are True

- [ ] A PID controller is used in an open-loop control system.
- [ ] When used in a controller all three terms must be weighted equally
- [ ] When used in a controller all three terms must have non-zero design parameters, Kp, Ki and Kd
- [x] The derivative term is used to anticipate error and provide a correction
- [x] The integral term is used to eliminate offset errors
- [x] The proportional term is used to improve response time

✔

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✔ Correct (1/1 point)

Edge-triggered Interrupts

2/2 points (graded)

Consider the basic approach to edge-triggerred interrupts. Assume the time between edges is long enough to allow the ISR to run to completion.

Which of the following statements are true? Check all that are True

- [x] Edge-triggering on the MSP432 can only be set for rising edge or falling edge but not both
- [ ] Edge-triggering on the TM4C123 can only be set for rising edge or falling edge but not both

- [ ] Consider the case where 2 or more pins from the same port are configured to request edge-triggered interrupts. If multiple pins are triggered simultaneously, it is possible to loose one of the events.
- [x] Consider the case where 2 or more pins from the same port are configured to request edge-triggered interrupts, the same interrupt handler is called no matter which pin of that port was the trigger of the interrupt.
- [x] If the software does not take steps to clear the flag that triggered the interrupt inside the ISR, then the ISR will be called repeatedly.

✔

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✔ Correct (2/2 points)

Switch Debouncing

1/1 point (graded)

Consider the general situation of debouncing a switch. In other words, assume the switch bounces up to 2ms after each touch and after each release. While bouncing there may be 0, 1, ...,10 extra edges.

Which of the following statements is true? Check all that are True

- [ ] A bouncing switch is a malfunctioning switch, good switches don't bounce.
- [x] A valid debouncing solution is to read a switch, wait an amount of time that the switch is known to bounce and read it again to see if it is in the same state as the first read.
- [ ] Interrupts cannot be used to solve switch debouncing
- [x] An RTOS solution to debouncing uses semaphores and sleeping

✔

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✔ Correct (1/1 point)

Priority Scheduler

2/2 points (graded)

Which of the following statements are true about priority-based schedulers?

Check all that are true

- [ ] The priority of a task cannot be changed over the task's lifetime
- [ ] The scheduler in the simple implementation given in Section 4.3.1 assumes that all tasks have unique priorities. In other words, there are no two tasks with the same priority.
- [ ] The scheuler in 4.3.1 maintains the task list in priority order so it takes only one step to find the highest priority task.
- [x] Priority inversion occurs when a lower priority task temporarily blocks a higher priority task from running due to a shared resource.

✔

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✔ Correct (2/2 points)

Schedulers

2/2 points (graded)

Please match the following scheduling algorithm with the letter of their corresponding rationale.

Round robin scheduler

B ✔

Priority scheduler assigning the highest priority to the task with the shortest time left to completion

D ✔

Priority scheduler assigning priority according to the frequency at which each task runs; assigning the highest priority to the most frequent task

A ✔

Priority scheduler with variable priority, decreasing priority if a task runs to completion

C ✔

A. Allows you to apply the **Rate Monitonic Theorem**

B. This scheduler is good for minimizing average response time across multiple threads.

C. **Multi-level feedback queue**

D. This scheduler is good for minimizing turnaround time across multiple threads

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✔ Correct (2/2 points)