TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Masters of Aeroespace Engineer, Técnico, University of Lisbon

Laboratory Report

Group 37

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1 Introduction

The objective of this laboratory assignment is to choose the best architecture of the Gain and Output amplifier stages in order to build an audio amplifier. This assignment allowed us to deal with important concepts such as BJTs Transistors and its diverse utility in circuits. We did this while paying attention to the merit of the project designed.
This merit is calculated exactly as the next equation:

$$M = \frac{voltageGain * bandwidth}{cost * lowerCutoffFreq} \tag{1}$$

Being the cost the following:

- cost = cost of resistors + cost of capacitors + cost of transistors
- cost of resistors = 1 monetary unit (MU) per kOhm
- cost of capacitors = 1 MU/μF
- cost of diodes = 0.1 MU per transistor

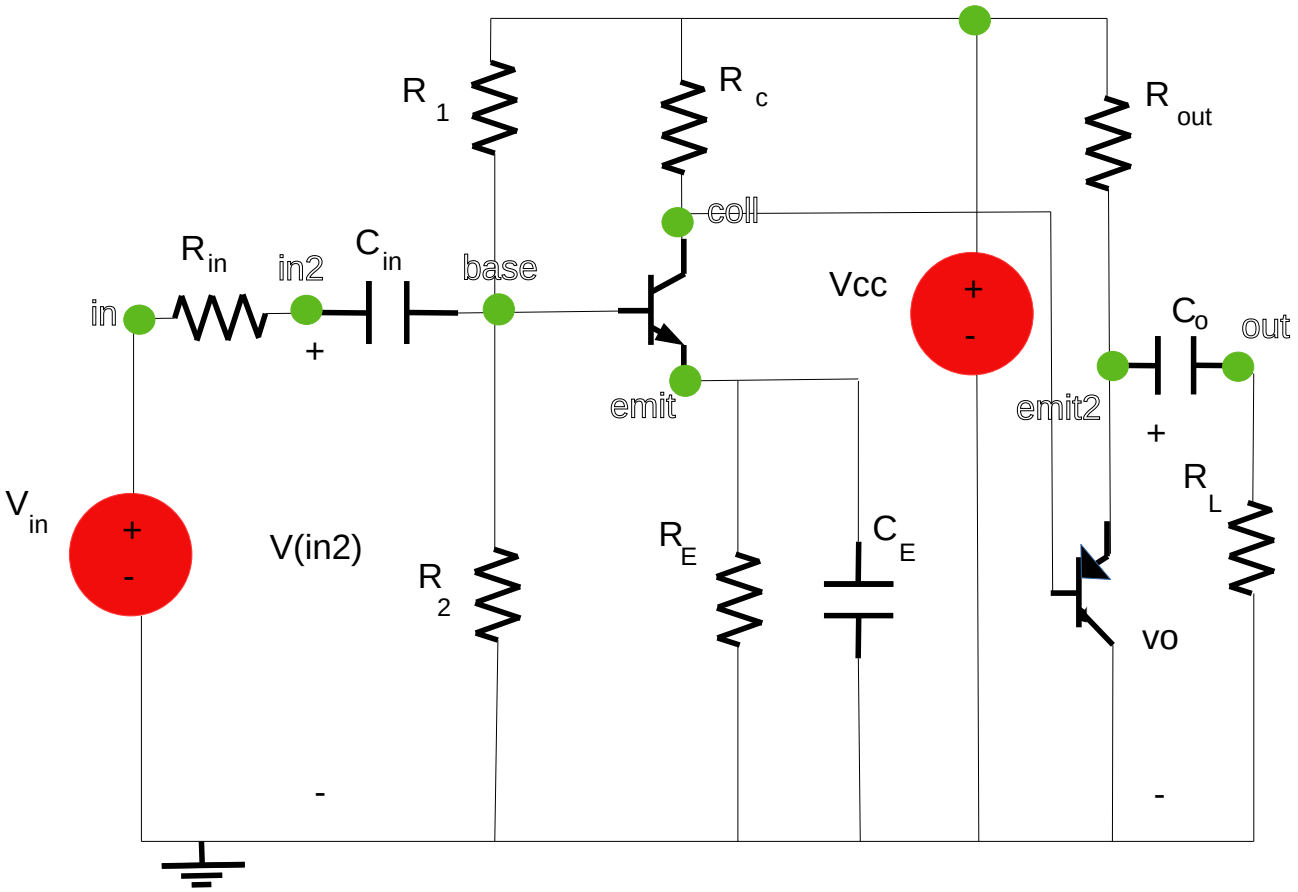

Figure 1: Audio Amplifier

To obtain the best values for the circuit, we've used the matlab simulink to optimize them for the best merit.

In Section 2, a theoretical analysis of the circuit is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

2 Theoretical Analysis

In this section we will analyse theoretical our audio amplifier circuit.
To do so, and because there were several things to be analysed, we divided the theoretical analysis in the following subsections that explain the different sectors that our circuit has and also each one will be detailed separately.

The constants values used are expressed in the following table.

2.1 Gain Stage

In the first place, we must discuss the first half of the circuit that was used. The goal of the gain stage is to ensure a high input voltage so the input signal is not degradated or distorted throughout the circuit. It also has an elevated gain associated, so this is the part that is responsible for the signal amplification.

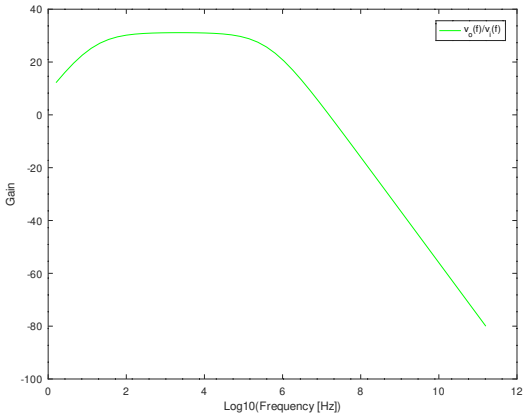

Figure 2: Gain

By analysing the figure 2, we can see that there are 3 types of elements: a NPN BJT, resistors and capacitors. The first capacitor, C_in , is a coupling capacitor, that acts as a DC Block, so that V_in doesn't introduce a DC component of 0, that would change the Operating Point (OP) of the transistor. The second capacitor, C_E , acts as a bypass capacitor, for it ensures that for low frequencies all the current flows through R_E, and for high frequencies, it passes through the capacitor. Generally, the output impedance of this stage is high, when compared with the load, being this the major reason why we cant use just this stage, and we need another one.

Both of the capacitors are being analysed in the section of Simulation Analysis.

2.1.1 Inspection analysis

2.1.2 Cutoff frequencies

2.2 Output stage

As we could see in the section of the Gain stage, we end up with a high output impedance Z_O1 . For that reason, we connect a second circuit to the output of the Gain Stage, that produce a low output impedance. This part of the stage is presented in the figure below:

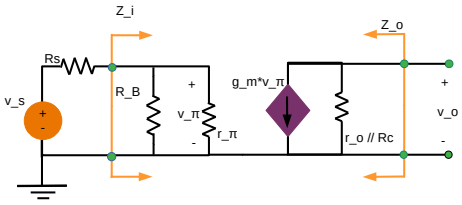

Figure 3: Output

By analysing the figure, we can conclude that this circuit presents similar components but with some differences. Instead of a NPN BJT, we use a PNP BJT, because it has a higher β_F, that lowers the output impedance as we desire. It also illustrates the use of another BJT transistor.

Another capacitor, C_o , is used with a similar goal as the previous coupling capacitor. If we didn't use this component, the gain stage would introduce a DC voltage of 0 to the second stage, which as previous would change and ruin the transistor's Operating Point.

We will end up with a lower output impedance in this stage, when compared to the load, and a higher input impedance when compared to the output impedance of the gain stage. When we combine both stages, we need to ensure that there is a compatibility between the impedances of both stages. In fact, by the voltage divider law, to make sure no voltage signal is lost, the input impedance of the second stage should be much greater than the output impedance of the first one.

To conclude, when we merge these two circuits, we end up with the BJT Audio Amplifier represented in Figure 1.

3 Simulation Analysis

In this section, Ngspice was used in order to simulate the audio converter, therefore, a brief description of the circuit modeled in NGspice is going to be presented and a comparison between the values obtained in NGspice and the ones in Octave is going to be done as well. In order to do that, transistors of the given models were used and the rest of the components specifications changed to be on par with the values through MatLab.

In the next sections we are interested in the two impedances associated with the circuit as a whole (Z_in and Z_out), both cut-off frequencies (f_{CO_L} and f_{CO_H}), the bandwidth (interval between the cut-off frequencies) and the total gain (A_V) measured in the bandpass region. The measurement of these parameters and the overall performance of the circuit is outlined in 3. We also confirm whether the BJTs are on the Forward Active Region (FAR), by comparing V_CE and V_BE for the NPN (and, analogously, V_EC and V_EB for PNP). The confirmation is presented below:

3.1 Coupling Capacitor

In our Amplifier circuit there are two coupling capacitors (C_in and C_O) but, since their functions are equivalent, we will focus on the first capacitor, the C_in . Below, is shown 2 figures of the frequency response analysis, just by changing the parameter C drastically.

As expected, the increase of the capacitance pushes the cutoff frequency to the left, without changing the higher cut-off frequency, which leads to a larger bandwidth.

As discussed previously, as ω tends to 0, the impedance Z(C_in) will tend to infinite, so this capacitor prevents the transistor from entering on either the saturation or cut-off regions, by blocking the DC component of the AUDIO IN source. This helps mantaining the Operating Point of the transistor, so that it can operate at lower frequencies, as the value of C_in increases.

3.2 Bypass Capacitor

In our Amplifier circuit there is one bypass capacitor (C_E).

Below, is shown 2 figures of the frequency response analysis, just by changing the parameter C_E.

As expected, by placing the bypass capacitor in parallel with R_E , this resistor becomes a short circuit for medium and high frequencies (because the capacitor impedance is 1/(jωC) and ω = 2πf). The amplifier's first stage gain is inversely dependent on this resistance, being that the bypass capacitor plays a very important role in maximizing the gain for medium and high frequencies.

3.3 R_c

In this subsection we will analyse the importance of R_C on the total Gain of the circuit. We also present assymptotical situations in order to fully understand that behaviour,

Analysing the figures, we can conclude that the gain increases with R_C and also antecipates the passband. This behaviour was already expected, because as described previous in the theorectical analysis of the gain, R_C is proportional to the gain. It is also important, in order to guarantee a high compatibility with AUDIO IN and to the speakers itself, to simulate the input and output impedances of the circuit. A good compatibility is ensured with a very high input impedance (Z_in) and a very low output impedance (Z_out).

The following tables show the simulation results obtained of Z_in and Z_out respectively.

As said theoretically, the load's impedance is equal to 8Ω . The value of Z_out should be lower than this value. Given that the output value of the simulation is higher, this is going to compromise the value of the merit.

3.4 Comparison

Now that we have established the concepts theoretically and shown the simulation results, we are going to do a comparison between the two approaches (theoretically and simulation) with the chosen values for the constants.

The next graphs show the theoretical and simulation graphs of the gain respectively:

In this case, the comparison of the shape can only be done on the left side, since we don't have the theoretical higher cut-off frequency. For this reason, there's no point in plotting the theoretical gain any further than 1M Hz. One should bear in mind that the theorectical analysis either considers the capacitors are short-circuited or are open-circuited (this approximation is made when for this analysis, the value of R E is either 0 or R E in Table 1, respectively). For this reason, two estimates were made (Figure 7) - in blue the capacitors are considered short-circuited; in orange the capacitors are considered open-circuited; in yellow dashed it is represented the medium-value plot, that can be considered as a rough approximation of the real gain. This theorectical approach does not guarantee a specific value for the overall gain, however it gives us a region of acceptable gains. The simulation gain obtained is satisfyingly in this prediction region. The overall shape of the graphs is similar, noting that the theoretical one can be thought of as assymptotical rather than a precise approach. In fact, as we imposed its shape, accordingly to the one given by Ngspice, it is not sensible to

variations that might occur (as the appearance of a second step in 6b). In a greater detail analysis, when remembering the values presented in the previous sub- sections - Z I and Z O , A v and f CO L -, despite the obvious differences, the comparison is sat- isfactory. Comparing the order of magnitude, when putting values side by side, they are within reasonable intervals of similarity. In fact, the lower cut-off frequencies (from tables 5 and 8) are really close, especially when you remember they are to be plotted in a logscale graph. In conclusion, the theoretical approach gives a rough perspective of the overall work condi- tions of the amplifier, which is good in a first sketch.

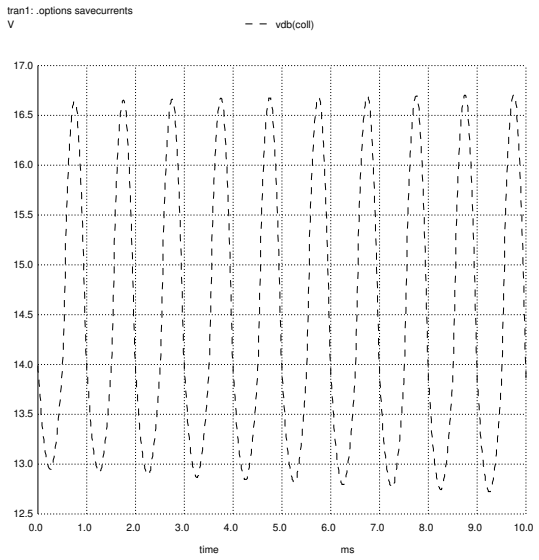

Figure 4: Output

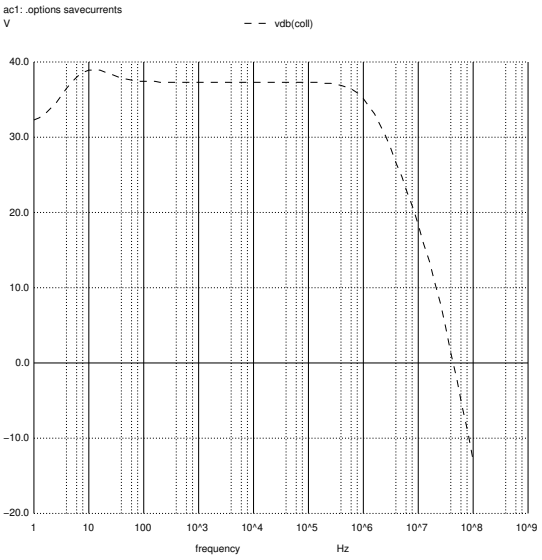

Figure 5: Output

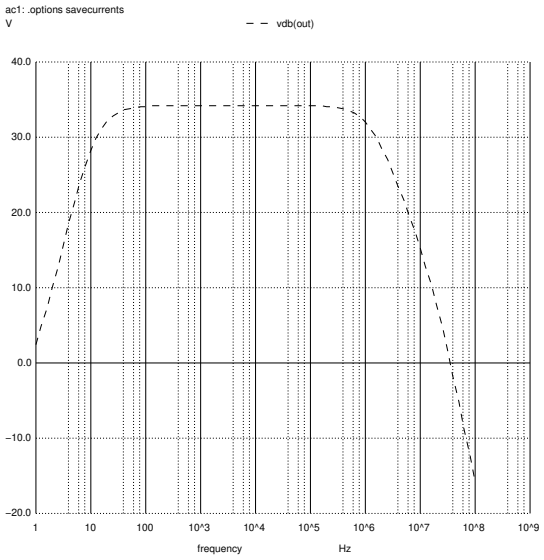

Figure 6: Output

3.5 Merit Results

From the results obtained through the Ngspice simulation and considering we used the data shown in table 1, we can compute the merit using the formula given in the lab assignment, represented in the Introduction.

The implemented circuit gave us a MERIT of ??? in NGSpice. The cost equals to ???.

4 Conclusion

In this laboratory assignment, the goal especified in the introduction has been achieved with a great merit. All analyses have been performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. When comparing these last two we conclude that there aren't any disparity between the results and therefore no errors associated. So, we conclude that the architeture that we used can be validated.