TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Masters of Aeroespace Engineer, Técnico, University of Lisbon

Laboratory Report

Group 37

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1 Introduction

The objective of this laboratory assignment is to choose the best architecture of the Gain and Output amplifier stages in order to build an audio amplifier. This assignment allowed us to deal with important concepts such as BJTs Transistors and its diverse utility in circuits. We did this while paying attention to the merit of the project designed.
This merit is calculated exactly as the next equation:

$$M = \frac{voltageGain * bandwidth}{cost * lowerCutoffFreq} \tag{1}$$

Being the cost the following:

- cost = cost of resistors + cost of capacitors + cost of transistors
- cost of resistors = 1 monetary unit (MU) per kOhm
- cost of capacitors = 1 MU/μF
- cost of diodes = 0.1 MU per transistor

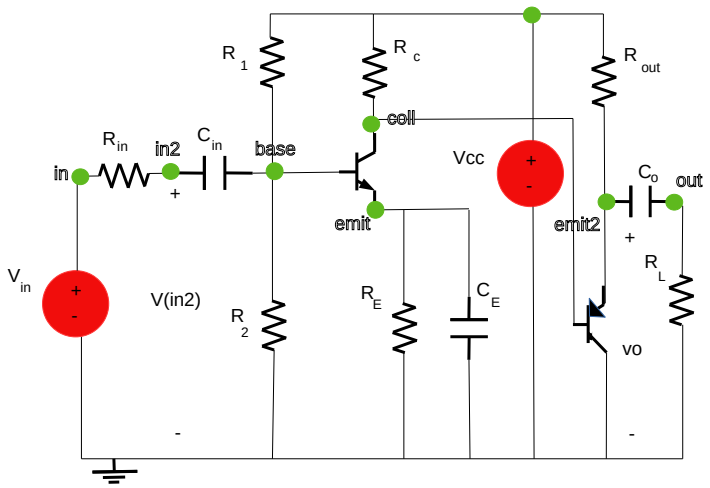


Figure 1: Audio Amplifier

In Section 2, a theoretical analysis of the circuit is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

2 Theoretical Analysis

In this section we will analyse theoretical our audio amplifier circuit.
To do so, and because there were several things to be analysed, we divided the theoretical analysis in the following subsections that explain the different sectors that our circuit has and also each one will be detailed separately.

The constants values used are expressed in the following table.

Name - Value	
C1	8.000000e-04 F
C2	8.000000e-04 F
C3	6.000000e-04 F
RB1	3.400000e+04 Ohm
RB2	3.400000e+03 Ohm
RC	4.200000e+03 Ohm
RE1	1.800000e+02 Ohm
RE2	4.500000e+02 Ohm

Table 1: Components Values

2.1 Gain Stage

In the first place, we must discuss the first half of the circuit that was used. The goal of the gain stage is to ensure a high input voltage so the input signal is not degradated or distorted throughout the circuit. It also has an elevated gain associated, so this is the part that is responsible for the signal amplification.

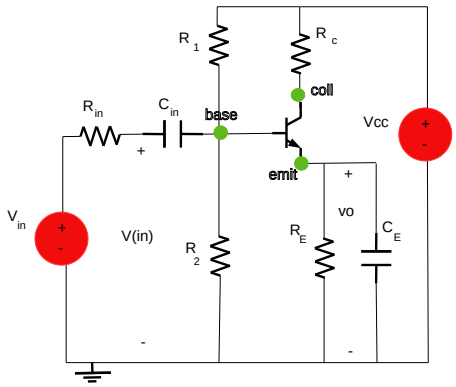


Figure 2: Gain

By analysing the figure 2, we can see that there are 3 types of elements: a NPN BJT, resistors and capacitors. The first capacitor, C_in , is a coupling capacitor, that acts as a DC Block, so that V_in doesn't introduce a DC component of 0, that would change the Operating Point (OP) of the transistor. The second capacitor, C_E , acts as a bypass capacitor, for it ensures that for low frequencies all the current flows through R_E, and for high frequencies, it passes through the capacitor. Generally, the output impedance of this stage is high, when compared with the load, being this the major reason why we cant use just this stage, and we need another one.

Both of the capacitors are being analysed in the section of Simulation Analysis.

2.2 Output stage

As we could see in the section of the Gain stage, we end up with a high output impedance Z_O1 . For that reason, we connect a second circuit to the output of the Gain Stage, that produce a low output impedance. This part of the stage is presented in the figure below:

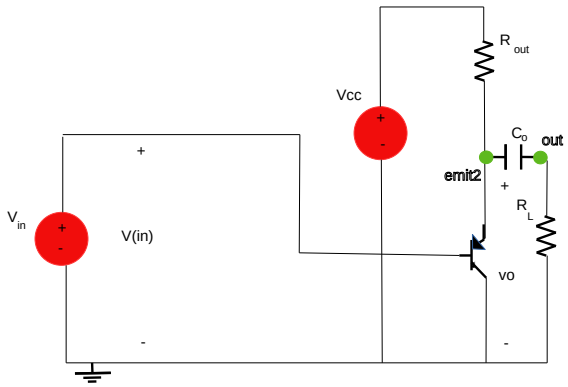


Figure 3: Output

By analysing the figure, we can conclude that this circuit presents similar components but with some differences. Instead of a NPN BJT, we use a PNP BJT, because it has a higher β_F, that lowers the output impedance as we desire. It also illustrates the use of another BJT transistor.

Another capacitor, C_o , is used with a similar goal as the previous coupling capacitor. If we didn't use this component, the gain stage would introduce a DC voltage of 0 to the second stage, which as previous would change and ruin the transistor's Operating Point.

We will end up with a lower output impedance in this stage, when compared to the load, and a higher input impedance when compared to the output impedance of the gain stage. When we combine both stages, we need to ensure that there is a compatibility between the impedances of both stages. In fact, by the voltage divider law, to make sure no voltage signal is lost, the input impedance of the second stage should be much greater than the output impedance of the first one.

To conclude, when we merge these two circuits, we end up with the BJT Audio Amplifier represented in Figure 1.

2.3 Inspection analysis

From the simulation results we know that the voltage gain curve is maximum for medium frequencies. So, in order to analyse this circuit, we start from the inspection analysis, this is, analysing the circuit for the medium frequencies to obtain the maximum voltage gain.

To make this analysis we start with computing the operating point (OP), to make sure that our trasistors are always operating in the foward active region(FAR). To compute the operating point for the gain stage we use the mesh method, which leeds to the following matrix:

$$\begin{pmatrix} R_{B1} \parallel R_{B2} & 0 & R_E \\ -\beta_f & 1 & 0 \\ -\beta_f - 1 & 0 & 1 \end{pmatrix} \begin{pmatrix} I_B \\ I_C \\ I_E \end{pmatrix} = \begin{pmatrix} \frac{R_{B2}}{R_{B1}+R_{B2}V_{CC}} - V_{BEON} \\ 0 \\ 0 \end{pmatrix} \tag{2}$$

From this matrix we've obtain the following values:

Name - Value	
VCE	3.363884e+00 V
VBEON	7.000000e-01 V
IB1	1.103113e-05 A
IC1	1.971263e-03 A
IE1	1.982294e-03 A

Table 2: Operating Point Values Gain Stage

Which indicate that the transistor is always operating in the FAR.

After this we procede to the incremental analysis, which we'll determine what is the actual voltage gain from the gain stage. The incremental circuit that is going to be analysed, the circuit for medium frequencies where the capacitor C_e is like a short circuit is the following:

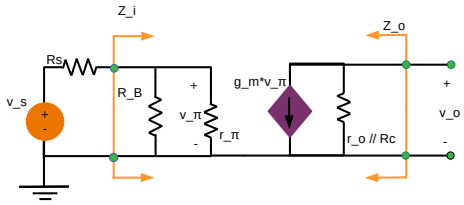


Figure 4: Incremental Circuit Gain Stage

Using the mesh method again, the expression for the voltage gain is presented below:

$$\frac{v_o}{v_i} = -g_m(R_C \parallel r_o)\frac{R_{B1} \parallel R_{B2} \parallel r_{\pi 1}}{R_S + R_{B1} \parallel R_{B2} \parallel r_{\pi 1}} \tag{3}$$

For the output stage we use the same procedure and its OP results are presented below:

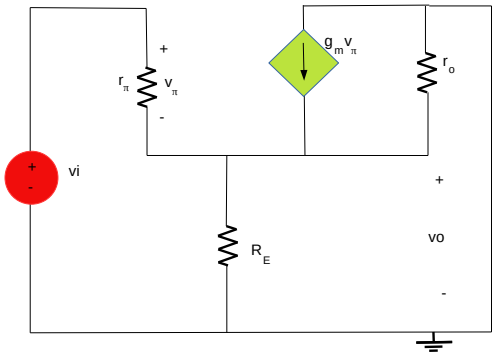


Figure 5: Incremental Circuit Output Stage

Name - Value	
VEC	4.420697e+00 V
VEBON	7.000000e-01 V
IB2	-7.377528e-05 A
IC2	1.676912e-02 A
IE2	1.684290e-02 A

Table 3: Operating Point Values Output Stage

Which means that the transistor is always operating in the FAR.

For the voltage gain in this stage, table below presents all the gains for the 2 stages and for the complete circuit.

Name - Value	
VoltageGain1	2.075755e+01 V
VoltageGain2	9.916852e-01 V
VoltageGain	1.980831e+01 V

Table 4: Volatge Gain in both stages

2.4 Impedances

In the thereotical analysis of the impedances, we will evaluate the four impedances associated with the two stages (Z_in1 & Z_out1 for the first stage, Z_in2 & Z_out2 for the second stage) as well as the two gains associated with each stage (A_V1 and A_V2, respectively). To do so, we need to perform an Operating Point Analysis to find the values necessary or the Incremental Analysis.

In the Gain stage, the input (Z_in) and output (Z_out) impedances can be derived by the Kirchoff Laws. Giving us the following equation, where R_B = R_1 // R_2

$$Z_{in1} = R_B//r_{\pi 1} \tag{4}$$

Due to the presence of the bypass capacitor and to the theoretical approach where it is assumed that the capacitors are short-circuited, we consider R_E approximately 0. It is important to say that the Gain Stage input impedance matches also with the total input impedance of the circuit, as this stage is load-independent.

On the other hand, the first stage output impedance can be obtained by:

$$Z_{out1} = r_o//R_C \tag{5}$$

Refering the second stage, by analysing the circuit we get:

$$Z_{in2} = \frac{(g_{m2} + g_{\pi 2} + g_{o2} + g_{E2})}{g_{\pi 2}(g_{\pi 2} + g_{o2} + g_{E2})} \tag{6}$$

$$Z_{out2} = \frac{1}{(g_{m2} + g_{\pi 2} + g_{o2} + g_{E2})} \tag{7}$$

And finally, the total output impedance is calculated as the following:

$$Z_{Out} = \frac{v_o}{i_o} = \frac{1}{g_{o2} + g_{m2}\frac{r_{\pi 2}}{r_{\pi 2}+Z_{out1}} + g_{E2} + \frac{1}{r_{\pi 2}+Z_{out1}}} \tag{8}$$

The 4 values are presented below,

Name - Value	
ZI1	2.811209e+03 Omega
ZO1	3.754073e+03 Omega

Table 5: optab

Name - Value	
ZI2	4.075483e+04 Omega
ZO2	1.478440e+00 Omega

Table 6: optab

Regarding to the compatibility between both stages, remembering that Z_{out1} needs to be much lower than Z_{in2}, we have satisfactory results, in order so that there is no signal degradation or loss between these stages. We can clearly affirm that V_{in2} needs to be as close as possible to V_{out2}, confirmed if we apply a voltage divider with $Z_{in2} >> Z_{out1}$:

$$V_{in2} = \frac{Z_{in2}}{Z_{in2} + Z_{out1}} V_{out2}. \tag{9}$$

2.5 Cutoff frequencies

After obtaining the gain for the medium frequencies we need to determine the frequency dependance of this gain. To do so we've used two methods called short circuit time constant (SCTC) and open circuit time constant (OCTC). The SCTC was used in the determination of the lower cutoff frequency and it consists in the determination of the equivalent resistance seen by all capacitors individually using the in the following steps:

- Short-Circuit all large Capacitors that are not being analysed
- Replace the capacitor that is being analysed by a test voltage source
- Remove all the independant sources(Short-circuit the independant voltage sources and open-circuit the independant current sources)
- Open-circuit all the small capacitors

by large capacitors we mean the capacitors implemented in the circuit and by small capacitors we mean the capacitors associated with the transistor.

After doing this steps, we use the dominant pole aproximation, which converts all poles of the graphic in just the one that has the most influence in the graphic. By these aproximation, the lower cutoff frequency is given by:

$$w_L = \sum_{n=1}^{n} \frac{1}{R_{iS} C_i} \tag{10}$$

Being n the number of large capacitors.

Proceding as described we've obtained the following expressions for the equivalent resistances:

$$R_{eq_{in}} = R_{in} + Z_{In1} \tag{11}$$

$$R_{eq_E} = \frac{1}{\frac{1}{R_E} + \frac{1+g_m r_{\pi 1}}{R_S \| R_B + r_{\pi 1}}} \tag{12}$$

$$R_{eq_{in}} = R_L + Z_{Out2} \tag{13}$$

So using the formulae 10 we've obtained the lower cutoff frequency.

Moving on to the higher cutoff frequency, we now have to use the OCTC, which has the same steps as the SCTC, but now we analyse the small capacitors associated with the transistor(C_π C_o). Another difference is the formulae associated with the dominant pole aproxiamtion, which is:

$$w_H = \frac{1}{\sum_{n=1}^{n} R_{iS} C_i} \tag{14}$$

so doing the OCTC we get:

$$R_{eq_\pi} = r_{\pi 1} \tag{15}$$

$$R_{eq_o} = r_o \tag{16}$$

And once more using the formulae 14 we've obtained the higher cutoff frequency.

Name - Value	
HighCutOff frequency	8.304945e+05 Hz
LowCutOff frequency	2.183854e+01 Hz
Bandwidth	8.304726e+05 rad/s

Table 7: Cutoff Frequencies

3 Simulation Analysis

In this section, Ngspice was used in order to simulate the Audio Converter. A brief description of the circuit modeled in NGspice is going to be presented and a comparison between the values obtained in NGspice and the ones in Octave is going to be done as well. In order to do that, transistors of the given models were used and the rest of the components specifications changed to be on par with the values through MatLab.

In the next sections we are interested in the two impedances associated with the circuit as a whole (Z_{in} and Z_{out}), both cut-off frequencies (f_{CO_L} and f_{CO_H}), the bandwidth (interval between the cut-off frequencies) and the total gain measured in the bandpass region. The measurement of these parameters and the overall performance of the circuit is well represented in the section 3.5.

Besides that, we also confirmed whether the BJTs are on the Forward Active Region (FAR), by comparing V_{CE} and V_{BE} for the NPN (and, similarly, V_{EC} and V_{EB} for PNP). The confirmation is presented below, to the NPN and PNP respectively:

Name - Value	
VCE	3.01461
VBE	0.666424
VCE greater than VBE	Correct F.A.R

Table 8: NPN Voltages and FAR confirmation

Name - Value	
VCE	4.13043
VEB7.5007	0.728441
VEC greater than VEB	Correct F.A.R

Table 9: PNP Voltages and FAR confirmation

The following table represents the results obtained from simulation in NGSpice:

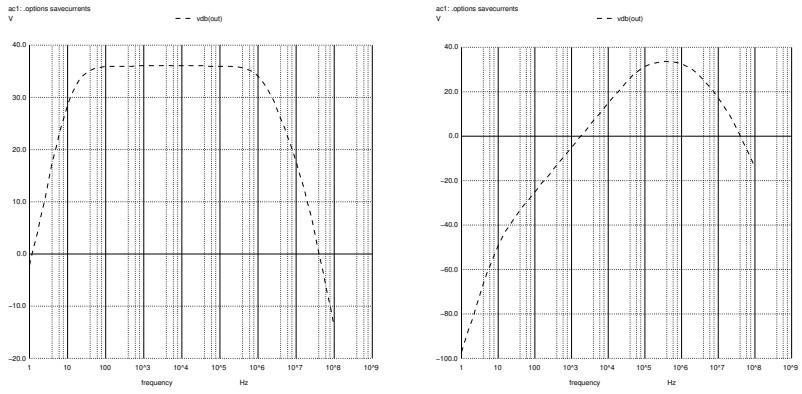
Name - Value	
V-Gain	63.2292
Bandwidth	1.33156E+06
CO-lowerFreq	18.9035
CO-7.5007higherFreq	1.33158E+06

Table 10: Results for the output

3.1 Coupling Capacitor

In our Amplifier circuit there are two coupling capacitors (C_{in} and C_O) but, since their functions are equivalent, we will focus on the first capacitor, the C_{in} .

Below, is shown the frequency response analysis to the different values of C, changing the parameter drastically.



(a) High C_in (b) Low C_in

Figure 6: C_in influence

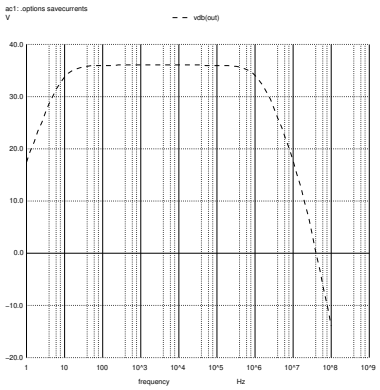
As expected, the increase of the capacitance pushes the cutoff frequency to the left, without changing the higher cut-off frequency, which leads to a larger bandwidth.

As discussed previously, as ω tends to 0, the impedance Z(C_{in}) will tend to infinite, so this capacitor prevents the transistor from entering on either the saturation or cut-off regions, by blocking the DC component of the AUDIO IN source. This helps mantaining the Operating Point of the transistor, so that it can operate at lower frequencies, as the value of C_{in} increases.

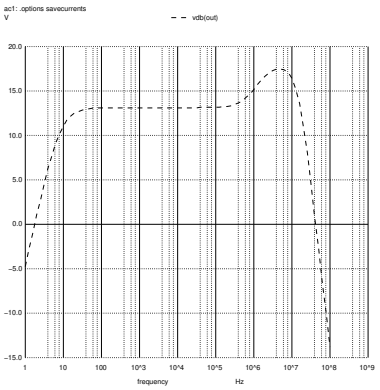
3.2 Bypass Capacitor

In our Amplifier circuit there is only one bypass capacitor (C_E).

Below, is shown 2 different graphs of the frequency response analysis, just by changing the parameter C_E.



(a) High C_E



(b) Low C_E

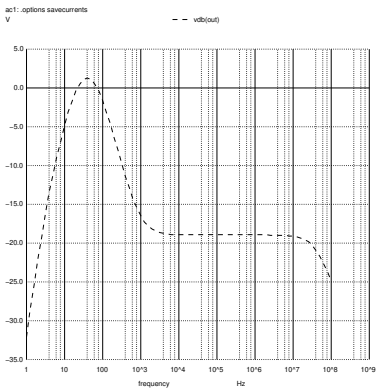
Figure 7: C_E influence

As expected, by placing the bypass capacitor in parallel with R_E , this resistor becomes a short circuit for medium and high frequencies (because the capacitor impedance is 1/(jωC) and ω = 2πf). The amplifier's first stage gain is inversely dependent on this resistance, being that the bypass capacitor plays a very important role in maximazing the gain for medium and high frequencies.

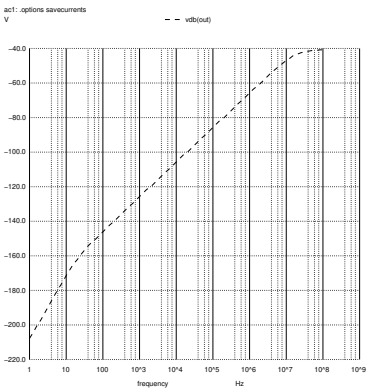
3.3 R_c

In this subsection we will analyse the importance of R_C on the total Gain of the circuit. We also present assymptotical situations in order to fully understand that behaviour.

The next graphs represent the R_C influence.



(a) High R_C



(b) Low R_C

Figure 8: R_C influence

Analysing the graphs, we can conclude that the gain increases with R_C and also antecipates the passband. This behaviour was already expected, because as described previous in the theorectical analysis of the gain, R_C is proportional to the gain. It is also important, in order to guarantee a high compatibility with AUDIO IN and to the speakers itself, to simulate the input and output impedances of the circuit. A good compatibility is ensured with a very high input impedance (Z_{in}) and a very low output impedance (Z_{out}).

The following tables show the simulation results obtained of Z_{in} and Z_{out} respectively.

Name - Value	
Zin	-1308.32 + 31.5448 j

Table 11: Results for the input impedance

Name - Value	
Zo	0.0942824 + 0.00810883 j
Zoabs	0.0946305

Table 12: Results for the output impedance

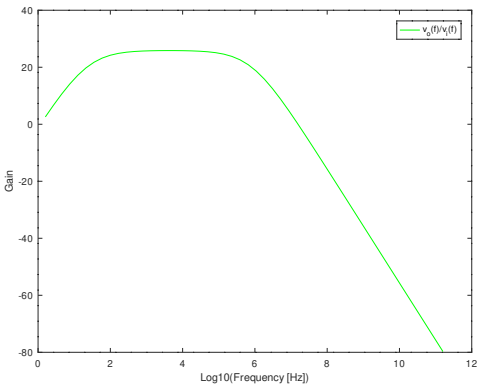
As said theoretically, the load's impedance is equal to 8Ω . The value of Z_{out} should be lower than this value.

Given that the output value of the simulation is higher, this is going to compromise the value of the merit.

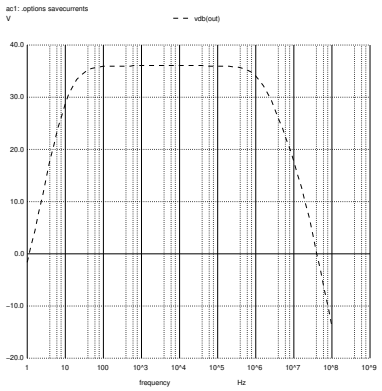
3.4 Comparison

Now that we have established the concepts theoretically and shown the simulation results, we are going to do a comparison between the two approaches (theoretical and simulation) with the chosen values for the constants.

The next graphs show the theoretical and simulation graphs of the gain respectively:



(a) Octave



(b) NgSpice

Figure 9: Output Voltage

The comparison of the shape can only be done on the left side of the graph, because we don't have the theoretical higher cut-off frequency, and therefore there's no point in plotting the theoretical gain any

further than 1e6 Hz. We also should be aware that the theorectical analysis either considers the capacitors open-circuited or short-circuited (this approximation is made when the value of R_E is R_E or 0 in Table 1, respectively).

In the Octave graph we used the medium-value plot, that represents the medium between the circuit when the capacitors are open-circuit and when they are short-circuit, that is consider to be a rough approximation of the real gain. This approach doesn't guarantee a specific value for the gain, however it gives us a region of acceptable gains. In the other hand, as expected, the graph that describes the simulation gain obtained is satisfyingly in this region. The overall shape of the graphs is similar. As it was said previously, whe while using the dominant pole aproximation can't determine what happens to the gain below the lower cutoff frequency and above the higher cutoff frquency. Subsequently, the shape of the gain graph in this regions isn't as accurate as it is below this two frequencies .

The next tables represent both the theoretically and the simulation results, respectivelly.

Name - Value	
VoltageGain	2.593695e+01 dB
HighCutOff frequency	8.304945e+05 Hz
LowCutOff frequency	2.183854e+01 Hz

Table 13: Octave

Name - Value	
V-GaindB	36.0185
CO-higherFreq	1.33158E+06
CO-lowerFreq	18.9035

Table 14: NGspice

Table 15: Results

Name - Value	
ZIn	2.811209e+03 Omega

Table 16: Octave

Name - Value	
Zin	-1308.32 + 31.5448 j
Zinabs	1308.7

Table 17: NGspice

Table 18: $Impedance_{in}$

Name - Value	
ZOut	1.478440e+00 Omega

Table 19: Octave

Name - Value	
Zo	0.0942824 + 0.00810883 j
Zoabs	0.0946305

Table 20: NGspice

Table 21: $Impedance_{out}$

With the values side by side, in a more detailed analysis, of Z_{in}, Z_{out} ,A_V,f_{CO_H} and f_{CO_L} despite the obvious differences, the comparison is satisfatory. When comparing the order of magnitude they are within reasonable intervals of similarity. In fact, the lower cut-off frequencies are really similar, especially when they are plotted in a logscale graph.

3.5 Merit Results

From the results obtained through the Ngspice simulation and considering we used the data shown in table 1, we can compute the merit using the formula given in the lab assignment, represented in the Introduction.

The values of cost and merit are represented in the next table:

Name - Value	
Cost	2292.43
merit	1942.86

Table 22: Cost and Merit

To obtain the best values for the circuit, we've used the matlab simulink to optimize them for the best merit.

4 Conclusion

In this laboratory assignment, the goal especified in the introduction has been achieved with a great merit.
All analyses have been performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. When comparing these last two we conclude that there aren't any disparity between the results and therefore no errors associated. So, we conclude that the architeture that we used can be validated.