TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Instituto Superior Técnico, University of Lisbon

Laboratory Report: Lab Assignment T2, Group 26

April, 2021

Contents

1 Introduction

The aim of this laboratory is to build an AC/DC converter circuit whose input is AC voltage source with a frequency of 50Hz and amplitude 230V.

The circuit chosen for this task is the following:

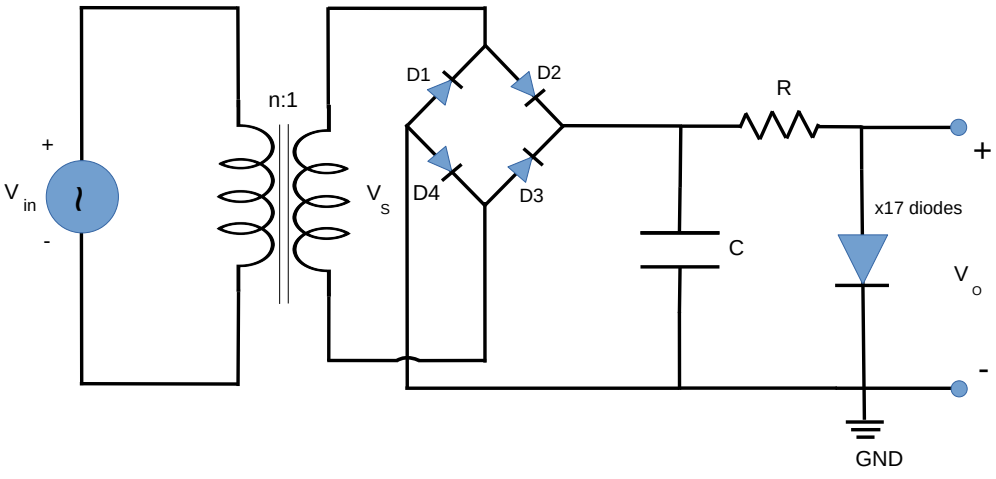

Figure 1: Circuit analysed.

The circuit is composed of several parts. The first one is a transformer with a ratio of 1:n loops with the goal of reducing the input's voltage by a factor of n. Then we can find the remaining parts of the circuit: the envelope detector and the voltage regulator. Following the transformer then is a full-wave bridge rectifier composed of 4 diodes as shown. In addition to the bridge recitfier, in the envelope detector we basically decided to insert only a capacitor with the objective of smoothing the "ripple", which is the residual periodic variation of the DC voltage which has been derived from the AC source. Lastly, in the voltage regulator we have a resistor in series with 18 diodes.

The way the full wave rectifier works is straightforward. The goal is to simply transform a sinusoidal signal that is can assume positive and negative values to only positive values. We will simplify the circuit to a AC voltage source with the bridge rectifier and a load resistor as shown in figure 2 to explain. When the input wave is positive, the route that the current takes is the following.

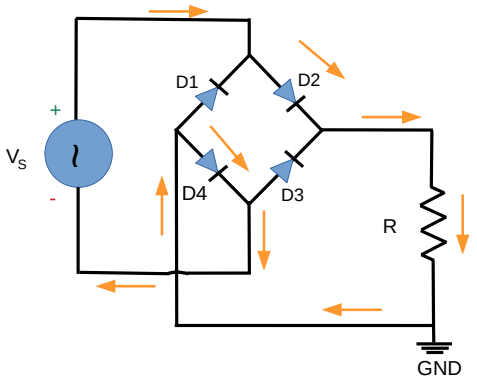

Figure 2: Positive half.

This is because the diode D1 is in reversed biased and therefore current can't pass through it. In the other hand the diode D2 is in forward biased so the current will go that way. After it has passed the resistor, the current goes through the diode D4. The reason it won't go through D1 is because the voltage drop in this diode is negative.

When the input wave is negative, the path taken by the current is the following:

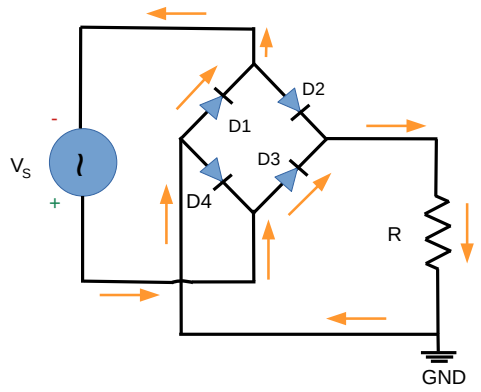

Figure 3: Negative half.

The reasoning behind why the current goes though D3 and D1 is the same as the reason why the current went through D2 and D4 in the positive half of the input wave explained before.

In the end the objective we seeked was fullfilled as can be shown in the figure 4. As we

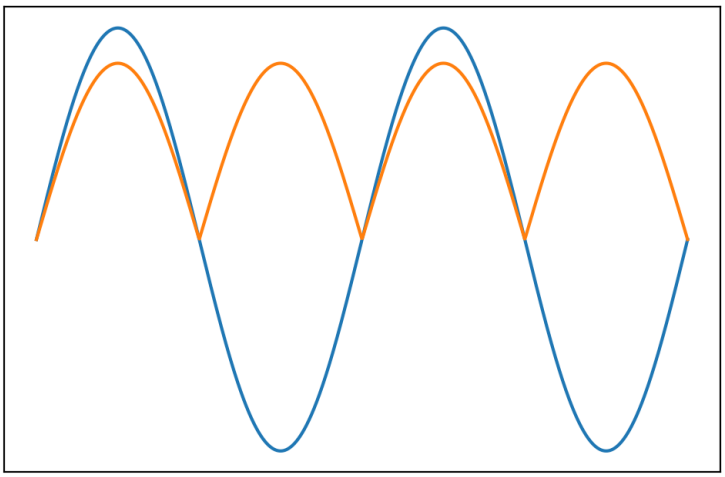

Figure 4: Wave rectified.

can see the voltage signal across the resistor (orange) has only positive values meanwhile the input signal (blue) has both positive and negative values.

The capacitor we've put after the bridge rectifier in the figure 1 allowed us to "smooth" the voltage drop when the signal gets weaker. When the signal is stronger that the voltage limiter(in this case the resistor and diodes) it allows the capacitor to charge so that, when the signal is not strong enough to support the voltage limiter, the capacitor starts to discharge and in consequence the sub circuit containing the capacitor, resistor and diodes will still be active while the rest of the circuit "stops". When the signal gets strong again, the capacitor charges again and this whole process repeats again. As we can see in figure 5 when the signal starts to

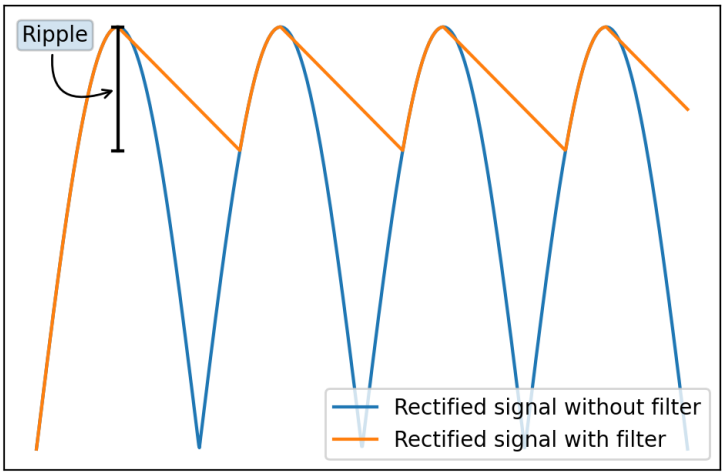

Figure 5: Wave rectified.

drop the capacitor starts to discharge to provide sufficient voltage for the circuit resistor-diode, that is why the slope demonstrate a "ripple" effect.

In section 2 we will give a theotherical analysis of the circuit chosen. Hereinafter, in section 3, we will simulate the same circuit using *Ngspice*. Finally, in section 4, we will compare the theotherical model to the simulation.

2 Theoretical Analysis

In this section, the circuit shown in figure 1 is analysed theoretically.

3 Simulation Analysis

In this section, $ngspice$ results for the circuit shown above are presented. The AC/DC converter was simulated for 10 periods and the default model was used for the diodes.

Since this laboratory assignment consisted of an optimization problem, to start off we used a more elementary model and after verifying it was working properly, modifications were made in order to improve the quality of the circuit. In this particular case, that meant having the smallest output voltage ripple and the smallest cost possible. Also we wanted to have an output voltage average as close as possible to the $12V$ we intended.

3.1 Average output voltage level

In this section we will describe the simulation of the circuit 1. The model for diodes chosen was the default model of *Ngspice*.

Starting off, we used a smaller and simpler circuit that could achieve the goal of the laboratory just to get a grasp of the circuit's behaviour. Later we optimized the circuit with 3 objectives:

- Reduce the cost of resistors, capacitors and diodes;
- Reduce the ripple of the signal;
- Get as close as posible to an average voltage of 12V.

Keeping that in mind, we immediately knew that using a full wave rectifer opposed to a half wave was very much worth, given that the monetary cost of the diodes was low and the ripple impact using the full wave was massive. The capacitance, resistance value and number of diodes were achieved by trial and error, trying to minimize the ripple and $|V_o - 12|V$ given the total cost.

Moreover, the functions used to calculate the average value, maximum and minimum (these last two to calculate the ripple) were respectively: AVG, MAX and MIN.

Big gráficos ahead: (não esquecer de mostrar o cálculo do mérito(?))
:)))))))))))))))

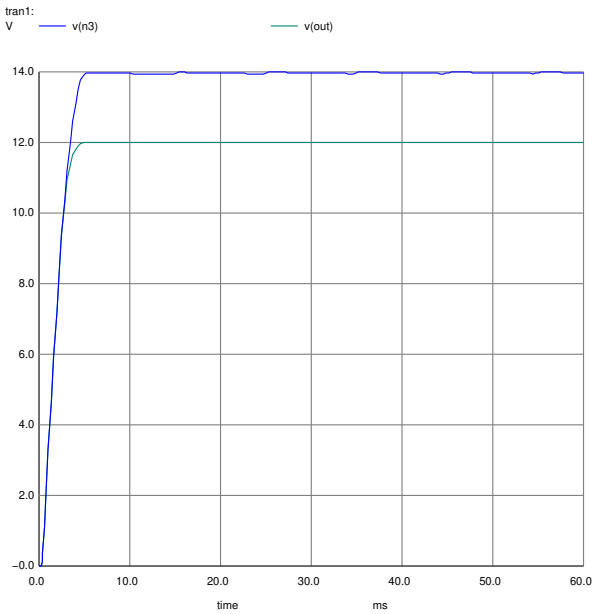

Figure 6: Negative half.

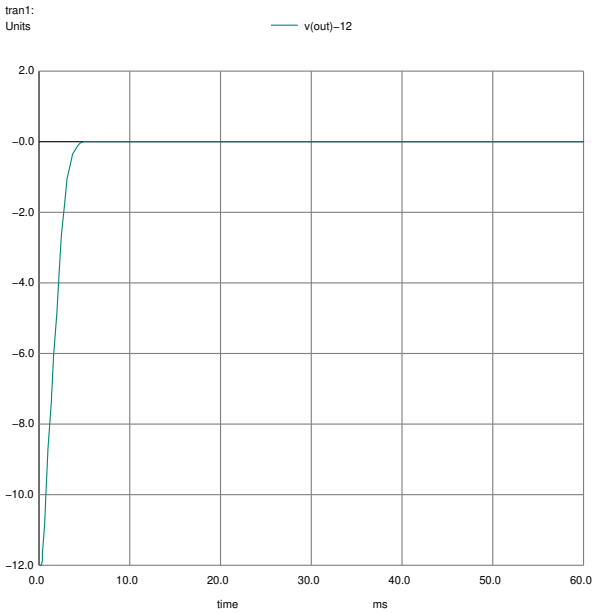

Figure 7: Negative half.

4 Conclusion

In this laboratory assignment, the objective of analysing the circuit presented in figure 1 has been achieved. The analysis was performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. The simulation results matched the theoretical results precisely. The reason for this perfect match is the fact that this is a straightforward circuit containing only linear components, so the theoretical and simulation models cannot differ. For more complex components, the theoretical and simulation models could differ, but this is not the case in this work.

References

[1] Phyllis R. Nelson. *Introduction to* spice *source files*.
`https://www.cpp.edu/ ~ prnelson/courses/ece220/220-spice-notes.pdf`

[2] John W. Eaton, David Bateman, Søren Hauberg, Rik Wehbring. *GNU Octave - Free Your Numbers*.
`https://octave.org/octave.pdf`

[3] LibreOffice Documentation Team. *Getting Started Guide*.
`https://documentation.libreoffice.org/assets/Uploads/Documentation/en/GS7.0/GS70-GettingStarted.pdf`

[4] Mesh analysis and node analysis notes. *Princípios fundamentais na análise de circuitos electrónicos*.
`https://moodle.fct.unl.pt/pluginfile.php/167552/mod_resource/content/0/NotasTecnicas/Apontamento_tecnico_3_ebf.pdf`

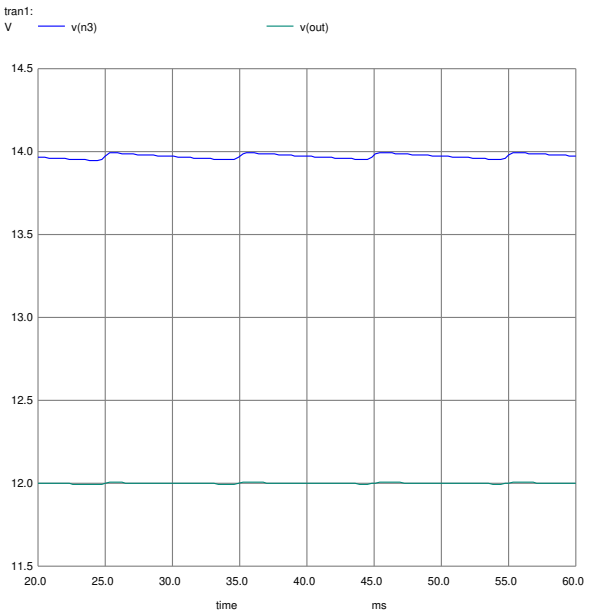

Figure 8: Negative half.

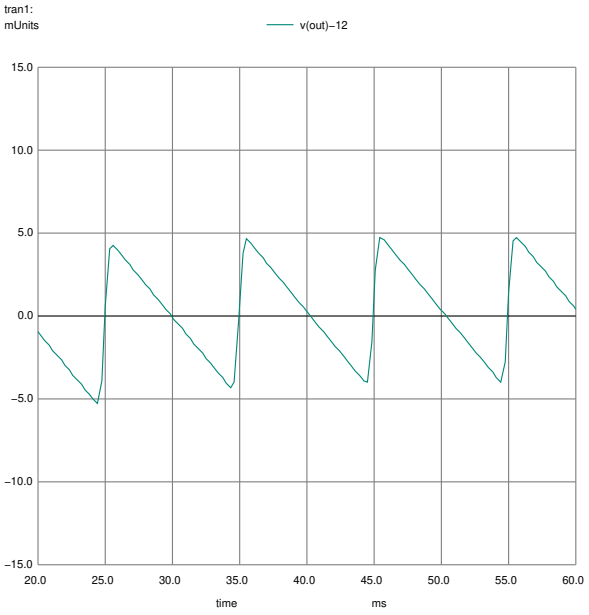

Figure 9: Negative half.