TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

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Laboratory Report: Lab Assignment T4, Group 26

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Contents

1 Introduction

The aim of this laboratory assignment is to build an audio amplifier with the goal of maximizing the gain and bandwidth and minimizing the total cost and the value of lower cut-off frequency. The circuit designed has two distinct parts: the gain stage and the output stage as shown in figure 1.

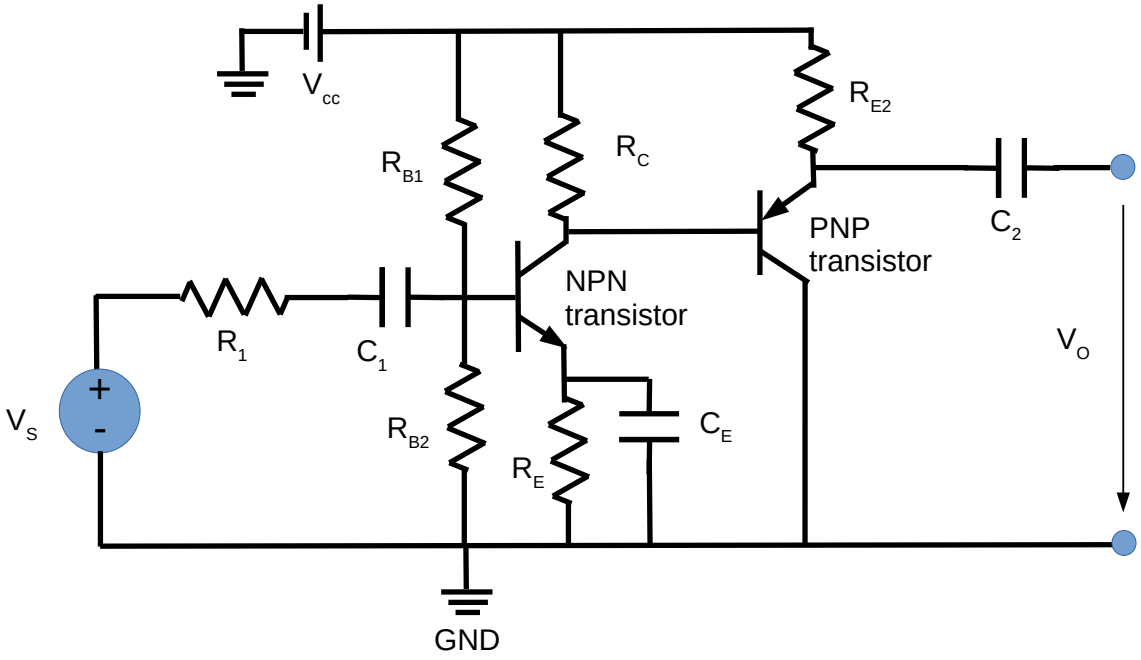

Figure 1: Circuit analysed.

The input (V_s) is a sinusoidal signal with a maximum amplitude of 10mV with an internal impendance of 100 Ω, represented by R_{in}. On the other end of the circuit we can find an 8 Ω speaker. Additionally, the circuit is supplied by a 12V DC source, V_{cc}, that garantees that the transistor operates in its forward-active region (Base Biasing).

The gain stage mentioned, which is connected to the input signal, is formed by a single stage common-emitter amplifier with degeneration that uses a NPN transistor. Furthermore, there is a bias circuit and a bypass capacitor which functions will be discussed later in the report. Moving on to the output stage, it was used a common collector amplifier but this time a PNP transistor was used. This stage is basically responsible for lowering the output impendace that comes from the previous stage, so that the values are appropriate for the speaker.

Now we will talk about the goal of the coupling capacitors (C_1 and C_2), bypass capacitors (C_3) and the effect of the resistance R_C.

Starting with the C_1 and C_2, they are low impendance coupling capacitors and DC blocking capacitors whose reactance at the signal frequency is designed to be negligible. The AC coupling through capacitors is used to inject AC input signal and extract output signal without disturbing the Q-point (steady-state voltage or current at a specified terminal of an active device with no input signal applied.) For this reason they have a direct impact on the lower and upper 3dB cut off frequencies and therefore the bandwidth of the network.

At low frequencies the reactance of coupling capacitor C2 is relatively high and hence very small part of the signal will pass from the amplifier stage to the load. At high frequencies the reactance of coupling capacitor C2 is very small and it behaves as a short circuit. This increases the loading effect of the amplifier stage and serves to reduce the voltage gain. At mid

frequencies the voltage gain of the amplifier is constant. The effect of the coupling capacitor C2 in this frequency range is such as to maintain a constant voltage gain. Thus, as the frequency increases in this range, the reactance of C2 decreases, which tends to increase the gain. If it is not used, then the amplified AC signal following through R_E will cause a voltage drop across it, thereby dropping the output voltage.

C_3 is a bypass capacitor that provides a low impendace path for the AC current from emitter to ground, thereby removing R_E (required for good Q-point stability) from the circuit when AC signals are considered which garantees that the resistor will not affect the gain.

In Section 3, a theoretical analysis of the circuit is performed, followed by an simulation in 2 with the goal of comparing and understand better the behaviour of this circuit.

2 Simulation Analysis

In this section we shall describe the simulation of the circuit presented in figure 1. The models used for the npn and pnp transistors shown in figure 1 are, respectively, the BC557A and the BC547A, both Philips' products. As far as the actual simulation is concerned, firstly we did a transient analysis in order to study the output of the circuit and so we could check whether or not the output had any visible distortion. Having confirmed the abscence of said distortion, we decided to print out the values of the voltages in the transistors so we could verify that they were, in fact, in the forward active region (F.A.R). These values are presented in the following tables.

Name	**Value [V]**
vcedc	6.807931e+00
vbedc	7.074442e-01

Table 1: Ngspice's npn transistor voltages.

Name	**Value [V]**
vecdc	8.296052e+00
vebdc	5.927437e-01

Table 2: Ngspice's pnp transistor voltages.

As can be seen, the transistors are indeed in the F.A.R, as $V_{CE} > V_{BE}$, for the npn transistor, and $V_{EC} > V_{EB}$, for the pnp transistor. We can also see that $V_{BE} \approx V_{EB} \approx 0.7\,V$. This value $(0.7\,V)$ is often used as an estimate of both V_{BE} and V_{EB}, for theoretical analysis, as it simplifies the calculations. We too shall use this approximation in the next section.

After this, we moved on to the frequency analysis. Before anything else, we decided to compute both the input and output impedances of the circuit used, as they are critical for understanding the behaviour of the circuit. The results obtained are shown in the tables below.

Name	**Value [$k\Omega$]**
zi	5.913131e-01,-7.52338e-02
abszi	5.960799e-01

Table 3: Ngspice's input impedance.

Name	**Value [Ω]**
zo	4.612861e+00 , 1.906177e-01
abszo	4.616798e+00

Table 4: Ngspice's output impedance.

In the first line of both tables, the impedance is presented in its complex form (first number refers to the real part, second refers to the imaginary part). The second line of both tables contains the impedances' absolute value. A good amplifier is one that has a high input impedance, so that the input signal isn't degredated, a low output impedance, which makes it so that the output signal, which is delivered to the load, isn't degredated as well, and a high gain. As we can see from the table above, the output impedance of our simulated amplifier is indeed low. The input impedance however, although much greater than the output impedance, could still be higher. Nevertheless, we figured the results were good enough despite this fact, so we didn't bother trying to increase the input impedance any further. We would also like to point out that, in order to compute the output impedance, we had to utilize a different *ngspice* script, in which we switched off the input voltage source, V_S, in figure 1, and connected a test voltage source to the output of the citcuit, instead of the load. The output impedance is then given by the quotient of this test voltage by the current flowing through the test voltage itself.

Following the previous frequency analysis, we obtained the graph shown in figure 2, for the gain in dB.

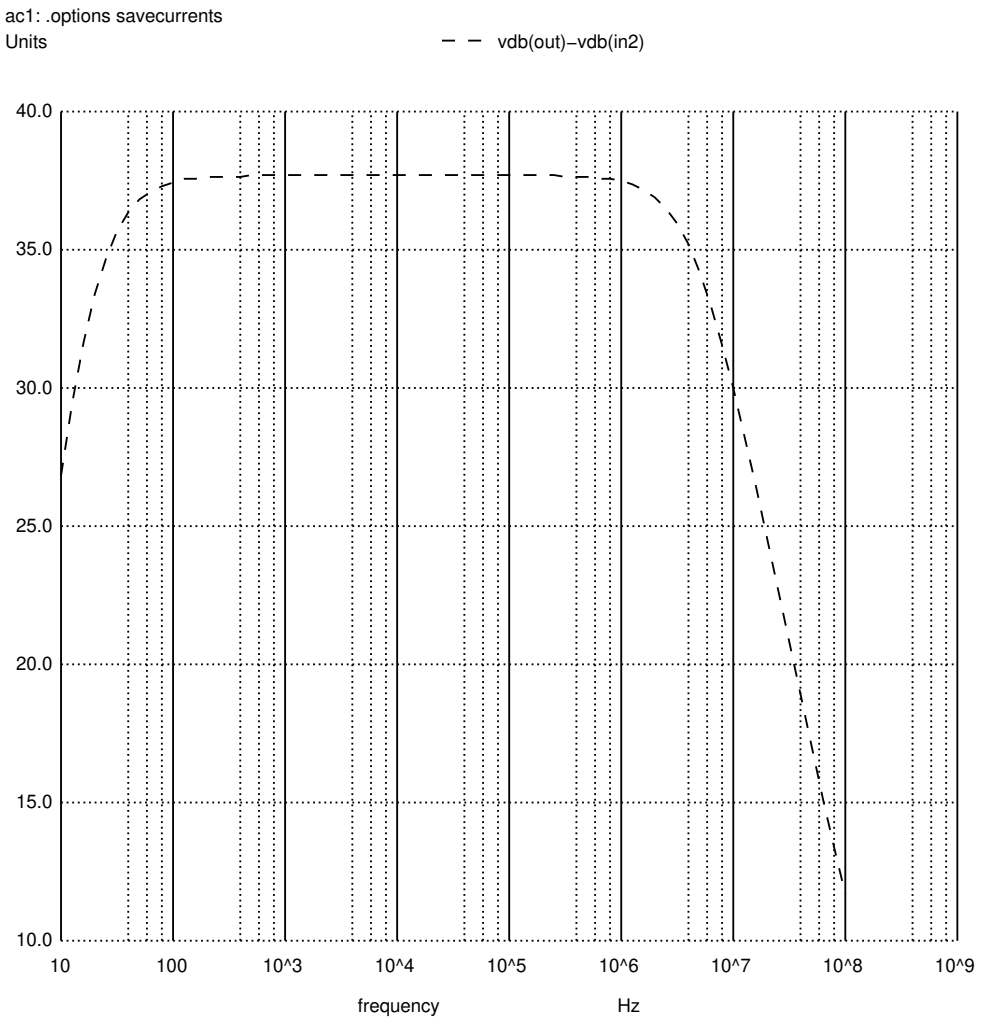

Figure 2: Ngspice gain in dB.

Utilizing this graph, we were able to compute the maximum gain of the amplifier. The lower and upper cut-off frequencies, as well as the bandwidth of the amplifier, were calculated using the output signal. The values obtained are presented in the following tables.

Name	Value [Hz]
lowercutoff	2.330909e+01
uppercutoff	2.849908e+06
bandwidth	2.849885e+06

Table 5: Ngspice's cut-off frequencies and bandwidth.

Name	Value [dB or -]
gaindbmax	3.768241e+01
lingain	7.658091e+01

Table 6: Ngspice's gain.

As we can see, the simulated amplifier has a lower cut-off frequency close to $20\ Hz$, which is really good, provided that the human ear cannot detect sounds below the $20\ Hz$ mark. This also means that we are not wasting any part of the bandwidth, given that the upper cut-off frequency is way above the limit of $20\ kHz$, which is the maximum frequency the human ear can detect. With that said, one can make the argument that we cannot hear sounds higher than $20\ kHz$ and, as such, we really are wasting part of the bandwidth. However, it turned out the upper cut-off frequency was generally very high, much higher than $20\ kHz$, regardless of the amplifier's specs. So, since there is not much we can do about that, we instead focus on the minimization of the lower cut-off frequency.

Lastly, we obtained a gain of 37.68241 dB (76.58091 in a linear scale), which seems high enough.

Utilizing these results, we were able to compute the merit of our work, making use of the following formula.

$$M = \frac{voltageGain \times bandwidth}{cost \times lowercutoffFreq} \tag{1}$$

The result is presented in the table below, in which we also show the cost of our circuit.

Name	**Value [MU or -]**
cost	4.351008e+03
merit	2.151952e+03

Table 7: Cost and merit using Ngspice's results.

The cost was computed using the following scheme.

- Resistors $\rightarrow$ 1 MU per kΩ;
- Capacitors $\rightarrow$ 1 MU per μF;
- Transistors $\rightarrow$ 0.1 MU per Transistor.

3 Theoretical Analysis

In this part we will discuss the theoretical analysis of the circuit shown in 1. In order to do that we will have to do both DC and AC analysis.

For the DC analysis, we can analyse both stages separatly, so we can do the following:

- Find the DC equivalent circuit by replacing all capacitors by open circuits;
- Find Q-point from DC equivalent circuit by using appropriate transistor model.

For the AC analysis:

- Find AC equivalent circuit by replacing all capacitors by short circuits and DC voltage sources by ground connections;
- Replace transistor by its hybrid Π model;
- Use small-signal AC equivalent to analyze AC characteristics of amplifier.

In the end, we just need to combine the end results of DC and AC analysis to yield the total voltages and currents in the network.

With this being said, let's start by the DC analysis of the gain stage and output stage, which can be done separately.

3.1 DC analysis

3.1.1 Gain stage

Replacing all capacitors with open circuits leaves us with the circuit shown in figure 3.

Replacing all connections to the transistor with their Thévenin equivalents gives the circuit presentend in figure 4, and applying KVL to the transistor yields the following expression:

$$V_{eq} - I_B R_{eq} - V_{BE} - I_E R_E = 0 \tag{2}$$

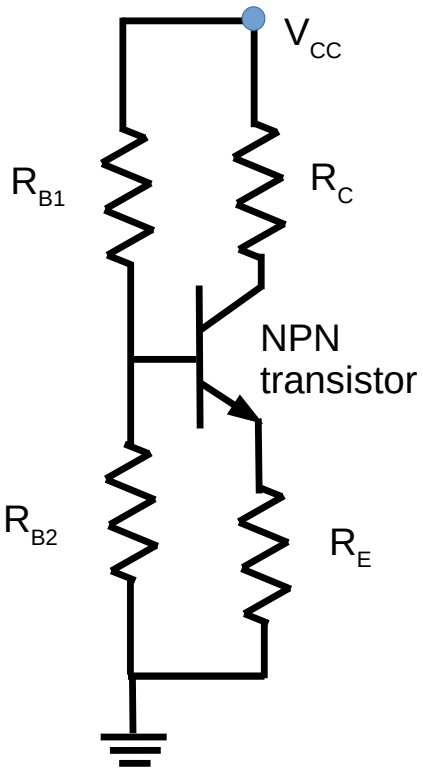

Figure 3: Gain stage OP computation.

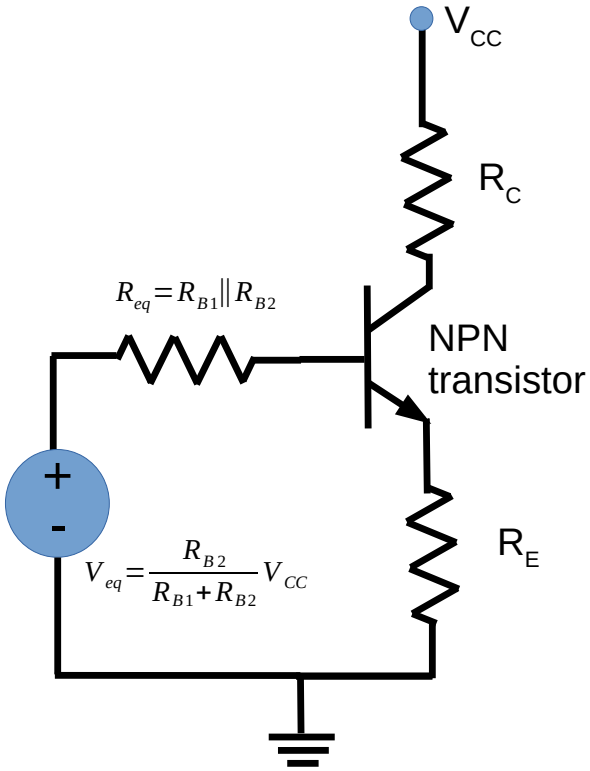

Figure 4: Thévenin equivalent.

Applying KCL to the transistor:

$$I_E = I_B + I_C \tag{3}$$

Because $I_C = \beta \times I_B$:

$$I_E = I_B\,(1 + \beta) \tag{4}$$

Substituting for I_E in the loop equation:

$$V_{eq} - I_B Req - V_{BE} - I_B\,(1 + \beta)\,R_E = 0 \tag{5}$$

We can assume $V_{BE} \approx 0.7V$ (the usual potencial barrier). With further development of these equations, we can get all the voltages and current values we need, mainly the current through the collector, to use in the AC analysis, and the voltage drop between collector and emitter, to check if the transistor is in the forward active region and to compare the theoretical with the simulation results. These results are shown in table 8.

Name	Value [A or V]
IC	0.008943
VCE	6.629261

Table 8: Current through collector and the voltage drop between collector and emitter.

As we can see $V_{CE} > V_{BE} = V_{BE_{ON}}$, so we know that the transistor is in the forward active region.

3.1.2 Output stage

For the Output stage, the analysed circuit is shown in figure 5.

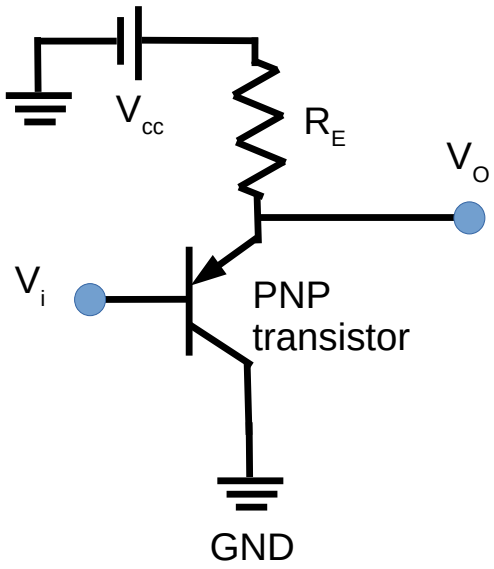

Figure 5: Output stage (DC analysis).

We assume that $V_{EB} \approx 0.7V$. Applying KVL to all meshes and knowing that the voltage V_I is equal to the output of the gain stage we get:

$$I_E = \frac{V_{CC} - V_{EB} - V_I}{R_E} \tag{6}$$

$$V_O = V_{cc} - R_E I_E \tag{7}$$

$$V_O = V_I + V_{BE} \tag{8}$$

Once again, with further development of these equations, we can get the same currents and voltages as for the gain stage, as shown in table 9.

Name	Value [A or V]
IC	0.037549
VEC	8.228555

Table 9: Current through collector and the voltage drop between emitter and collector.

As we can see $V_{EC} > V_{EB} = V_{EB_{ON}}$, so we know that the transistor is in the forward active region.

3.2 AC analysis

With the operating point analysis done, we can now replace the capacitors with short circuits and start the AC analysis, using incremental analysis. In this subsection, we have only considered the incremental analysis for medium frequencies, and that is why it is possible to replace the capacitors with short circuits. In addition, all the DC-only sources can be replaced with short circuits, too, and the transistors can be replaced with the corresponding incremental model. We first studied the gain stage and the output stage independently.

3.2.1 Gain stage

The resulting circuit can be simplified to:

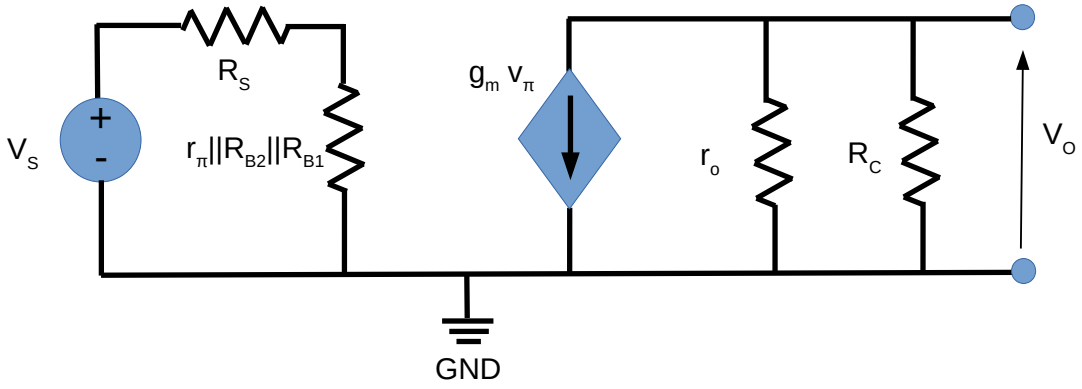

Figure 6: Gain stage AC analysis - incremental circuit.

As we derived in the theotherical classes we have that:

$$\begin{cases} \frac{v_o}{v_i} = -g_m \left(R_c \| R_0\right) v_\pi \\ v_\pi = \frac{r_\pi \| R_{B1} \| R_{B2}}{R_s + r_\pi \| R_{B1} \| R_{B2}} \end{cases} \tag{9}$$

$$\Rightarrow \frac{v_o}{v_i} = -g_m \left(R_c \| R_0\right) \frac{r_\pi \| R_{B1} \| R_{B2}}{R_s + r_\pi \| R_{B1} \| R_{B2}} \tag{10}$$

For the input and output impendances we have:

$$\begin{cases} Z_I = R_{B1} \| R_{B2} \| r_\pi \\ Z_0 = R_c \| r_O \end{cases} \tag{11}$$

The results are presented in table 10.

Name	Value [- or Ω]
AV1	-139.316657
ZI1	484.433630
ZO1	469.857366

Table 10: Gain and impedances.

3.2.2 Output stage

The resulting circuit can be simplified to:

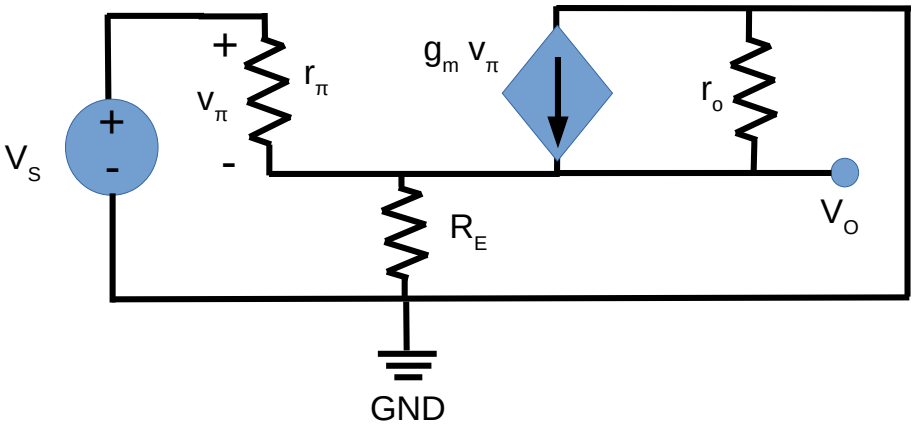

Figure 7: Output stage AC analysis - incremental circuit.

Relative to the output stage we got:

$$\frac{v_0}{v_i} = \frac{g_m}{g_\pi + g_E + g_o + g_m} \tag{12}$$

$$Z_I = \frac{g_\pi + g_E + g_o + g_m}{g_\pi \left(g_\pi + g_E + g_o\right)} \tag{13}$$

$$Z_o = \frac{1}{g_\pi + g_E + g_o + g_m} \tag{14}$$

The results are presented in table 11.

Name	**Value [- or Ω]**
AV2	0.988407
ZI2	13053.450802
ZO2	0.658073

Table 11: Gain and impedances.

As we can see the gain stage output impedance and the output stage input impedance are quite compatible and that garantees that they can be connected without significant signal loss.

3.3 Frequency response

Now we will calculate the frequency response $\frac{V_o(f)}{V_I(f)}$. For this, we need the total incremental circuit, as shown below:

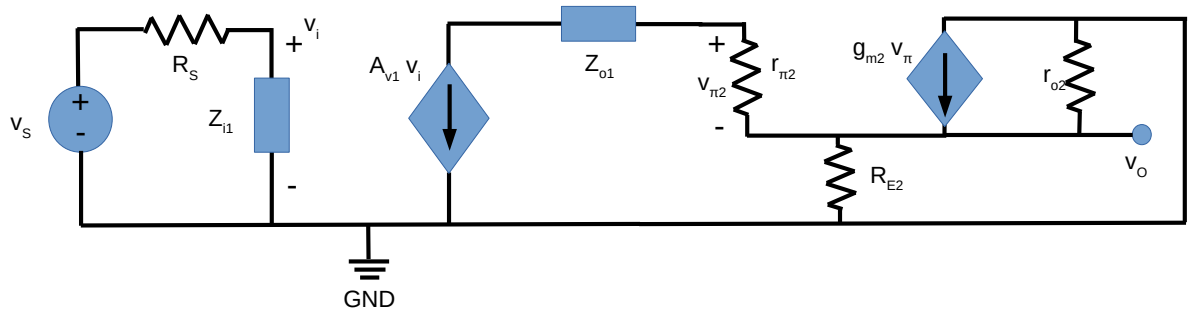

Figure 8: Complete circuit.

The gain was only calculated for medium frequencies, so we end up considering the frequency response as a constant value (equivalent to saying that the cut off frequencies are 0 and ∞). The gain was calculated using the following expression:

$$\frac{vo}{vi} = \frac{\frac{1}{r_{\pi_2}+Z_{o1}} + \frac{g_{m2}r_{\pi 2}}{r_{\pi_2}+Z_{o1}}}{\frac{1}{r_{\pi_2}+Z_{o1}} + \frac{1}{R_{E2}} + \frac{1}{r_{o2}} + \frac{g_{m2}r_{\pi 2}}{r_{\pi_2}+Z_{o1}}} A_{v1} \tag{15}$$

where A_{v1} is the gained obtained for the gain stage. In the following graphic we present the frequency response, ranging from $10Hz$ to $100Mhz$, in logarithmic scale and with 10 points per decade.

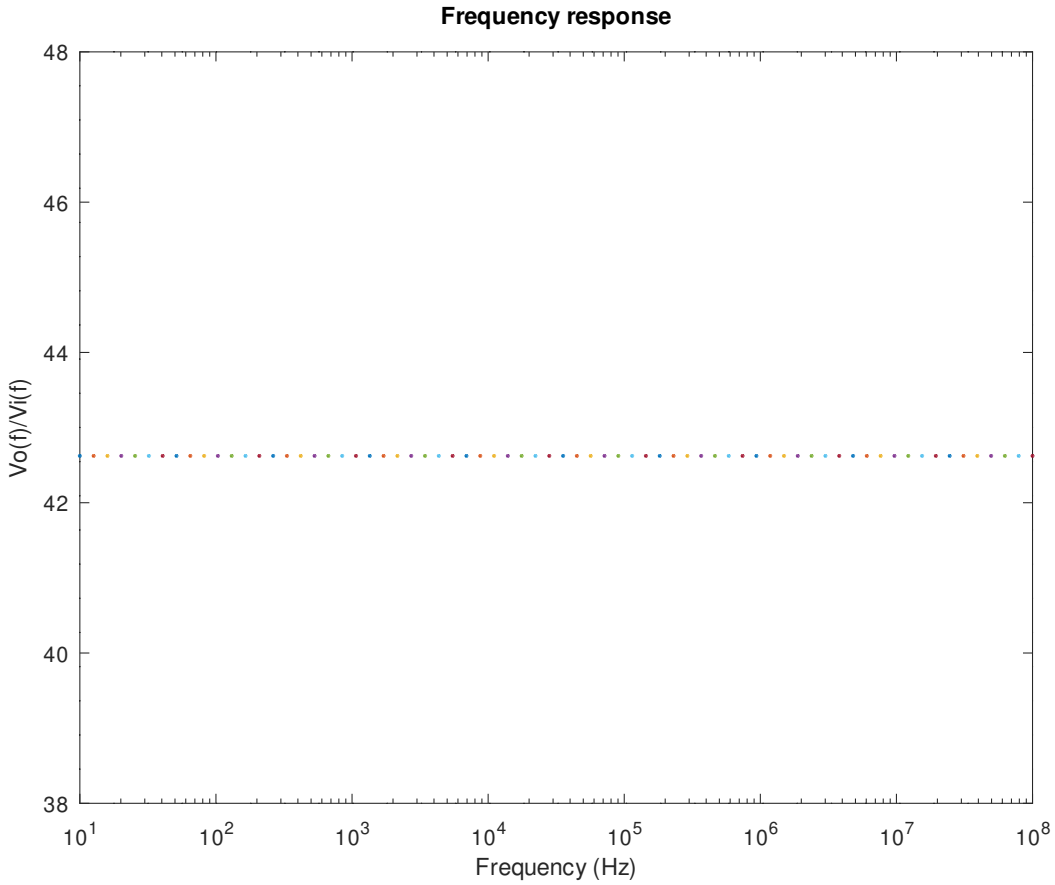

Figure 9: Theoretical gain.

4 Comparison

As one may notice, there are a few differences when comparing *Ngspice*'s and *Octave*'s results. But this is somewhat normal since the models used in the theoretical analysis are approximations of non linear components that are the transistors. Moreover, the Hybrid Π model used was not the full one, so we did not take into account the Miller effect and complete Early Effect that occurs in this type of network. Despite this, the results are quite satisfactory.

5 Conclusion

In this laboratory assignment, the objective of analysing the circuit presented in figure 1 has been achieved. The analysis was performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. Although the theoretical results differed slightly from the simulation results we did achieve good results overall. The reason for this slight mismatch is the fact that the model for the transistors in both were different, being the theoretical a simpler of the two. In the end, we think that the goal of this laboratory was achieved. The building and optimization of the circuit allowed us to further reflect about the behaviour of transistors and their relationship with the other components already studied.

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