TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

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Laboratory Report: Lab Assignment T5, Group 26

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Contents

1 Introduction

In this laboratory assignment, our aim was to design a band-pass filter (BPF) with a central frequency, defined as the geometric mean of the lower and upper cut-off frequencies, of 1 kHz and a gain at the central frequency of 40 dB. For the design, the material available for use was as follows:

- One 741 OP-AMP
- At most three 1kΩ resistors
- At most three 10kΩ resistors
- At most three 100kΩ resistors
- At most three 220nF capacitors
- At most three 1μF capacitors

With this in mind, the circuit we chose to use for this report was the following:

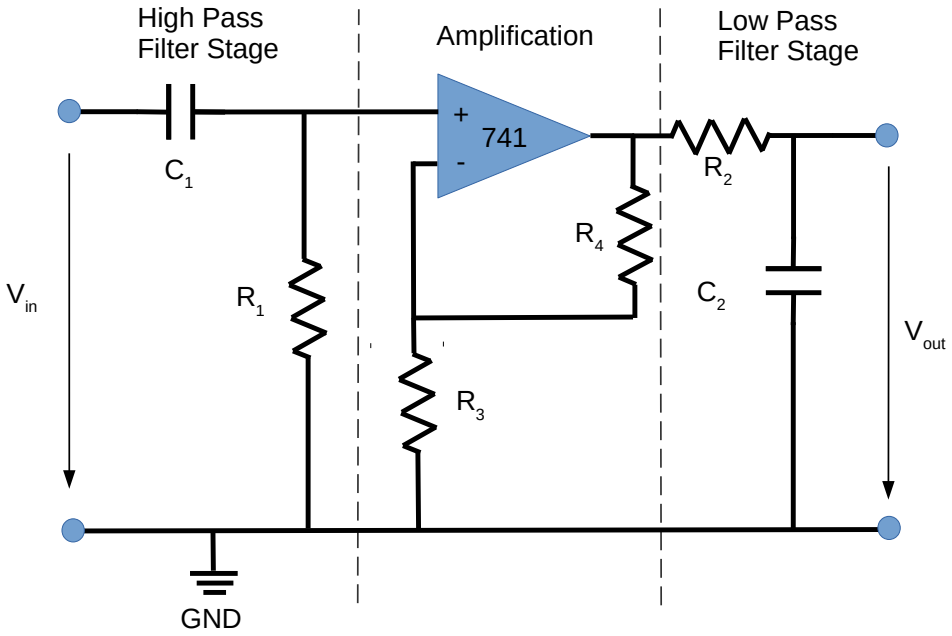

Figure 1: Band-pass filter circuit.

Basically the circuit consists of 3 stages: high pass filter, amplification and low pass filter in this exact order. The first stage consists simply of a passive filter which attenuates low frequencies and lets through high frequency signals. It is then followed by a non-inverting amplifier as shown. Finally, to cut the highest frequencies, a passive RC filter was used, which together with the previous high pass filter produces the desired BPF.

In section 2, using *Ngspice*'s capabilities, we improve the circuit by optimizing the values of the resistors and capacitors and simulate the circuit in question. Later, in section 3 we carry out a theoretical analysis where we calculate the transfer function, input and output impedances and the cut-off frequencies. Next we compare the results obtained in both analyses and briefly discuss their possible similarities and differences in section 4. Finally, in section 5 we present our final thoughts regarding the work developed.

2 Simulation Analysis

In this section we shall describe the simulation of the circuit presented in figure 1. This circuit was translated into *ngspice* source code and simulated as follows. Firstly, we did transient analysis in order to study the output of the circuit and so we could check whether or not it had any visible distortion. Having confirmed the abscence of said distortion, we proceeded to the frequency analysis, the main focus of this lab assignment. As such, we decided to compute both the input and output impedances of the circuit used, as they are critical for understanding the behaviour of the circuit. The results obtained are shown in the table below. Keep in mind that these values were calculated at the central frequency, which we shall present later in the analysis.

Name	Value [Ω]
abszinatfc	1.440293e+03
abszoatfc	7.235581e+02

Table 1: *Ngspice*'s input and output impedances' absolute values.

The first and second lines of the table contain, respectively, the input and output impedances' absolute values. Generally, when designing a circuit such as this one, we want it to have a high input impedance, so that the input signal isn't degredated, and a low output impedance, which makes it so that the output signal, which is delivered to the load, isn't degredated as well. As we can see from the table above, the values obtained are far from ideal. The input impedance is far from infinite and the output impedance is also distant from zero. Nevertheless, we figured the results were good enough despite this fact, so we didn't bother trying to increase the input impedance nor decrease the output impedance any further. However, this is a fact that still needs to be kept in mind if we inted to connect this circuit to other circuits. We would also like to point out that, in order to compute the output impedance, we had to utilize a different *ngspice* script, in which we switched off the input voltage source, V_{in} , in figure 1, and connected a test voltage source to the output of the citcuit. The output impedance is then given by the quotient of this test voltage by the current flowing through the test voltage itself. Following the previous frequency analysis, we obtained the graph shown in figure 2, for the gain in dB, and the graph shown in figure 3, for the phase of the gain.

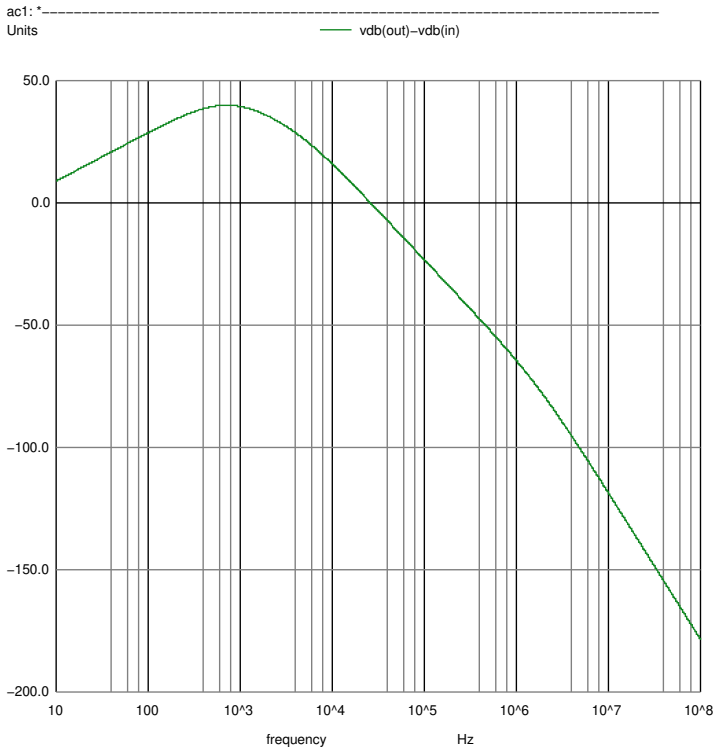

Figure 2: *Ngspice* gain in dB.

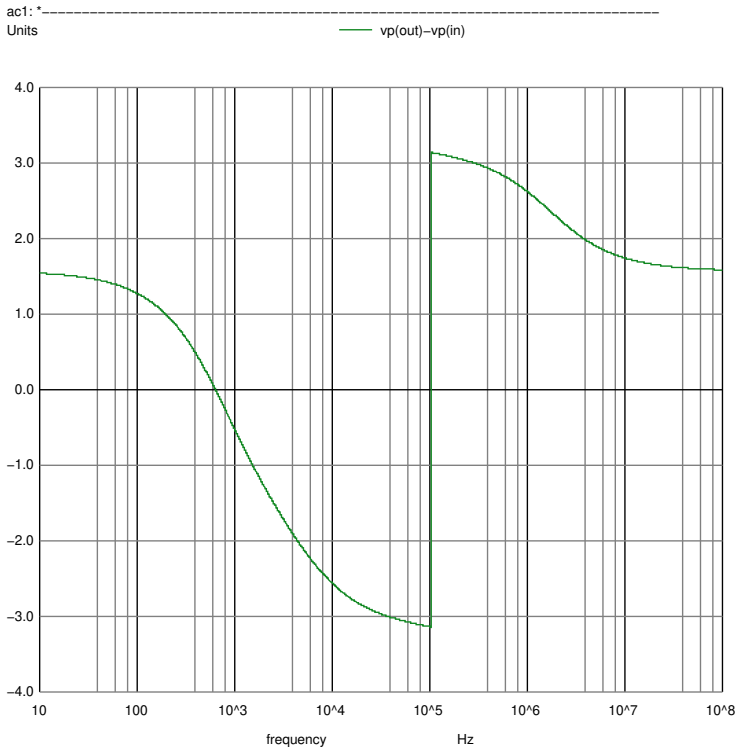

Figure 3: *Ngspice* gain's phase.

Utilizing the graph shown in figure 2, we were able to compute the maximum gain of the circuit, the lower and upper cut-off frequencies, as well as the central frequency, defined as the geometric mean of the lower and upper cut-off frequencies. The values obtained are presented in the following tables.

Name	Value [Hz]
lowercutoff	2.973792e+02
uppercutoff	1.638347e+03
fc	6.980045e+02

Table 2: *Ngspice*'s cut-off frequencies and central frequency.

Name	Value [dB or -]
gaindb	3.997001e+01
lineargain	9.965532e+01

Table 3: *Ngspice*'s gain in dB and linear gain.

In designing this filter circuit we didn't really worry about its bandwidth as it wasn't necessary for what we wanted to achieve. Instead, we focused on its gain, as well as its central frequency. We managed to achieve a gain which was really close to 40 dB, as was intended. The central frequency, however, is relatively far away from the intended 1 kHz. Given the restrictions imposed by the professor in terms of available components, we had some trouble getting both the gain and central frequency to match the intended values. As such we decided to prioritize the gain of the filter circuit and in doing such ended up sacrificing the central frequency. In hindsight, we realized this wasn't the most ideal, as our circuit was supposed to be a filter circuit, which means we should have focused on its central frequency instead.

Anyways, moving on, utilizing these results we were able to compute the merit of our work, making use of the following formula.

$$M = \frac{1}{\text{Cost} \times (\text{voltage gain deviation} + \text{central frequency deviation} + 10^{-6})} \tag{1}$$

The result is presented in the table below, in which we also show the cost of our circuit.

Name	**Value [MU or -]**
cost	1.352673e+04
merit	2.445183e-07

Table 4: Cost and merit using *Ngspice*'s results.

The cost was computed using the following scheme.

- Resistors $\rightarrow$ 1 MU per kΩ;
- Capacitors $\rightarrow$ 1 MU per μF;
- Transistors $\rightarrow$ 0.1 MU per Transistor;
- Diode $\rightarrow$ 0.1 MU per Diode (used in OP-AMP).

3 Theoretical Analysis

In this part we will discuss the theoretical analysis of the circuit shown in figure 1. The values used for R_1, C_1, R_2, C_2, R_3 and R_4 are the same as the ones used in *Ngspice*, so it is easier to compare both analyses. Even though we could do the calculations with the actual model presented in figure 1, we decided to use the incremental model presented in figure 4, below, since it makes calculations easier.

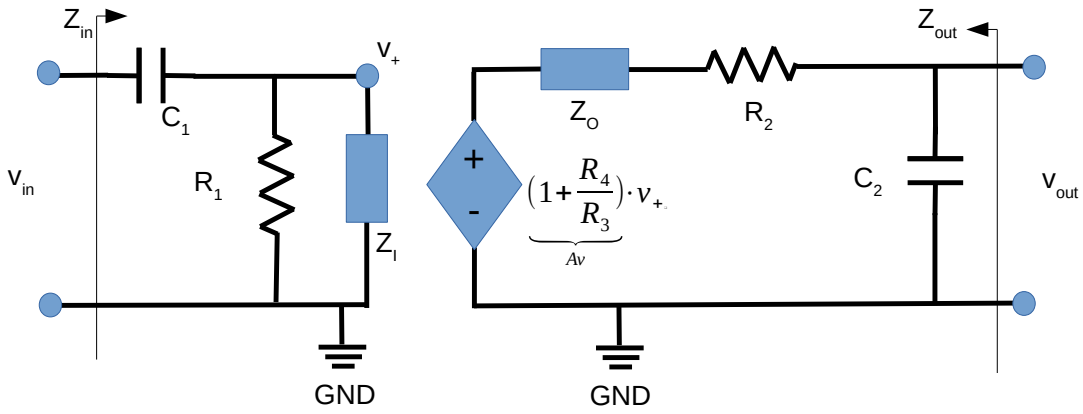

Figure 4: Band-pass filter incremental circuit.

The gain associated with the dependent voltage source is given by $1+\frac{R_4}{R_3}$, since the amplifier subcircuit corresponds to a non-inverting amplifier.

The OP-AMP is considered to be ideal, so $Z_I = \infty$ (behaves like an open circuit) and $Z_O = 0$ (behaves like a short circuit). Additionally, it is know that $v_+ = v_-$ (would be needed if we did not use the incremental model). This way, we can determine the expression for the gain using only the two voltage divider relations below:

$$v_+ = \frac{R_1}{R_1 + Z_{C_1}} v_{in} \tag{2}$$

$$v_{out} = \frac{Z_{C_2}}{Z_{C_2} + R_2} v_+ A_v = (\frac{Z_{C_2}}{Z_{C_2} + R_2})(\frac{R_1}{R_1 + Z_{C_1}})(1 + \frac{R_4}{R_3}) v_{in} \tag{3}$$

where $Z_{C_1} = \frac{1}{j\omega C_1}$ and $Z_{C_2} = \frac{1}{j\omega C_2}$. This way the gain is given by equation 4:

$$\frac{v_{out}}{v_{in}} = (\frac{Z_{C_2}}{Z_{C_2} + R_2})(\frac{R_1}{R_1 + Z_{C_1}})(1 + \frac{R_4}{R_3}) \tag{4}$$

Computing the absolute value of the gain (in dB), for a frequency vector in log scale with 10 points per decade, from 10 Hz to 100 MHz, we obtained the graphic in figure 5. Computing the phase we obtained the graphic in figure 6.

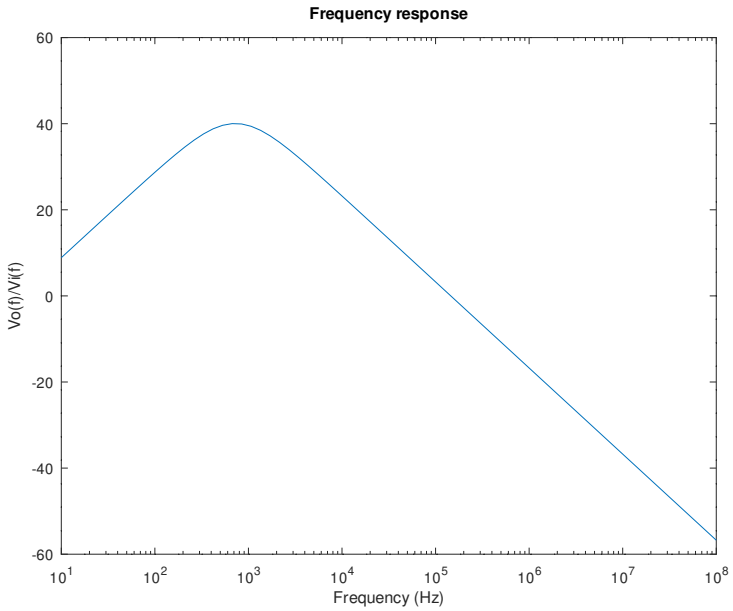

Figure 5: *Octave* gain in dB.

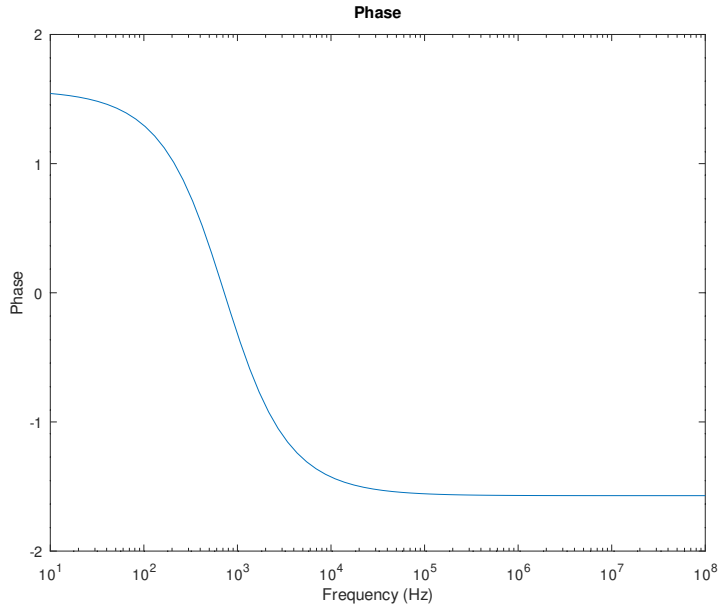

Figure 6: *Octave* gain's phase.

Since we know that the cut-off frequencies correspond to a gain 3 dB lower than the maximum gain, we were able to find the lower cut-off frequency, f_L, and the upper cut-off frequency, f_H. The central frequency, f_c, is then given by the geometric mean of the two cut-off frequencies, given by equation 5:

$$f_c = \sqrt{f_L \times f_H} \tag{5}$$

The values for f_L, f_H and f_c, as well as the gain at the central frequency, are shown in tables 5 and 6.

Name	Value [Hz]
lowercutoff	300.161057
uppercutoff	1743.457911
fc	723.407333

Table 5: *Octave*'s cut-off frequencies and central frequency.

Name	Value [dB or -]
gain(dB)	40.043765
gain(linear)	100.505129

Table 6: *Octave*'s gain in dB and linear gain.

Finally, we calculated the input and output impedances of the circuit at the central frequency.

For the input impedance, Z_{in}, we considered an output load $Z_L = \infty$, and an input voltage source with the central frequency. Since $Z_I = \infty$ and behaves like an open circuit, Z_{in} is simply given by the impedances of C_1 and R_1 in series, as in equation 6:

$$Z_{in} = R_1 + Z_{C_1} \tag{6}$$

For the output impedance, Z_{out}, we considered a null input voltage and an output voltage source with the central frequency. Since there is no input voltage, $v_+ = 0$, as we can confirm using the voltage divider (equation (2)), and consequently the dependent voltage source acts like a short circuit. This way, since $Z_O = 0$, Z_{out} is simply given by the impedances of C_2 and R_2 in parallel, as in equation 7:

$$Z_{out} = \frac{R_2 Z_{C_2}}{R_2 + Z_{C_2}} \tag{7}$$

Z_{in} and Z_{out} are computed at the central frequency. The results are shown in table 7.

Name	Value [Ω]
Z_{in}	1414.237243
Z_{out}	707.118621

Table 7: *Octave*'s input and output impedances' absolute values.

4 Comparison

In this section we present *Ngspice*'s and *Octave*'s results side by side, so it is easier to compare the two.

4.1 Gain plots

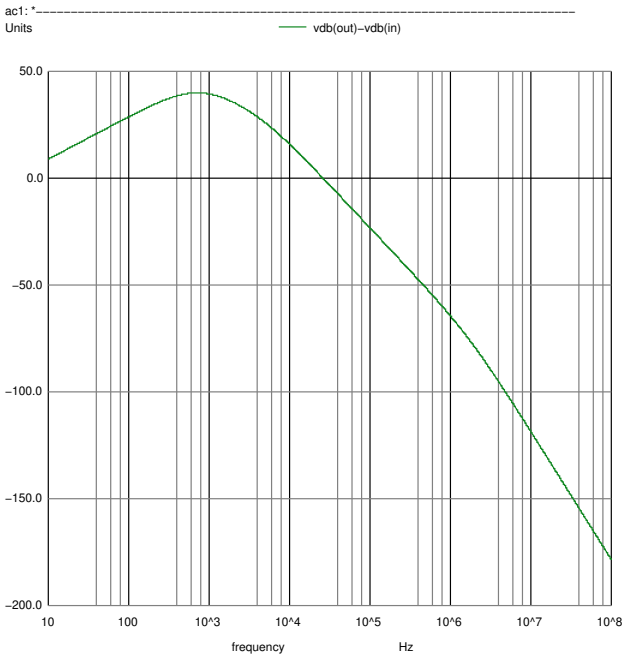

Figure 7: *Ngspice*'s gain in dB

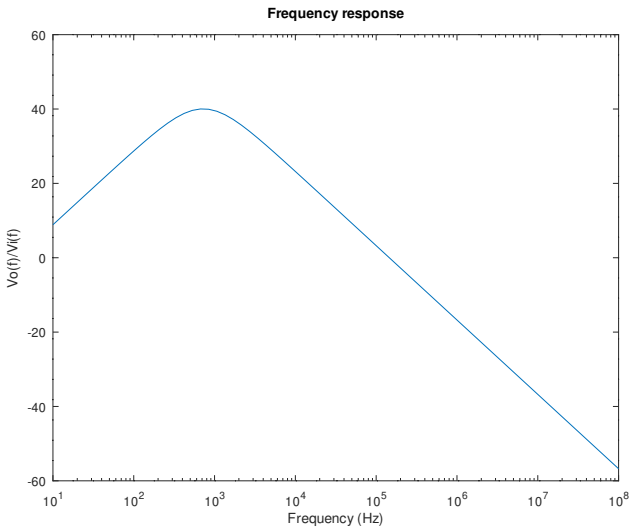

Figure 8: *Octave*'s gain in dB.

4.2 Phase plots

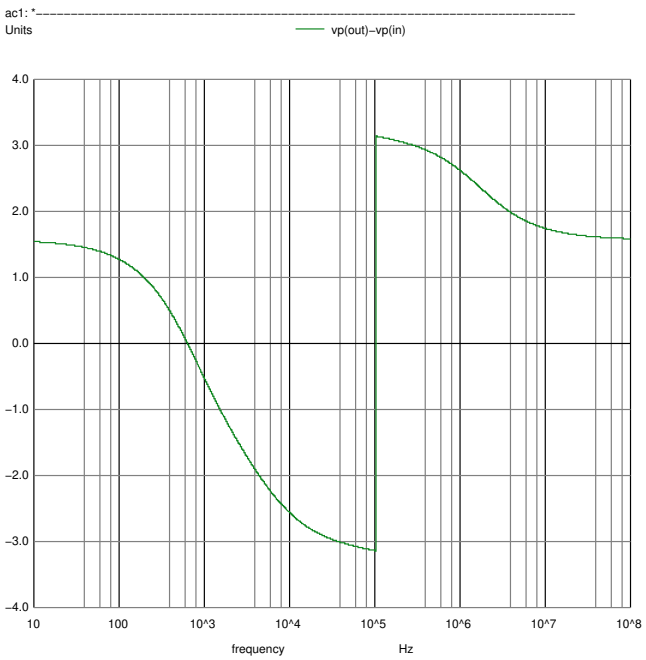

Figure 9: *Ngspice*'s phase plot.

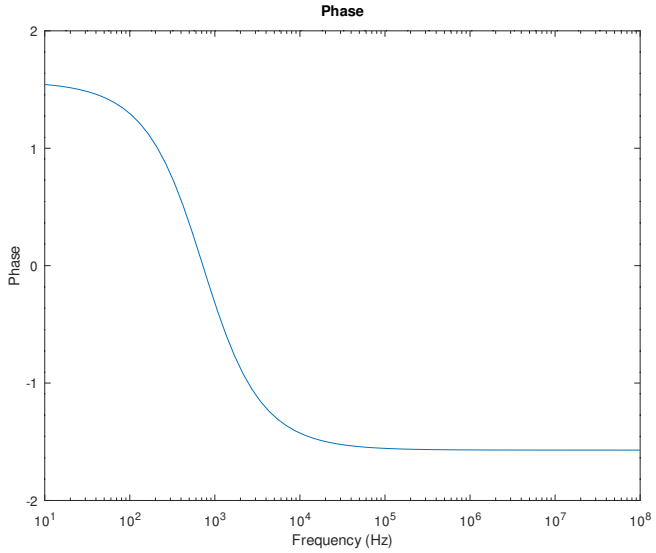

Figure 10: *Octave*'s phase plot.

4.3 Frequency tables

Name	Value [Hz]
lowercutoff	2.973792e+02
uppercutoff	1.638347e+03
fc	6.980045e+02

Table 8: *Ngspice*'s cut-off frequencies and central frequency.

Name	Value [Hz]
lowercutoff	300.161057
uppercutoff	1743.457911
fc	723.407333

Table 9: *Octave*'s cut-off frequencies and central frequency.

4.4 Gain tables

Name	Value [dB or -]
gaindb	3.997001e+01
lineargain	9.965532e+01

Table 10: *Ngspice*'s gain in dB and linear gain.

Name	Value [dB or -]
gain(dB)	40.043765
gain(linear)	100.505129

Table 11: *Octave*'s gain in dB and linear gain.

4.5 Input and output impedances (at central frequency) tables

Name	Value [Ω]
abszinatfc	1.440293e+03
abszoatfc	7.235581e+02

Table 12: *Ngspice*'s input and output impedances' absolute values.

Name	Value [Ω]
Z_{in}	1414.237243
Z_{out}	707.118621

Table 13: *Octave*'s input and output impedances' absolute values.

As one may notice, there are a few differences when comparing *Ngspice*'s and *Octave*'s results. This is somewhat normal, since the OP-AMP is composed of several transistors, which are non linear, and the model used in the theoretical analysis to describe it is the ideal model, which is far from reality. On the other hand, the model used in *Ngspice* is far more complex. Despite this, the results are quite satisfactory. The most notable difference is in between the two phase plots. This can be explained, once again, by the fact that we use the ideal OP-AMP model for the theoretical analysis, whereas *Ngspice* uses a real model, which in turn results in the introduction of two more poles in the transfer function, which end up changing the overall aspect of the phase plot.

5 Conclusion

In this laboratory assignment, the objective of analysing the circuit presented in figure 1 has been achieved. The analysis was performed both theoretically using the *Octave* maths tool and by circuit simulation using the *Ngspice* tool. Although the theoretical results differed slightly from the simulation results we did achieve good results overall. The reason for this slight mismatch is the fact that the model for the OP-AMP in both were different, being the theoretical a simpler of the two. In the end, we think that the goal of this laboratory was achieved. The building and optimization of the circuit allowed us to further reflect on the behaviour of OP-AMPs and their relation with the other components already studied.

References

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