Introduction to Digital Design Lab 315

- TA – May Lin (m.lin143@umiami.edu)
- Office – Lab 179 & 506.

Lab Content

- 2 Labs (Hardware , Software implementation)
- 2 Tests
- 3 VHDL Projects

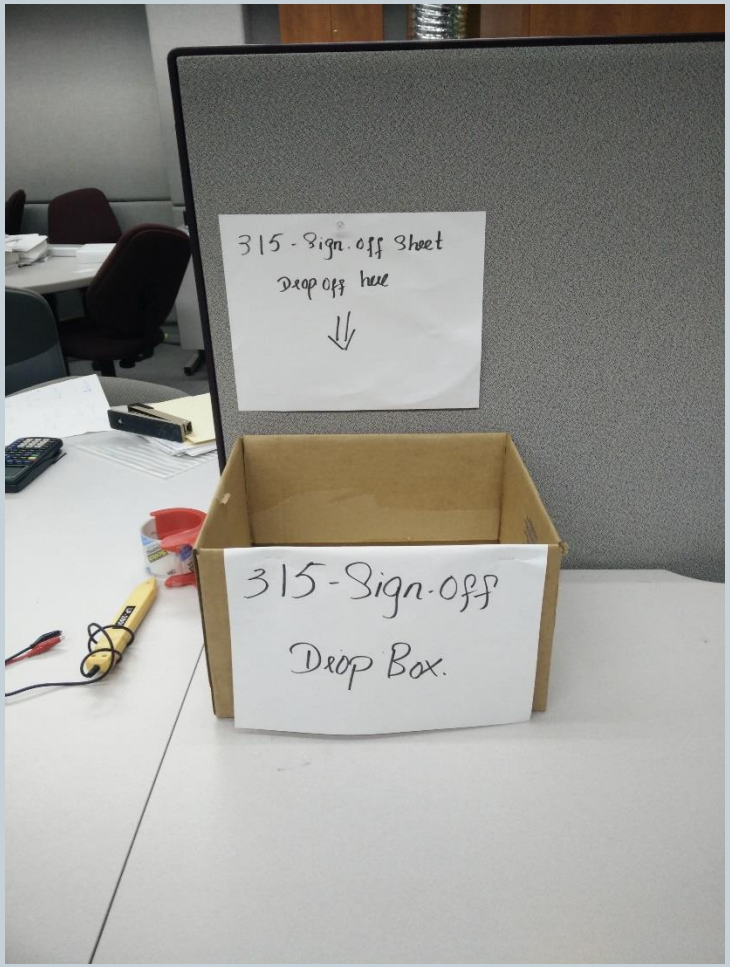
Group

- 2-3 Students per groups (max 3). You can also work individually.
- TA has no responsibility on distributing workload within your group.

Assignment and Submission

- 1 assignment per week (assigned on Monday).
- You have the whole week to finish it. Once you finish implementation, you need to ask one of the TAs to inspect your circuit.
- 3 TAs in lab 179 & 180
  - May Lin -315
  - Zhang Da -316
  - Part time TA
- After inspection, TA will sign on the Sign off sheet which you can download on Blackboard. (Before you ask us to check your circuit, you should have the Sign off sheet ready.)
- Once you get the signature, you can drop off the sheet in Sign off Drop Box in Lab 179. (Before you drop off, take the pic of your sigh off sheet.)

Sign Off Sheet & Drop off



Project 1: Four bit Multiplier

Student Group Number: 11

Student Name	Student C #	Contribution	Signature
[redacted]	[redacted]	Circuit Written/Debugging	[redacted]
[redacted]	[redacted]	Debugging	[redacted]

Due Date:
Monday, February 15, 2016

Assignment Specifications:
Implement a four bit multiplier in Quartus. Test the design with various inputs. Compare simulations with hand calculations.

To Be Submitted:
☑ Fully functional four bit multiplier implemented in Quartus.

Comments:

Sign Off Date	Sign Off Time	TA Signature
02/15/2016	3:00 pm	[signature]

Report Submission

- The report has to be individual. You may share the circuit diagrams and table within group members.

(It has to be typed. No handwritten tables or diagram.)

- Submit a Soft Copy PDF of your report to my email (m.lin143@umiami.edu).
- Please follow the submission description mentioned in Blackboard for email Subject & Report file name.
- Once I receive your report, I will reply back confirming the receipt within 1-2 days.
- If you don't get my reply, please inform me on the next following class.

Course Content

- Familiarization with properties and use of digital electronic Components (logic gates, FFs, etc.)
  - Tone Generator – Hardware Implementation
    - Lab 1.A – Sequence Generator (Assign 01/23; Due 01/30)
    - Lab 1.B – Frequency Generator (Assign 01/30; Due 02/6)

    Report for Lab 1 Due on 02/07 11:59 pm.
  - Implementation using Quartus II
    - Lab 2 – 4 –Bit Multiplier (Assign 02/06; Due 02/13)

    Report for Lab 2 Due on 02/14 11:59 pm.
- Test 1 – testing the understanding on design and component usage on Lab 1 & 2. (02/20)
- Introduction to VHDL Programming
  - Full-Subtractor
    - VHDL 1 – Implementation of Full Subtractor in VHDL (Assign 02/27: Due 03/06)

    Report for VHDL 1 Due on 03/07 11:59 pm.
  - VHDL 2
    - (Assign 03/06; Due TBA)

    Report for VHDL 2 Due on TBA.
  - VHDL 3
    - (Assign TBA; Due TBA)

    Report for Lab 3 Due on TBA..
- Test 2 – Basic knowledge on VHDL programming.
- Final Presentation on Calculator Project .

* Subject to change according the project progress.

Grading

	Implementation	Report	Final Grade	Remark
Lab 1	7.5%	7.5%	15%	
Lab 2	7.5%	7.5%	15%	
Test 1			15%	
VHDL 1	5%	5%	10%	
VHDL 2	7.5%	7.5%	15%	
VHDL 3	7.5%	7.5%	15%	
Test 2			15%	
Total			100%	

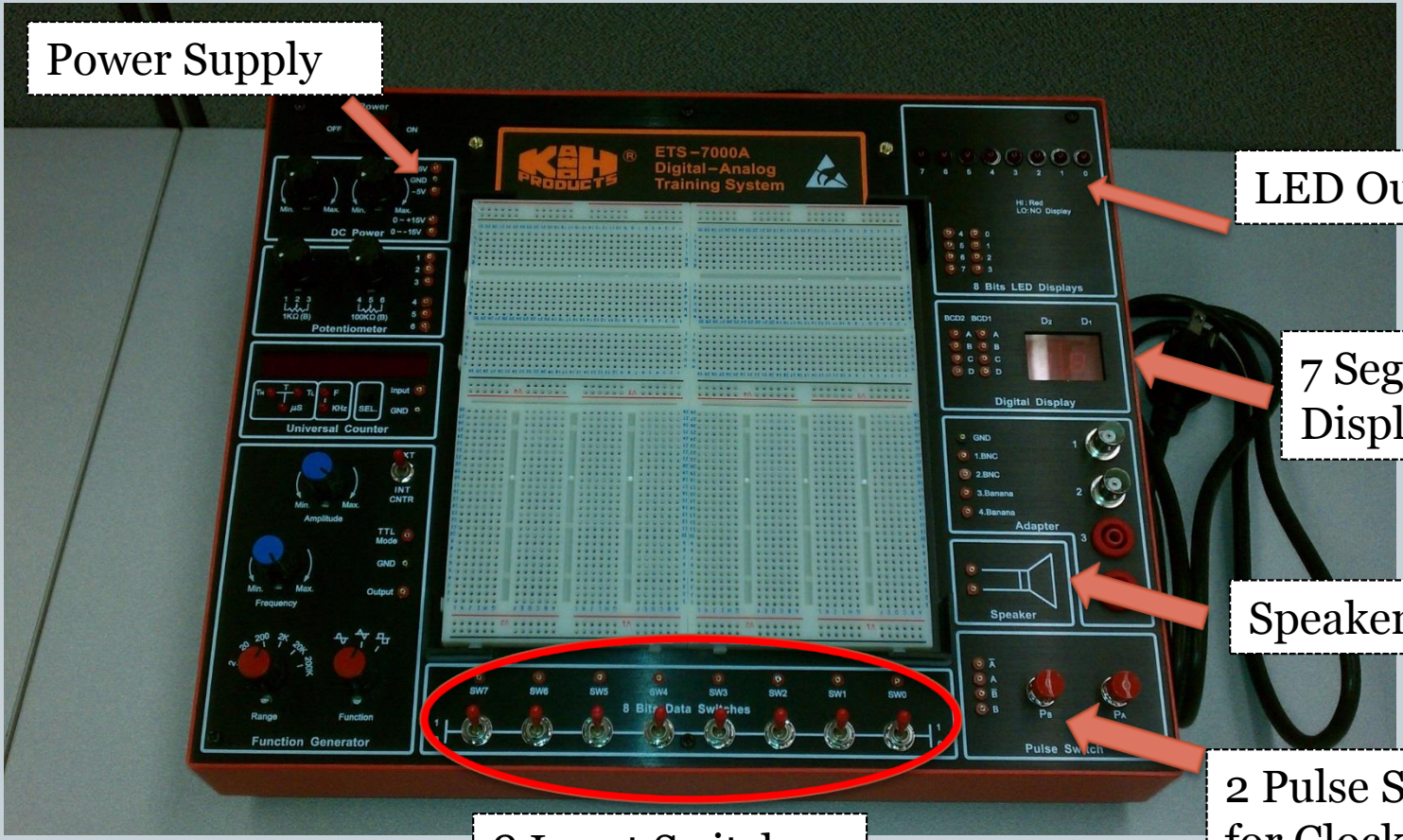
Lab Hour

- Weekdays 10 am - 6 pm.
- On Saturday 10 am – 12 pm (only by appointment. You must make an appointment for weekends on Thursday.)
- whoever leaves the lab last after 6 pm has the responsibility to lock the lab.

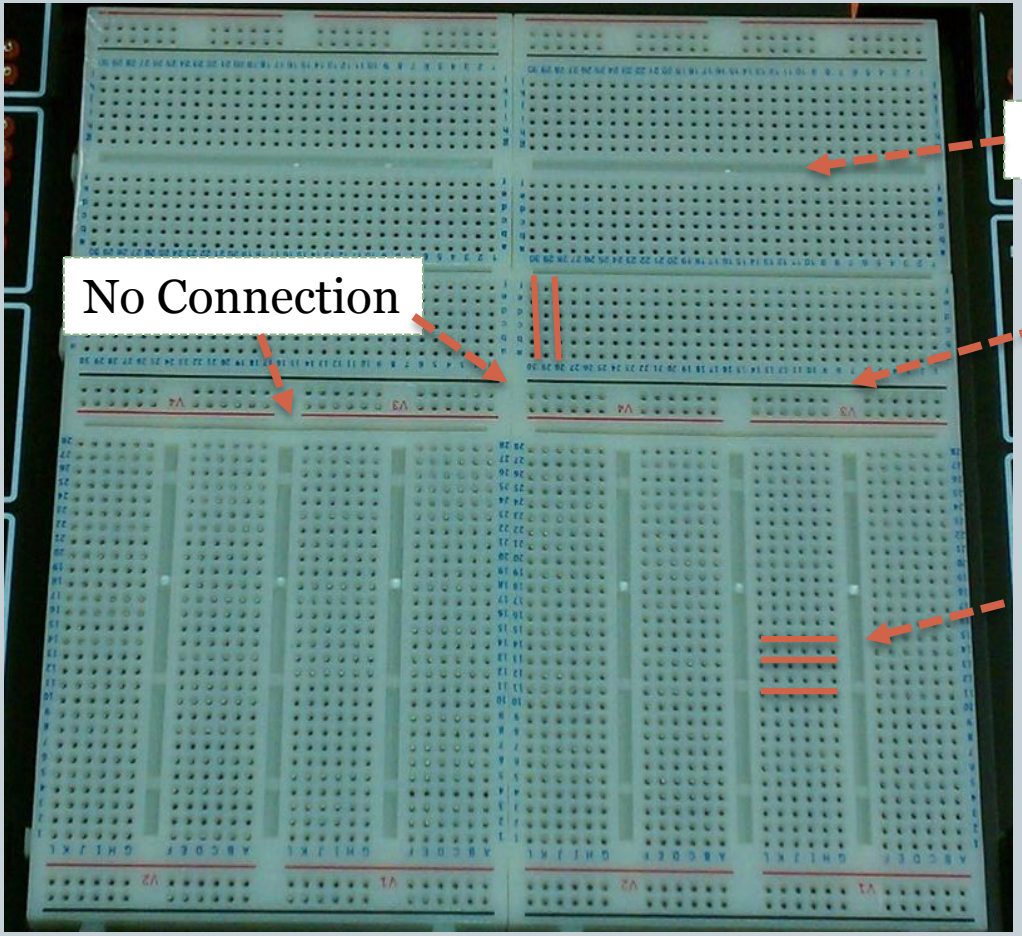
Lab Equipment

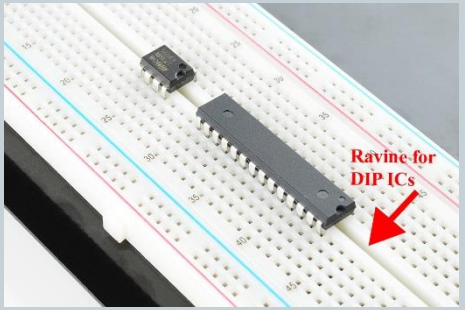
- Hardware Implementation
  - Digital Trainer Kit
  - Bread Board
  - Testing Probe
  - ICs
  - Jumpers

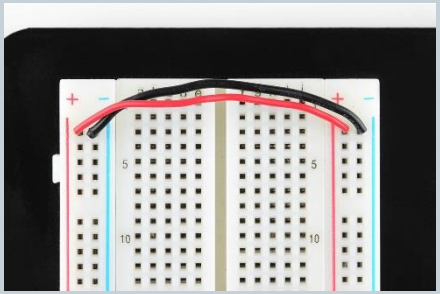
Digital Trainer Kit

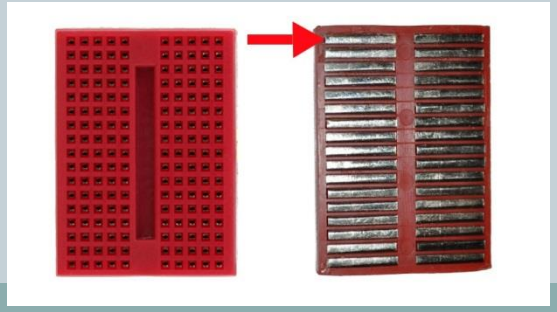


Bread Board

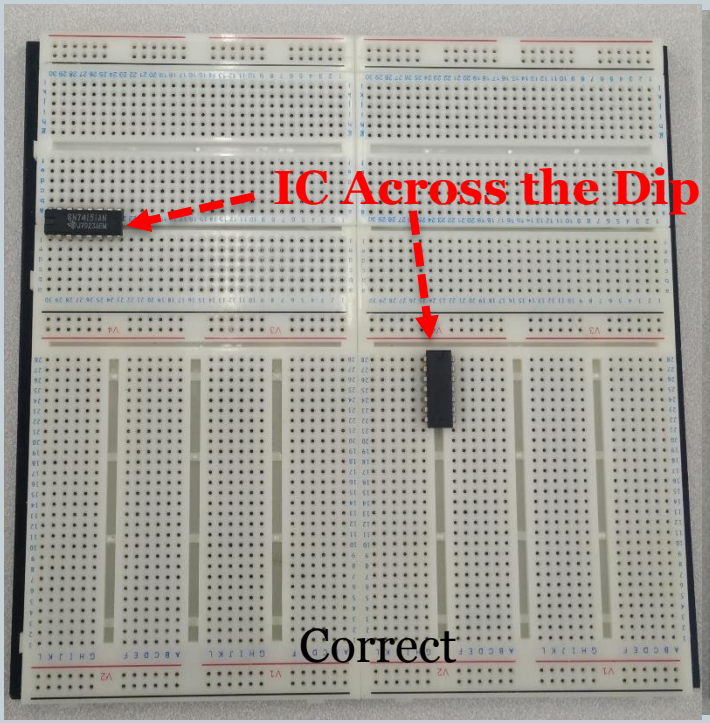

Dip Support
No Connection
Power Rails
Terminal Strips

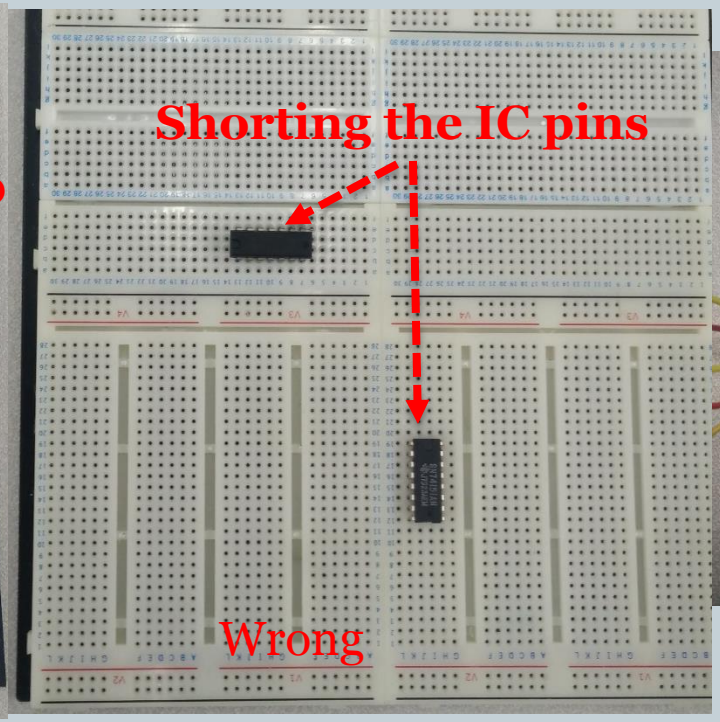

Ravine for
DIP ICs

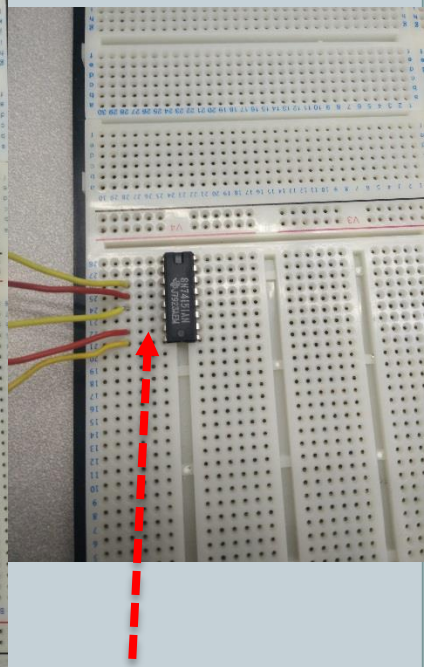




Breaboard Tips

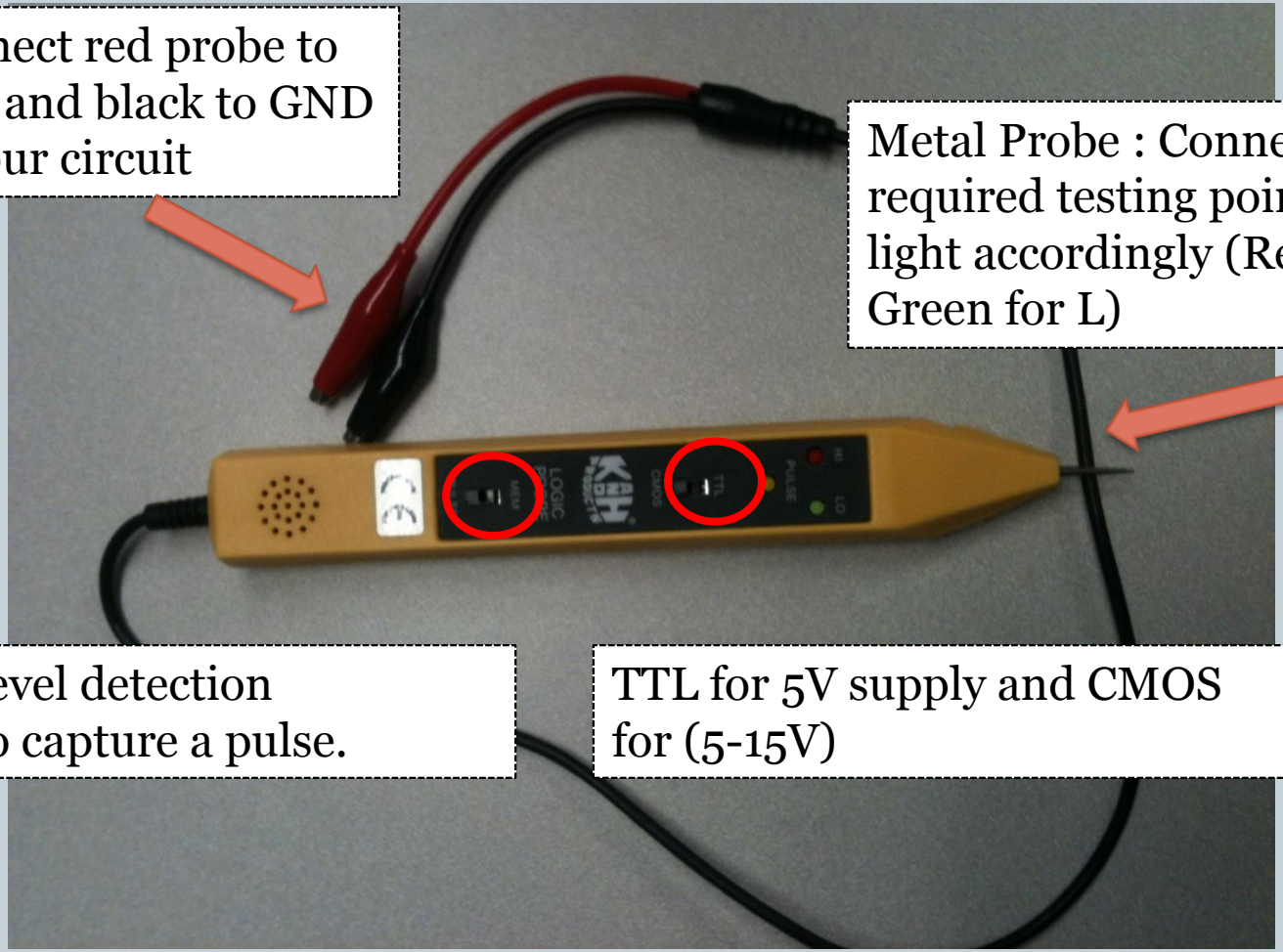






When connecting IC pins, leave some space between jumpers and pins so that it is easier to reach to the IC pins later in debugging.

Testing Probe



Connect red probe to VCC and black to GND of your circuit

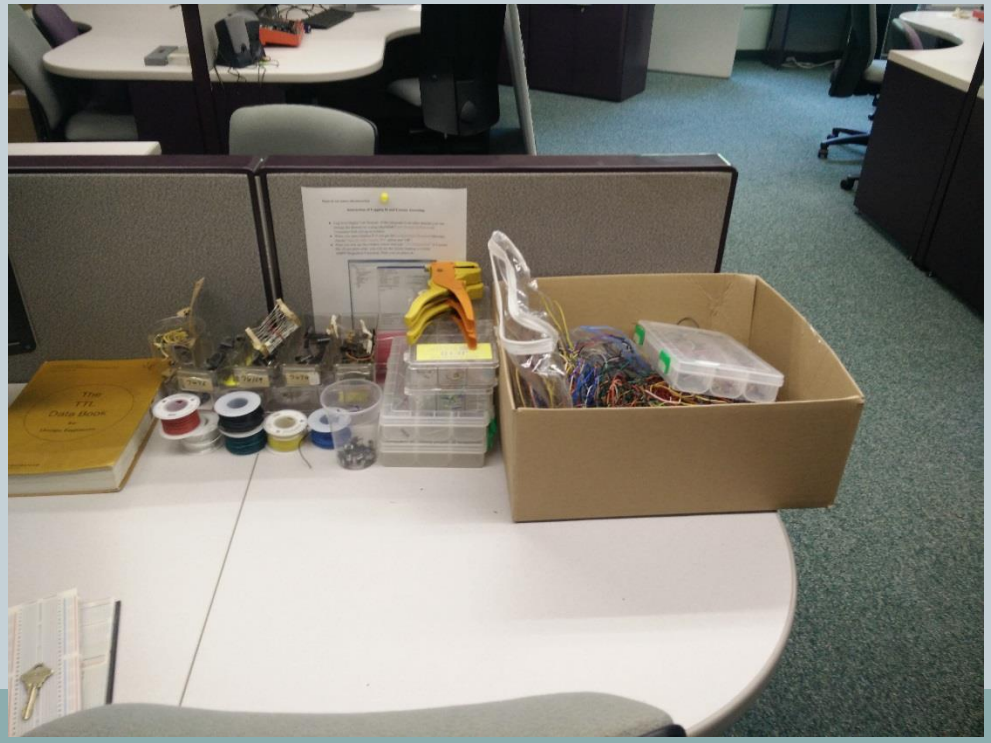
Metal Probe : Connect to the required testing point. LED will light accordingly (Red for H and Green for L)

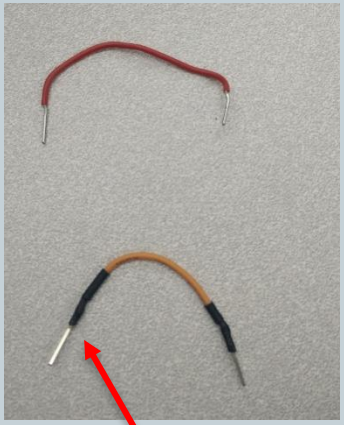
Pulse : level detection
Mem : to capture a pulse.

TTL for 5V supply and CMOS for (5-15V)

IC, Resistors and LED

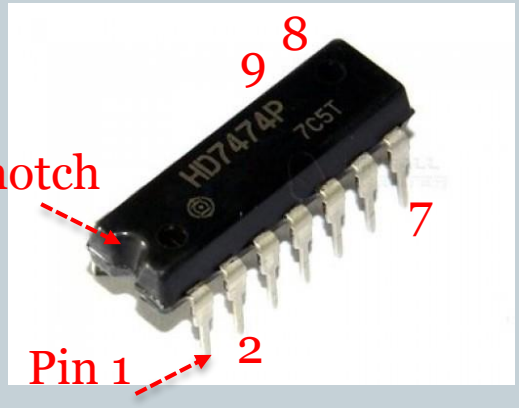
- ICs and Jumpers are provided in Lab 180.
- Put the used jumper in the box. You may recycle the jumper.
- When reusing jumper, use the wire without pin head. Those jumper with the pin head might be broken at the pin head.





Avoid using Jumpers with Pin head

IC Data Book



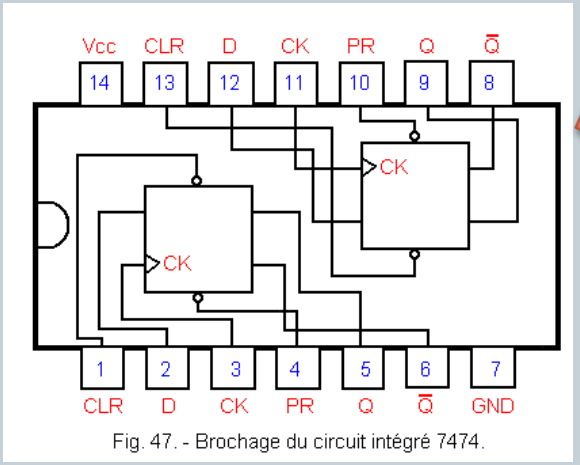


Fig. 47. - Brochage du circuit intégré 7474.

SN5474, SN54LS74A, SN54S74
SN7474. SN74LS74A, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

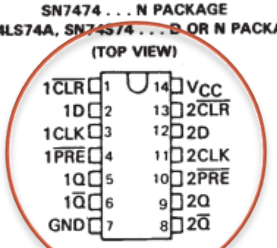
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

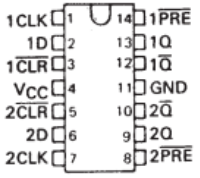
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

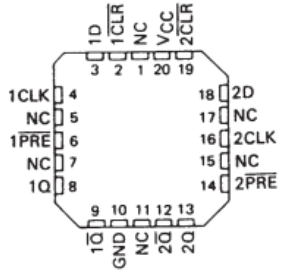
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)



SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

Digital Circuits

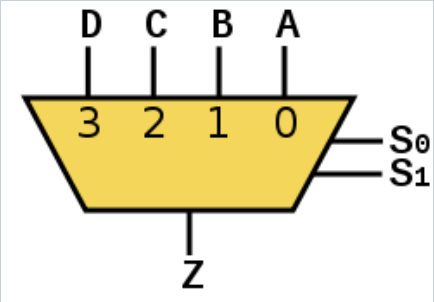
- Combinational and Sequential.
- Combinational logic is used in computer circuits to do boolean algebra on input signals and on stored data. In digital circuit theory, combinational logic (sometimes also referred to as combinatorial logic) is a type of digital logic which is implemented by boolean circuits, where the output is purely a function of the present input only.

Elements of Combinational Circuits

- Logic gates. (AND/ OR/ NOT/ NAND/NOR/XOR/XNOR).
- Multiplexer.
- DE-multiplexer.
- Encoder.

Multiplexer.

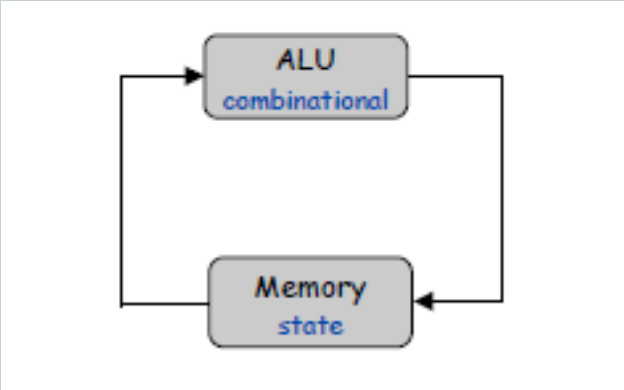
- In digital electronics, a multiplexer (or mux) is a device that selects one of several digital input signals and forwards the selected input into a single output line.



- A multiplexer of inputs has ‘n’ select lines, which are used to select which input line to send to the output.

Sequential

- In digital circuit theory, sequential logic is a type of logic circuit whose output depends not only on the present input but also on the history of the input. This is in contrast to combinational logic, whose output is a function of only the present input. That is, sequential logic has memory to store the previous states.



Elements of Sequential Circuits

- Latch and Flip Flop
- Different type of Flip Flops:

1) SR Flip Flop
2) D Flip Flop
3) JK Flip Flop
4) T Flip Flop