

# Lab 1A - Sequence Generator

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# Implementation LAB 1A

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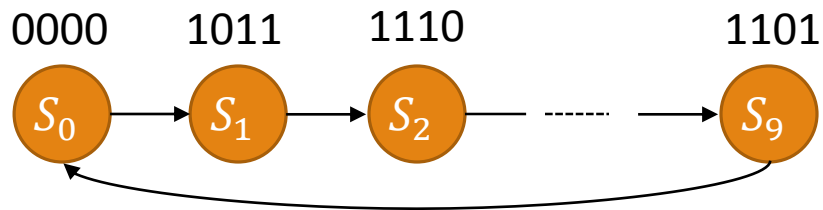
## Deliverables:

### 1. Sequence generator:

- Design and implement a sequence generator to generate a sequence which has a minimum of 10 different states: 0, 11, 14, 5, 4, 15, 12, 9, 2, 13, 0, 11, ...
- Ensure that all invalid stages of the machine clear it (set it too state zero.)
- Make sure you have zero in your sequence.

# Sequence generator

The sequence : 0, 11, 14, 5, 4, 15, 12, 9, 2, 13, 0, 11, ...



Design the circuit using D flip-flop and MUX.

PS	D MSB	C	B	A LSB	NS	QD	QC	QB	QA
0	0	0	0	0	11	1	0	1	1
1	0	0	0	1		0	0	0	0
2	0	0	1	0	13	1	1	0	1
3	0	0	1	1		0	0	0	0
4	0	1	0	0	15	1	1	1	1
5	0	1	0	1	4	0	1	0	0
6	0	1	1	0		0	0	0	0
7	0	1	1	1		0	0	0	0
8	1	0	0	0		0	0	0	0
9	1	0	0	1	2	0	0	1	0
10	1	0	1	0		0	0	0	0
11	1	0	1	1	14	1	1	1	0
12	1	1	0	0	9	1	0	0	1
13	1	1	0	1	0	0	0	0	0
14	1	1	1	0	5	0	1	0	1
15	1	1	1	1	12	1	1	0	0

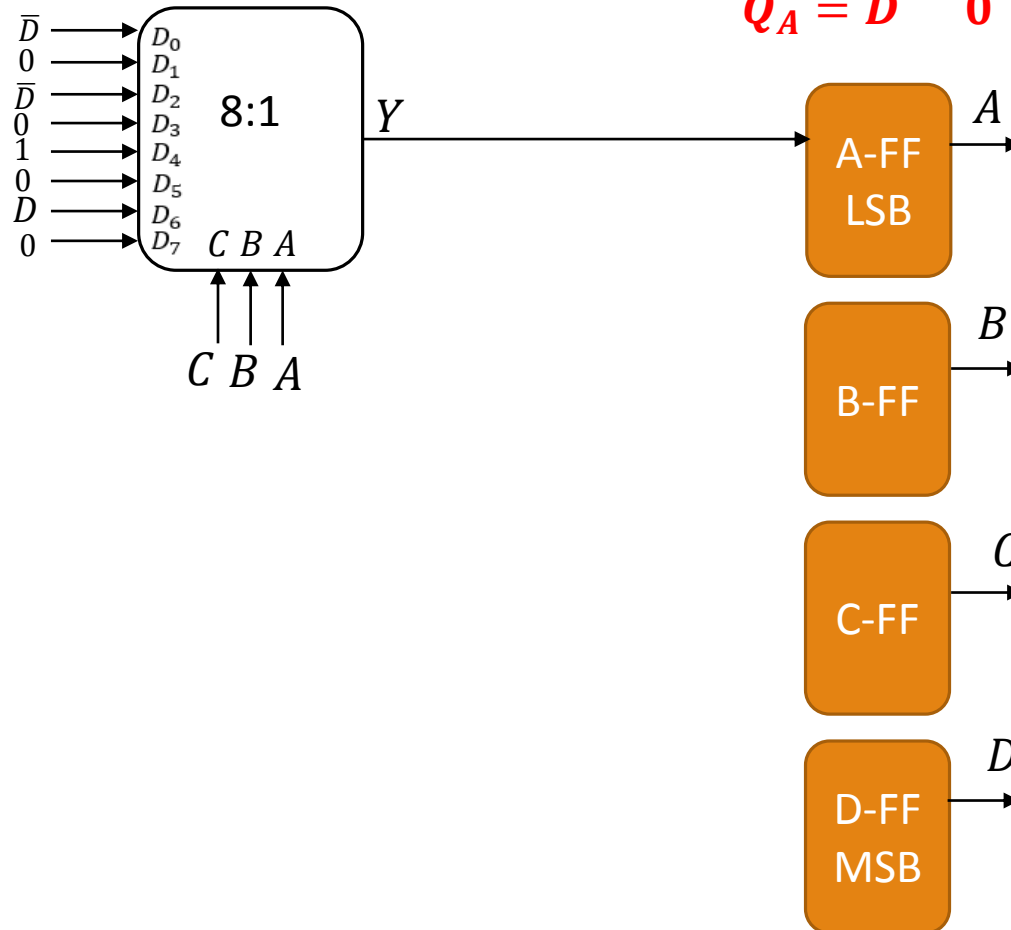
# MUX Design

PS	D MSB	C	B	A LSB	NS	QD	QC	QB	QA
0	0	0	0	0	11	1	0	1	1
1	0	0	0	1		0	0	0	0
2	0	0	1	0	13	1	1	0	1
3	0	0	1	1		0	0	0	0
4	0	1	0	0	15	1	1	1	1
5	0	1	0	1	4	0	1	0	0
6	0	1	1	0		0	0	0	0
7	0	1	1	1		0	0	0	0
8	1	0	0	0		0	0	0	0
9	1	0	0	1	2	0	0	1	0
10	1	0	1	0		0	0	0	0
11	1	0	1	1	14	1	1	1	0
12	1	1	0	0	9	1	0	0	1
13	1	1	0	1	0	0	0	0	0
14	1	1	1	0	5	0	1	0	1
15	1	1	1	1	12	1	1	0	0

- 4 D- Flip Flops
- Use Mux to derive the input of each flip flops.
- Use **CBA** as the select for MUX

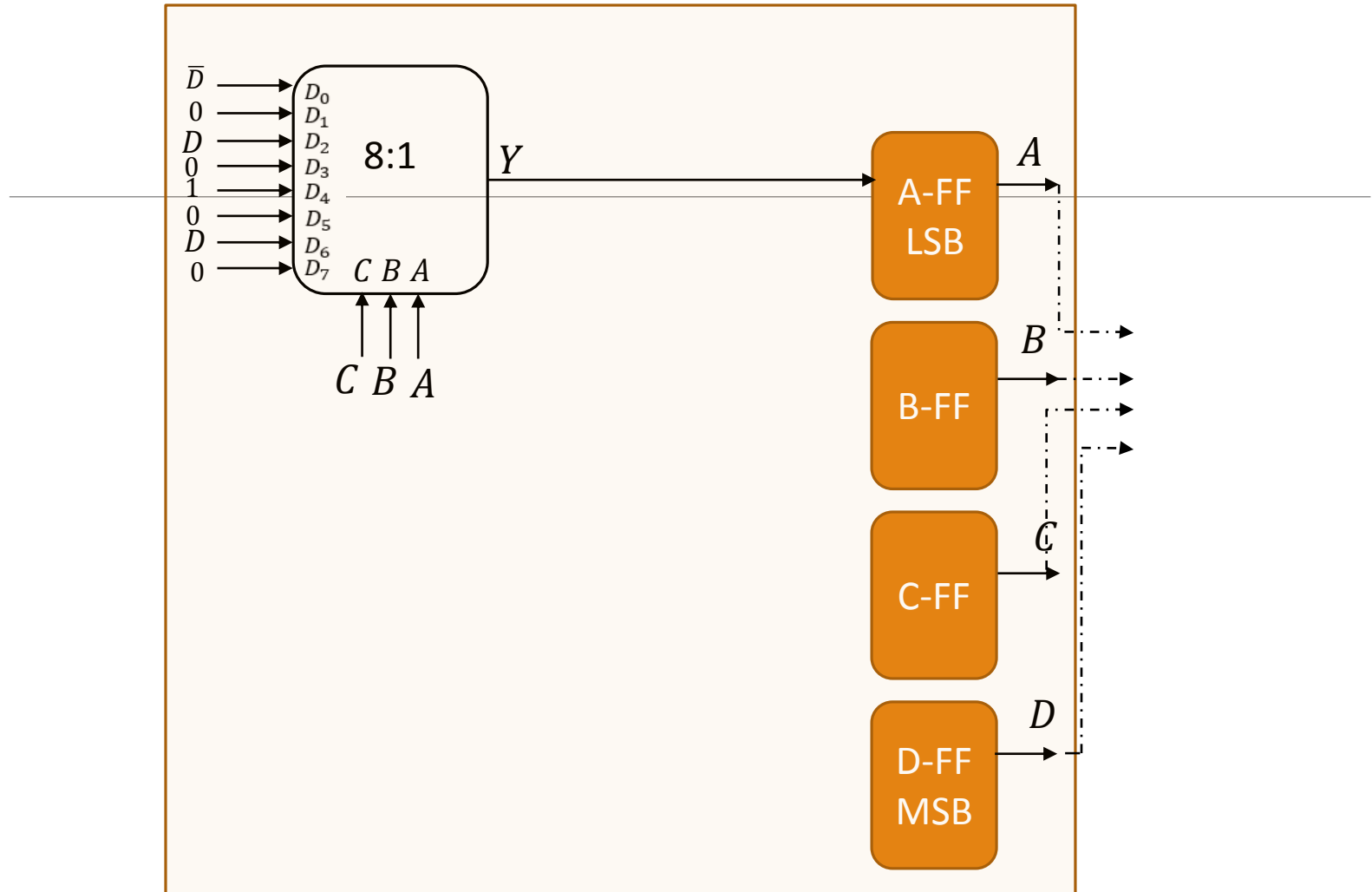
		CBA							
		000	001	010	011	100	101	110	111
D	0	1	0	1	0	1	0	0	0
	1	0	0	0	0	1	0	1	0
$Q_A = \bar{D}$		0	$\bar{D}$	0	1	0	$D$	0	

# Circuit Diagram



CBA		000	001	010	011	100	101	110	111
D	0	1	0	1	0	1	0	0	0
	1	0	0	0	0	1	0	1	0

$Q_A = \bar{D} \quad 0 \quad \bar{D} \quad 0 \quad 1 \quad 0 \quad D \quad 0$



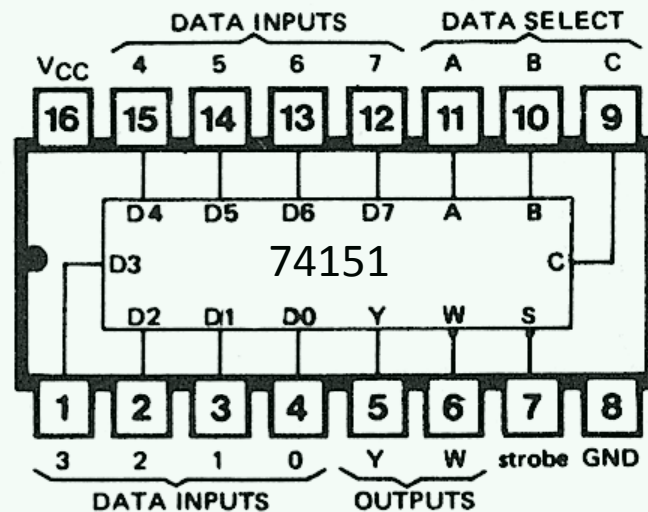
Sequence Generator

# ICs

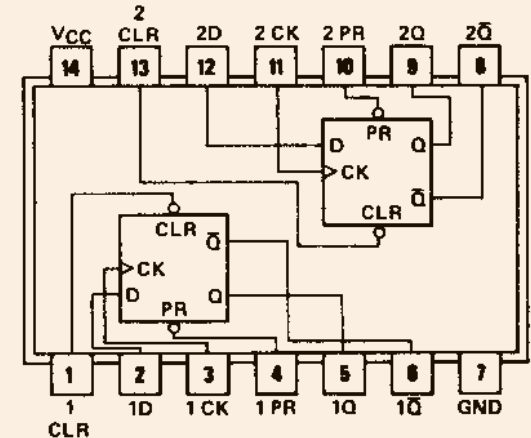
- 7474 Dual Positive Edge Triggered D-FF
  - Vcc to PR and CLR Pin
- 74151 8:1 Mux.
  - Gnd to Strobe Pin

Truth Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$



## 7474



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{Q_0}$