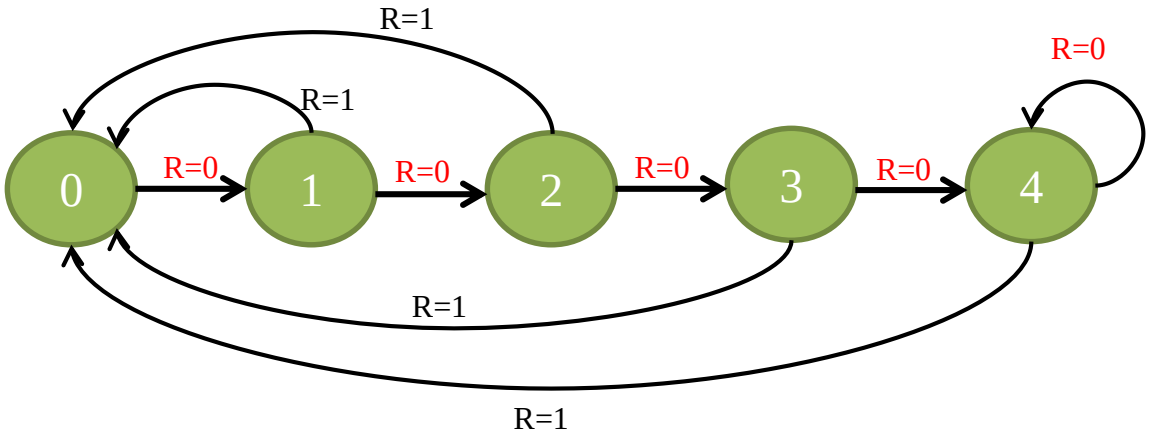
Lab 5 A

- Counter, 8 Bit Register and BCD Circuit
  - i. Counter
    - Design a 3 Bit Up Counter with Reset.
  - ii. 8 Bit Register
    - Design a 8 Bit Register which stores and outputs a 8 bit binary input on clock rising edge with ‘High’ on Load Input.
  - iii. Design a ckt to decode a 8 bit binary to BCD.

Counter Design Example

- Design a 3 bit up counter which counts 0,1,2,3 and 4 once reset, it goes back to zero.



Counter Design Example

PS CBA	NS R=0 $C^+B^+A^+$	NS R=1 $C^+B^+A^+$
000	001	000
001	010	000
010	011	000
011	100	000
100	100	000

CR \ BA	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	x	x	x
10	0	x	x	x

$$A^+ = \bar{A}\,\bar{C}\bar{R}$$

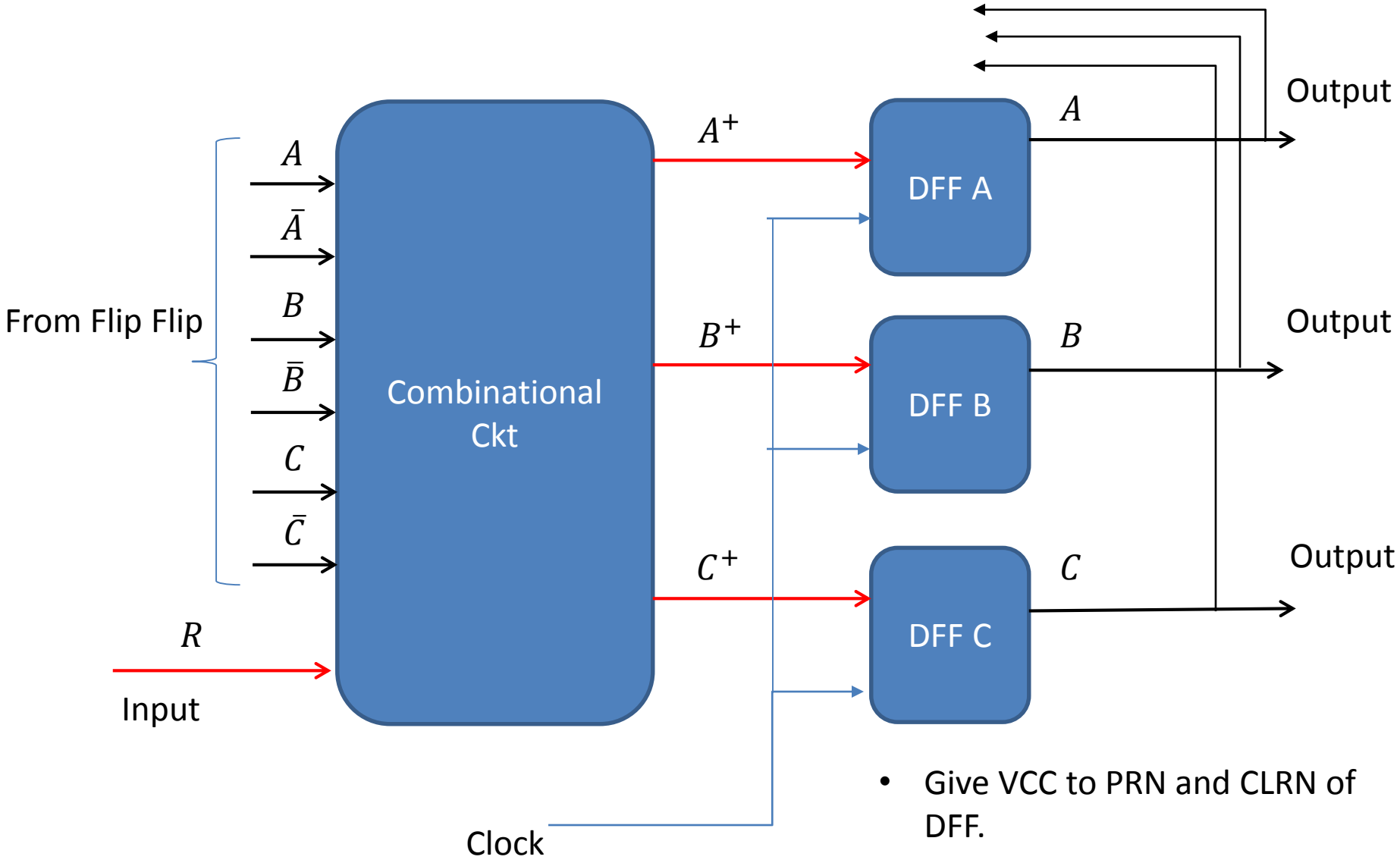
CR \ BA	00	01	11	10
00	0	1	0	1
01	0	0	0	0
11	0	x	x	x
10	0	x	x	x

$$B^+ =$$

CR \ BA	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	0	x	x	x
10	1	x	x	x

$$C^+ =$$

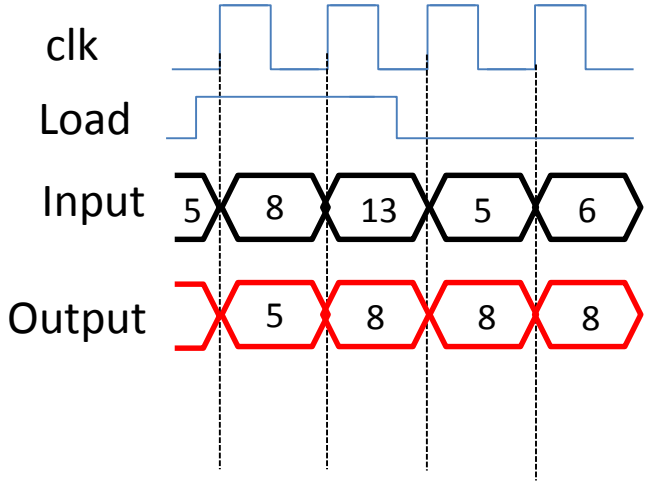
Counter Block Diagram



- Give VCC to PRN and CLRN of DFF.

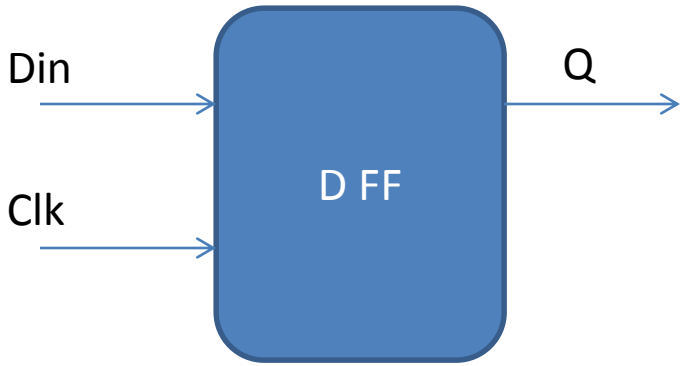
A 8 bit Register Using Dff

- A register is a storage or memory component in a digital ckt.
  - If (clock rising edge and Load = ‘1’)
    - Output = input;
  - Else
    - Output = Prev_Output;
  - End if;



D Flip Flop

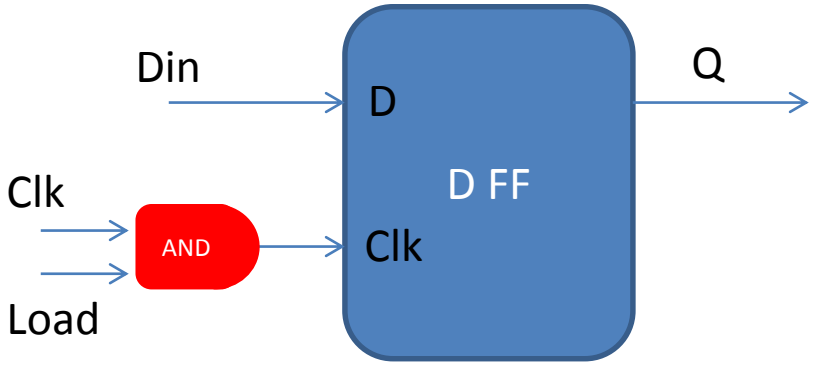
D	Clk	Q+
x	0	No change
1	Rising Edge	1
0	Rising Edge	0



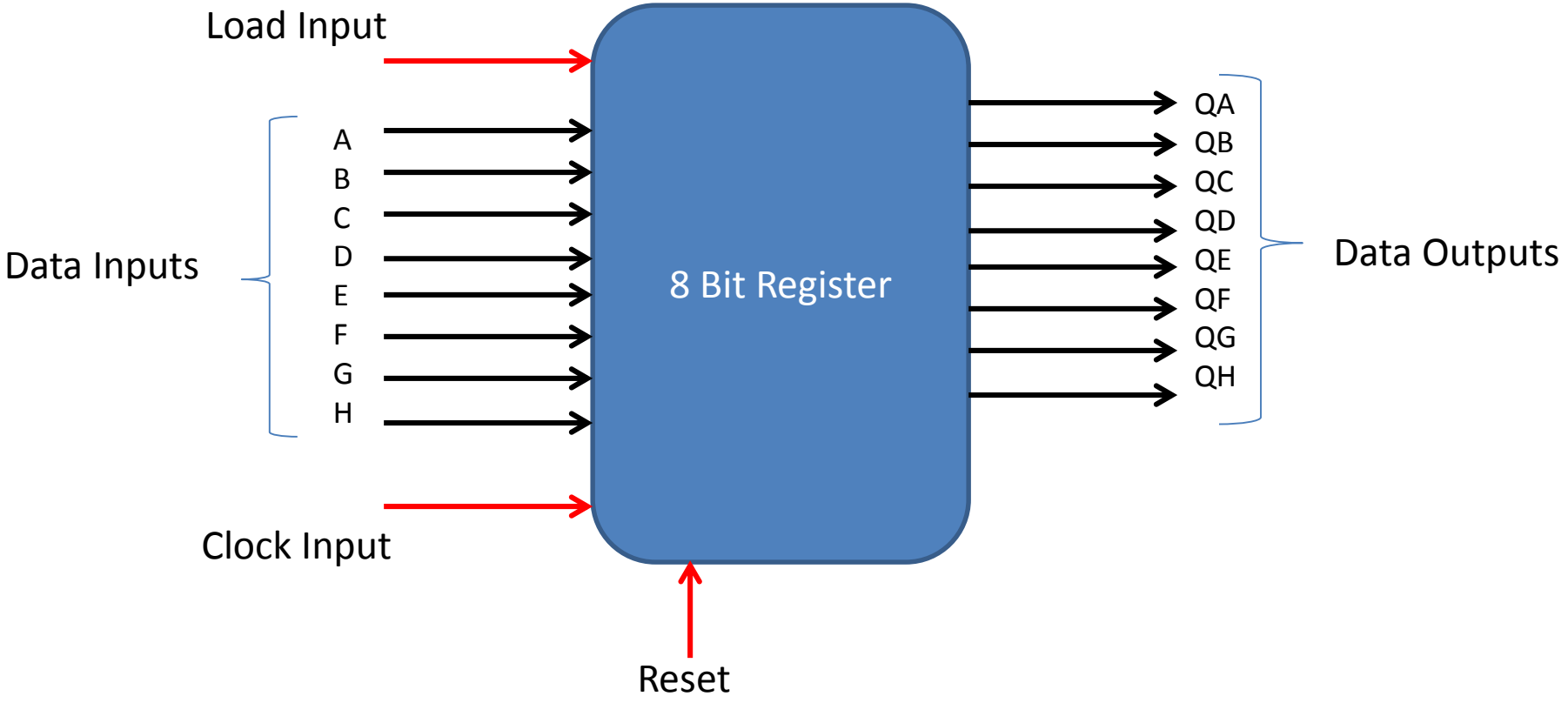
Modified D Flip Flop

- Modify D FF with an extra input: Load.

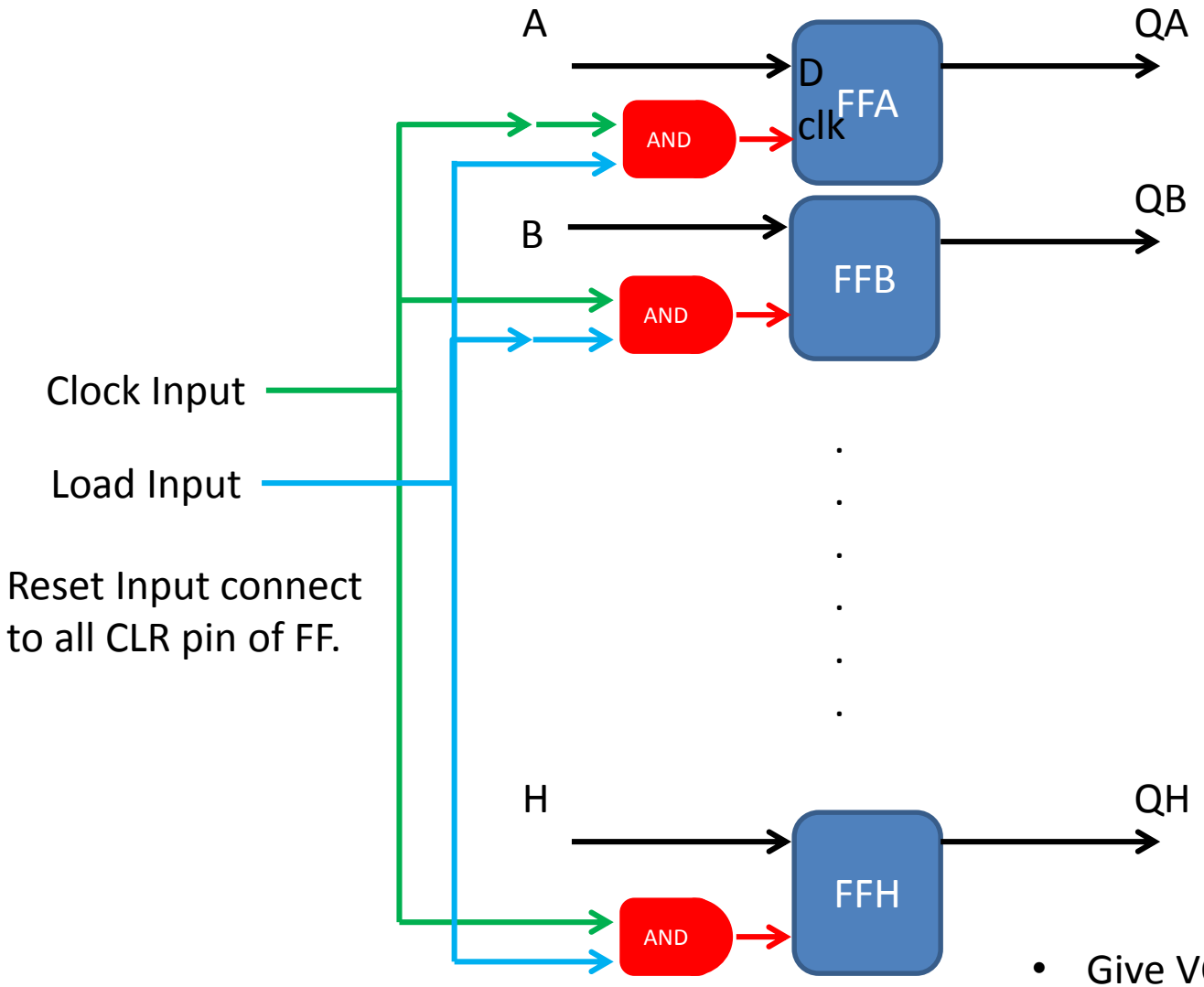
D	Clk	Load	Q+
x	0	0	No change
x	Rising Edge	0	No Change
1	Rising Edge	1	1
0	Rising Edge	1	0



Register Block Diagram



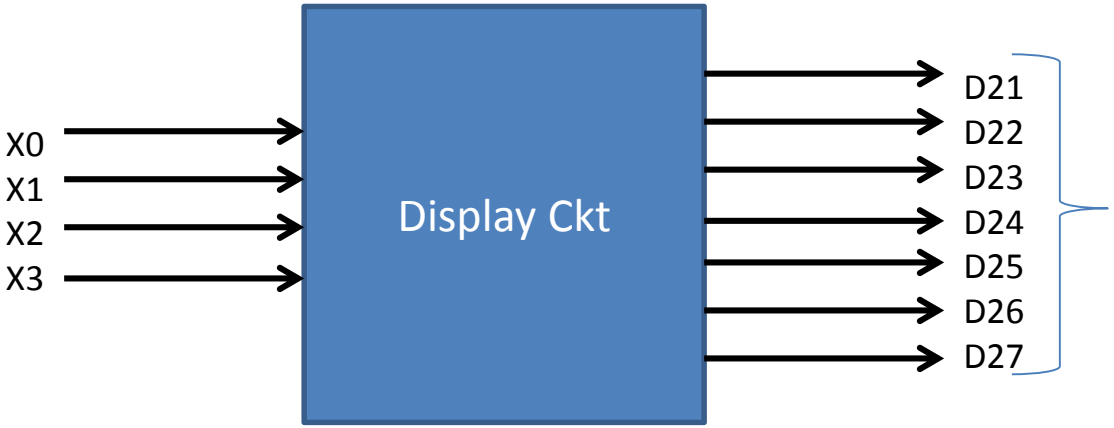
8 Bit Register



- Give VCC to PRN.

Modify Display Ckt

- First, modify your 7 segment display ckt to 4 inputs - 7 outputs. (Just Delete the Display output (D10-D16).



BCD

- A BCD is a binary system which represents one decimal number with 4 binary number.
  - 15 → 1111 (in Binary)
  - 15 →0001 0101 (in BCD)
- Implement a ckt that convert a 8 bit binary input to two BCD.
- Maximum binary the ckt can decode is 99.
- When the input is higher than 99,

overflow = ‘1’.

BCD: Binary Coded Decimal

Binary Number	BCD Outputs $U_3U_2U_1U_0$ $L_3L_2L_1L_0$	OverFlow
0000 0001 . . .	0000 0001	0 . . .
0000 1001	0000 1001	0
0000 1010	0001 0000	0
0000 1011	0001 0001	0
0000 1100	0001 0010	0
. . . 0110 0011	1001 1001	. . . 0
0110 0100	xxxx xxxx	1

Shift Add 3 Alg

- Do 8 times (for 8 bin binary input).
- 1. Shift left one to the binary input.
- 2. Add 3 to BCD if its greater than 5.
- 3. Go to 1.

Example

$$(99)_{10} = (01100011)_2 = (1001\ 1001)_{BCD}$$

		BCD								Binary							
	OF	U3U2U1U0				L3L2L1L0											
		2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	0	1	1	0	0	0	1	1
Shift 1		0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	
Shift 2		0	0	0	0	0	0	0	1	1	0	0	0	1	1		
Shift 3		0	0	0	0	0	0	1	1	0	0	0	1	1			
Shift 4		0	0	0	0	0	1	1	0	0	0	1	1				
Add- 3						0	0	1	1								
		0	0	0	0	1	0	0	1	0	0	1	1				
Shift 5		0	0	0	1	0	0	1	0	0	1	1					
Shift 6		0	0	1	0	0	1	0	0	1	1						
Shift 7		0	1	0	0	1	0	0	1	1							
Add 3						0	0	1	1								
		0	1	0	0	1	1	0	0	1							
Shift 8		1	0	0	1	1	0	0	1								

Example

$(100)_{10} = (01100100)_2 = (0000\ 0000)_{BCD}$ and OF = 1 (overflow)

		BCD								Binary							
	OF	U3U2U1U0				L3L2L1L0											
		0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
Shift 1		0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	
Shift 2		0	0	0	0	0	0	0	1	1	0	0	1	0	0		
Shift 3		0	0	0	0	0	0	1	1	0	0	1	0	0			
Shift 4		0	0	0	0	0	1	1	0	0	1	0	0				
Add- 3						0	0	1	1								
		0	0	0	0	1	0	0	1	0	1	0	0				
Shift 5		0	0	0	1	0	0	1	0	1	0	0					
Shift 6		0	0	1	0	0	1	0	1	0	0						
Add 3						0	0	1	1								
		0	0	1	0	1	0	0	0	0	0						
Shift 7		0	1	0	1	0	0	0	0								
		0	0	1	1												
		1	0	0	0	0	0	0	0								
Shift 8	1	0	0	0	0	0	0	0									

Add 3 Ckt

- If Input $>$ 5
- Output = Input +3;
- Else
- Output = Input;
- End

Input = 0101 (which is greater than 4)

Output = 0101 + 0011 = 1000

Input DCBA	Output QDQCQBQA
0000	0000
0001	0001
0010	0010
0011	0011
0100	0100
0101	1000
0110	1001
0111	
1000	
1001	
1010	xxxx
.	.
.	.
1111	xxxx

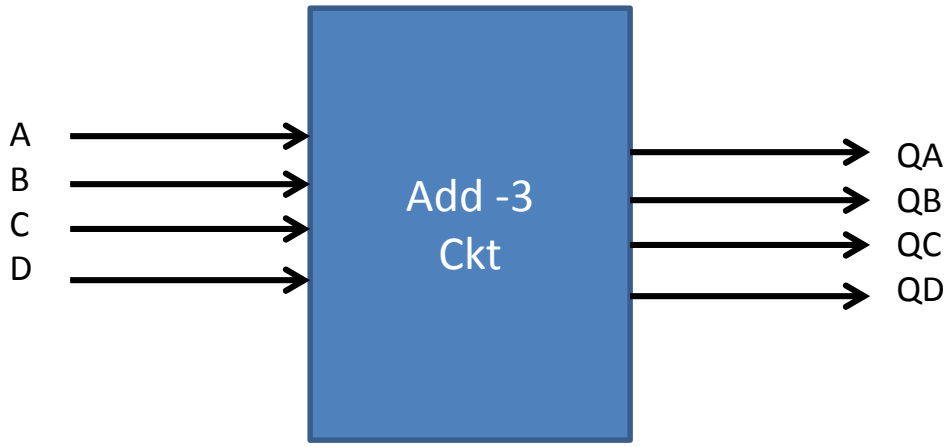
When $input \leq 4$.

Fill these outputs

When input > 9, don't care.

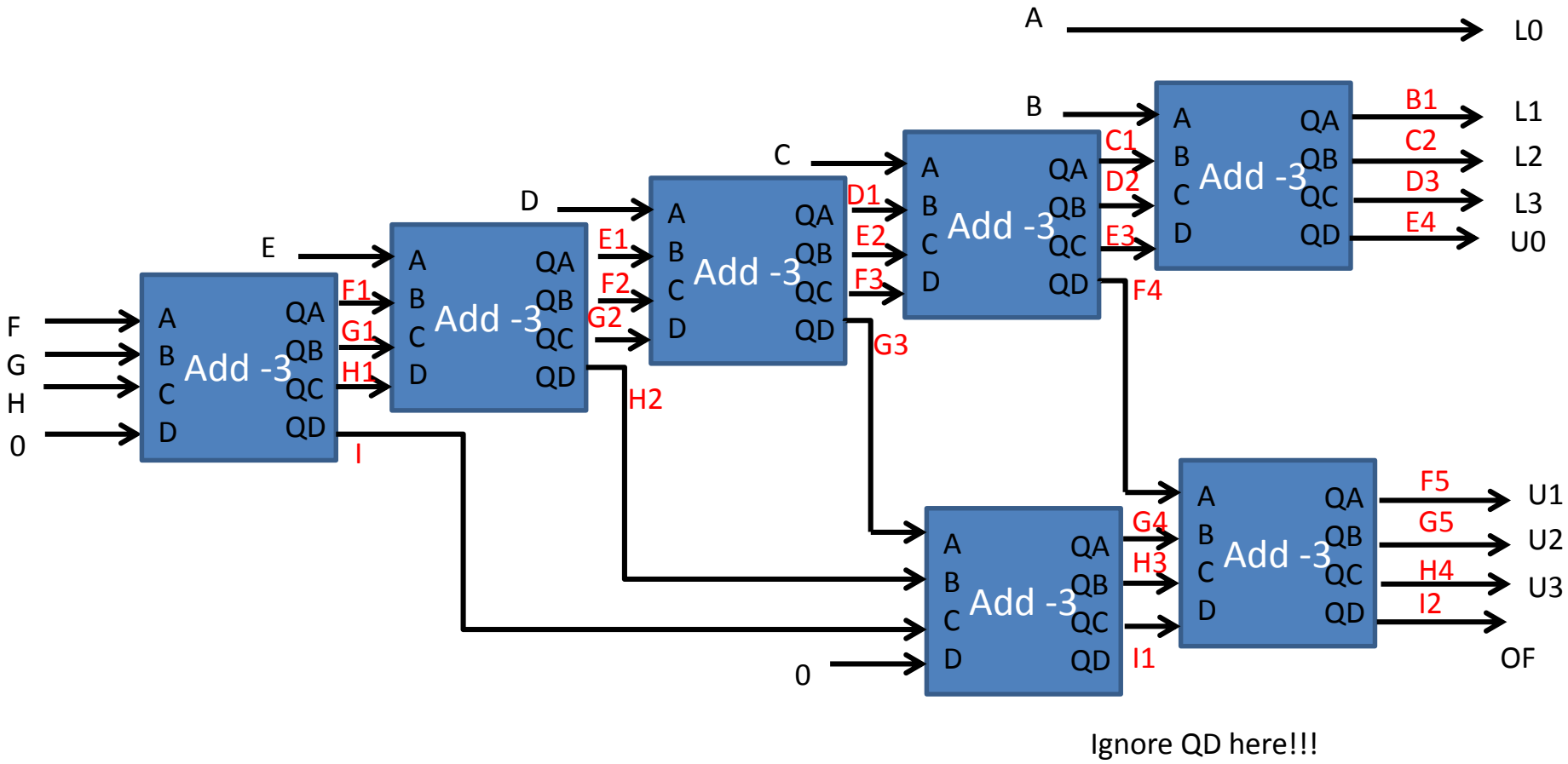
Add 3 Ckt

- Complete the Truth Table from prev slide
- Find the Boolean expression for QD,QC,QB and QA.
- Implement the Ckt.



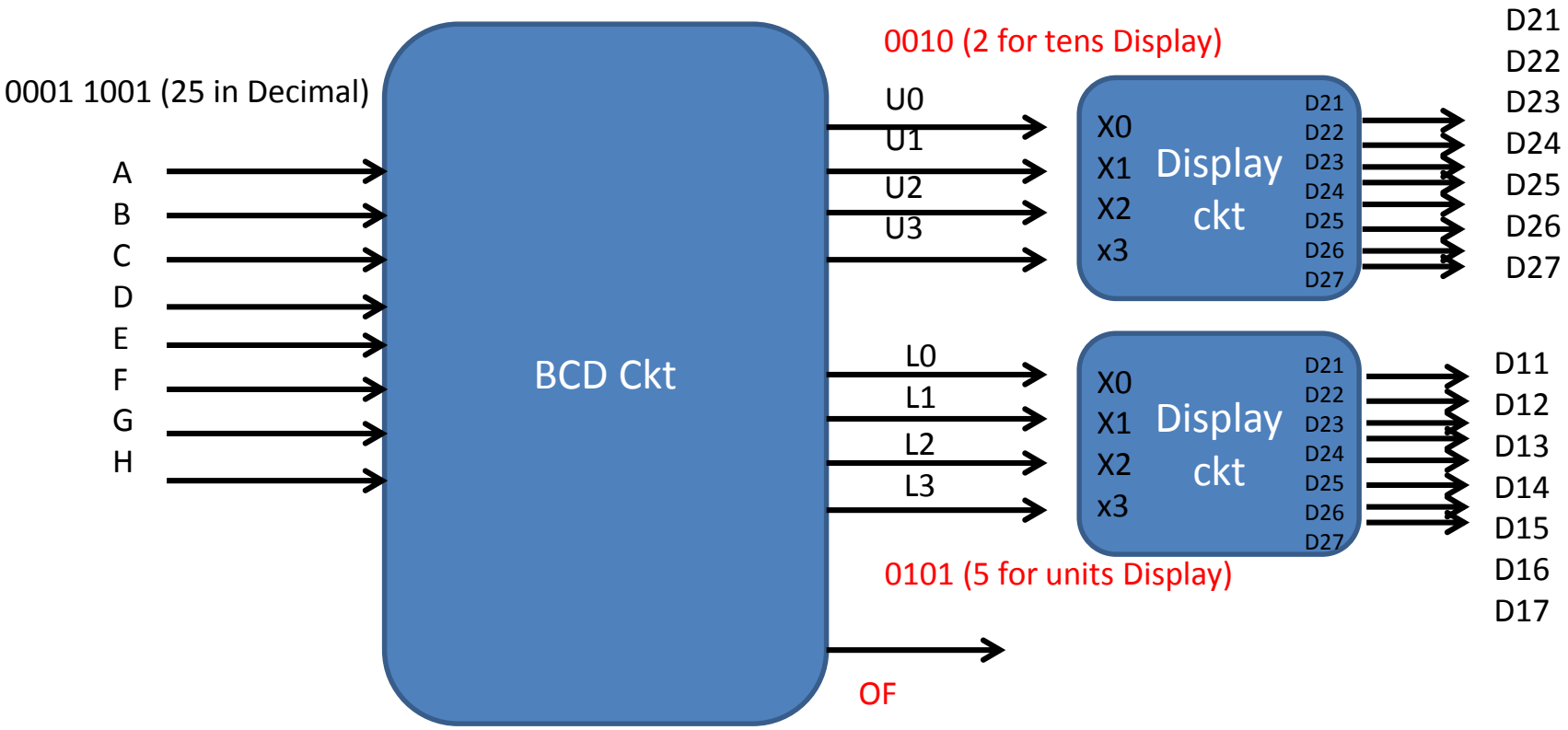
		BCD								Binary							
	OF	U3U2U1U0				L3L2L1L0											
		0	0	0	0	0	0	0	0	H	G	F	E	D	C	B	A
Shift 1		0	0	0	0	0	0	0	H	G	F	E	D	C	B	A	
Shift 2		0	0	0	0	0	0	H	G	F	E	D	C	B	A		
Shift 3		0	0	0	0	0	H	G	F	E	D	C	B	A			
		If 0HGF > 5, I H1 G1 F1= 0HGF + 0011															
		0	0	0	0	I	H1	G1	F1	E	D	C	B	A			
Shift 4		0	0	0	I	H1	G1	F1	E	D	C	B	A				
		If H1 G1 F1 E > 5, H2 G2 F2 E1 = H1 G1 F1 E + 0011															
		0	0	0	I	H2	G2	F2	E1	D	C	B	A				
Shift 5		0	0	I	H2	G2	F2	E1	D	C	B	A					
		If G2 F2 E1 D> 5, G3 F3 E2 D1= G2 F2 E1 D + 0011															
		0	0	I	H2	G3	G3	E2	D1	C	B	A					
Shift 6		0	I	H2	G3	F3	E2	D1	C	B	A						
		If I H2 G3 > 5, J I1 H3 G4 =I H2 G3 + 0011 If F3 E2 D1 C> 5, F4 E3 D3 C1= F3 E3 D1 C+ 0011															
		J	I1	H3	G4	F4	E3	D2	C1	B	A						
Shift 7		I1	H3	G4	F4	E3	D2	C1	B	A							
		If I1 H3 G4 F4 > 5, I2 H4 G5 F5 = I1 H3 G4 F4 + 0011 If E3 D2 C1 B > 5, E4 D3 C2 B1 = E3 D2 C1 B + 0011															
		I2	H4	G5	F5	E4	D3	C2	B1	A							
Shift 8	I2	H4	G5	F5	E4	D3	C2	B1	A								

BCD Alg

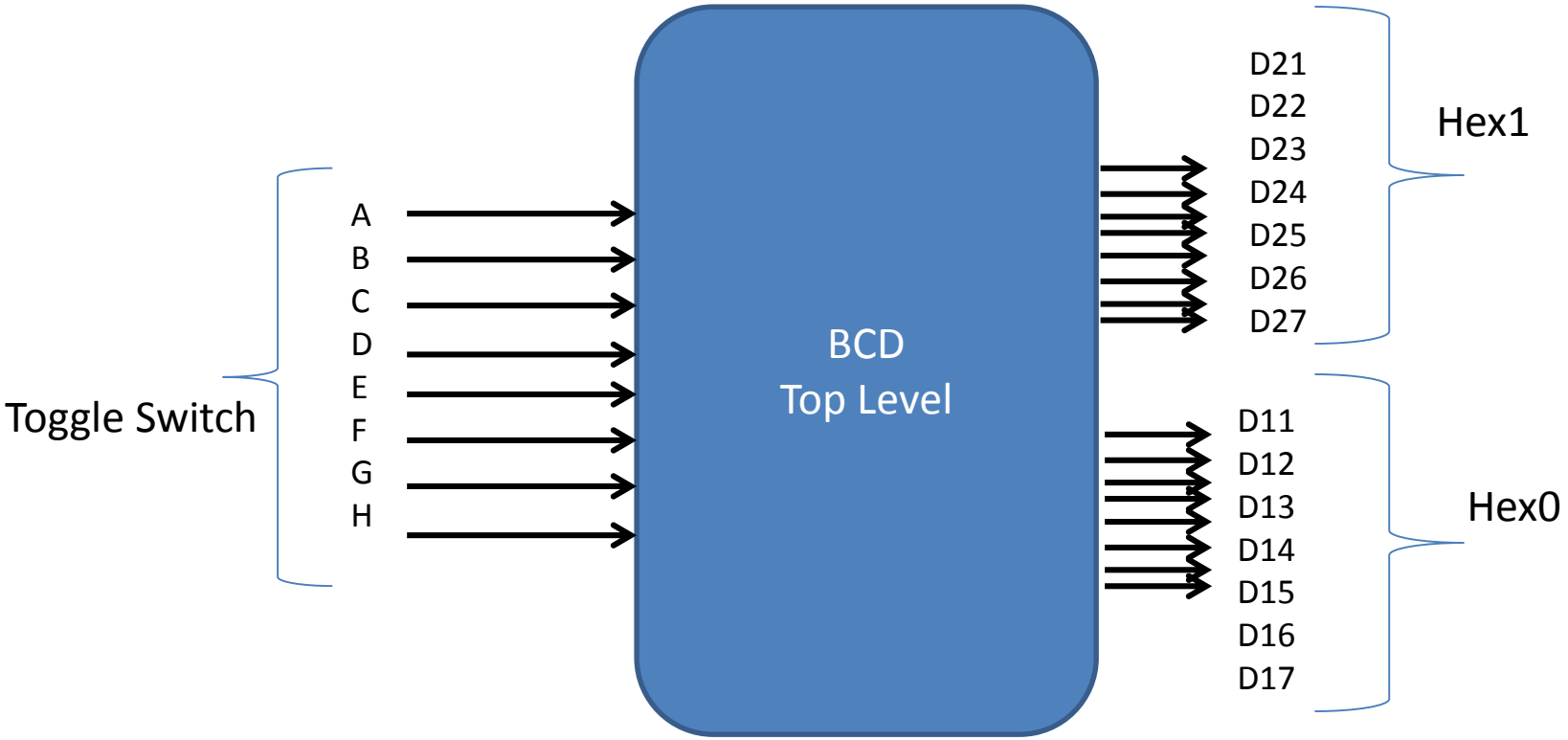


Ignore QD here!!!

BCD Circuit Block Diagram



BCD TopLevel



Simulation and Downloading

- Simulation Waveform for Counter and 8 bit Shift Register.
- Download BCD Ckt to DE 2 Board.