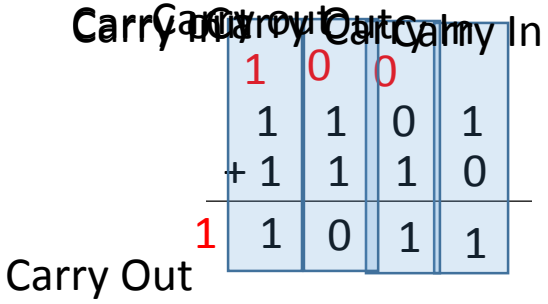
LAB-3 4 Bit Adder

Deliverables:

- Implement a one bit full adder with carry in and carry out pin using Quartus II Schematic Block.
- Connect 4 one-bit full adder in series to get a 4-bit full adder.
- Compilation and Simulation on Quartus II
- Combine the 4 bit full adder with the 7 segment display and test it on DE2 Board.

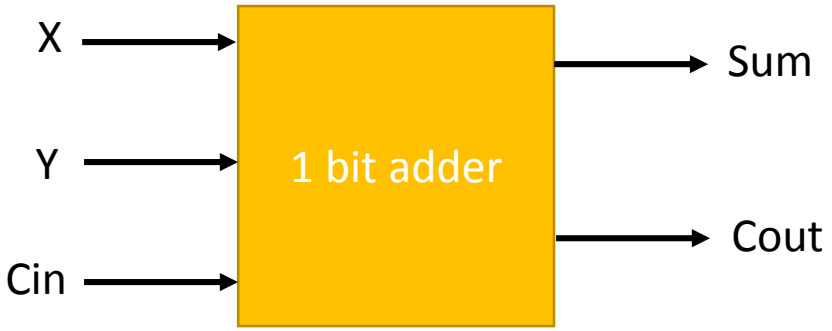
Binary Addition

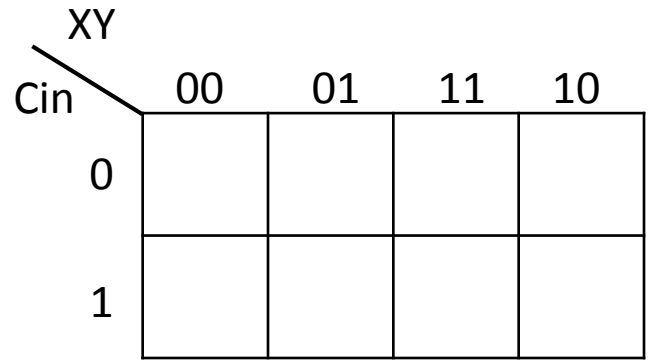
- Binary 1 bit addition
  - 0 + 0 = 0
  - 1 + 0 = 1
  - 0 + 1 = 1
  - 1 + 1 = 0 with carry out of 1.
- When implement adder using logic gates, we need to add the carry input (from the previous bit) and carry out output. Eg.



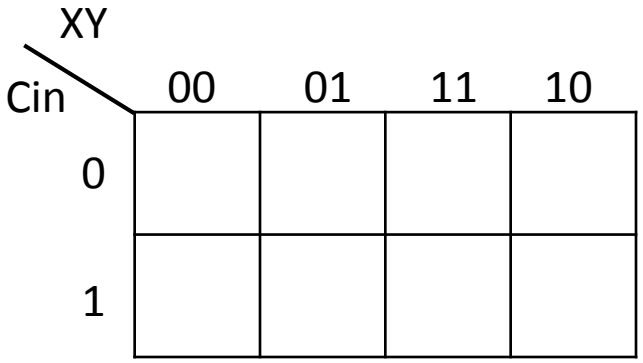
1 Bit Full Adder

X	Y	Cin	Sum	Cout
0	0	0	0	0
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		





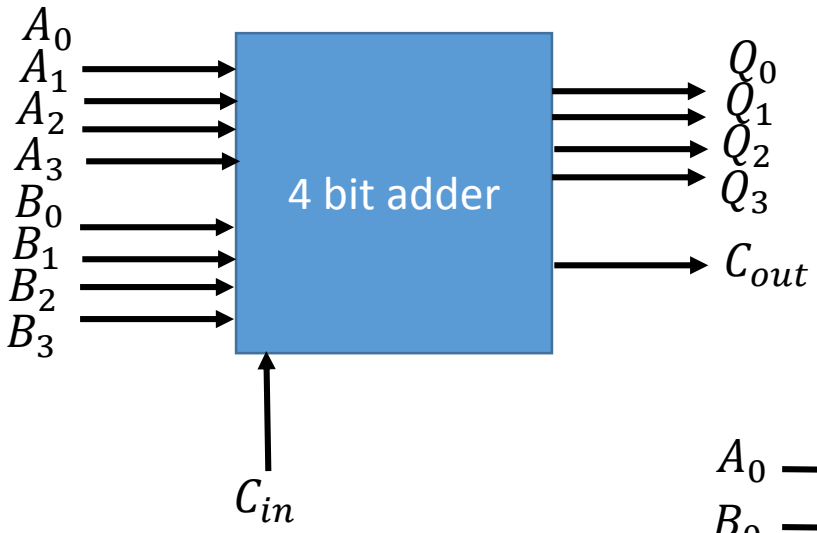
$Sum = ????$



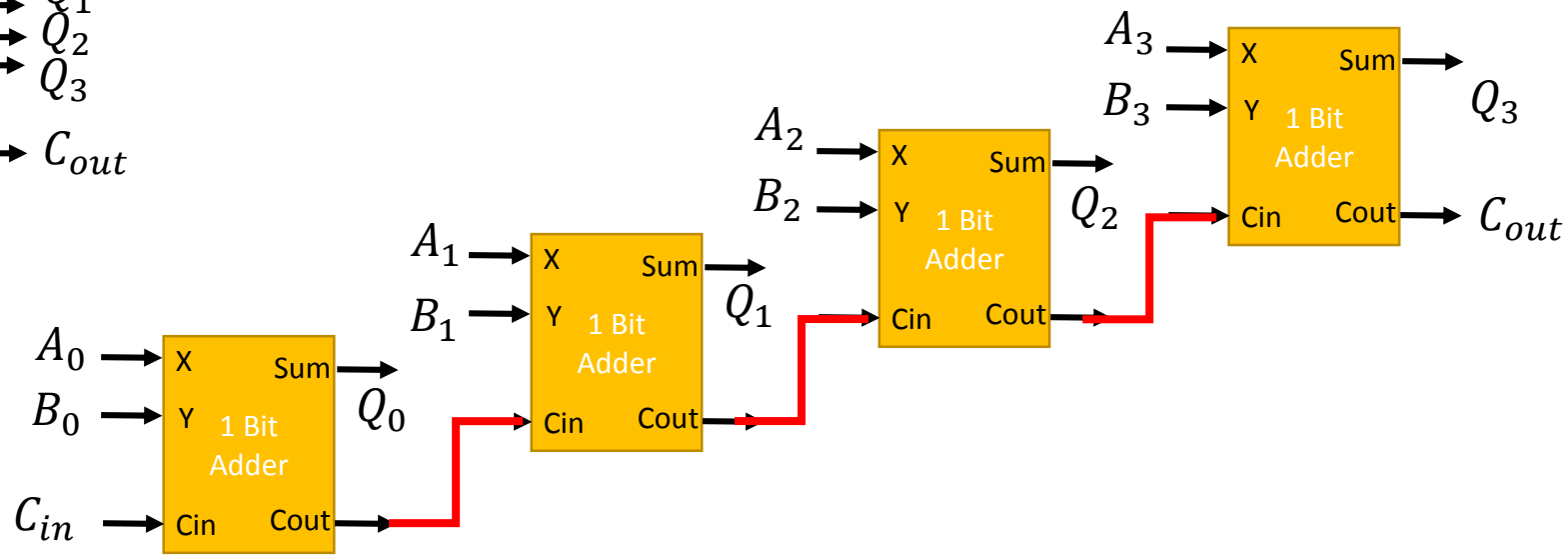
$Cout = ????$

4 Bit Adder

- Block diagram of a 4 bit adder .

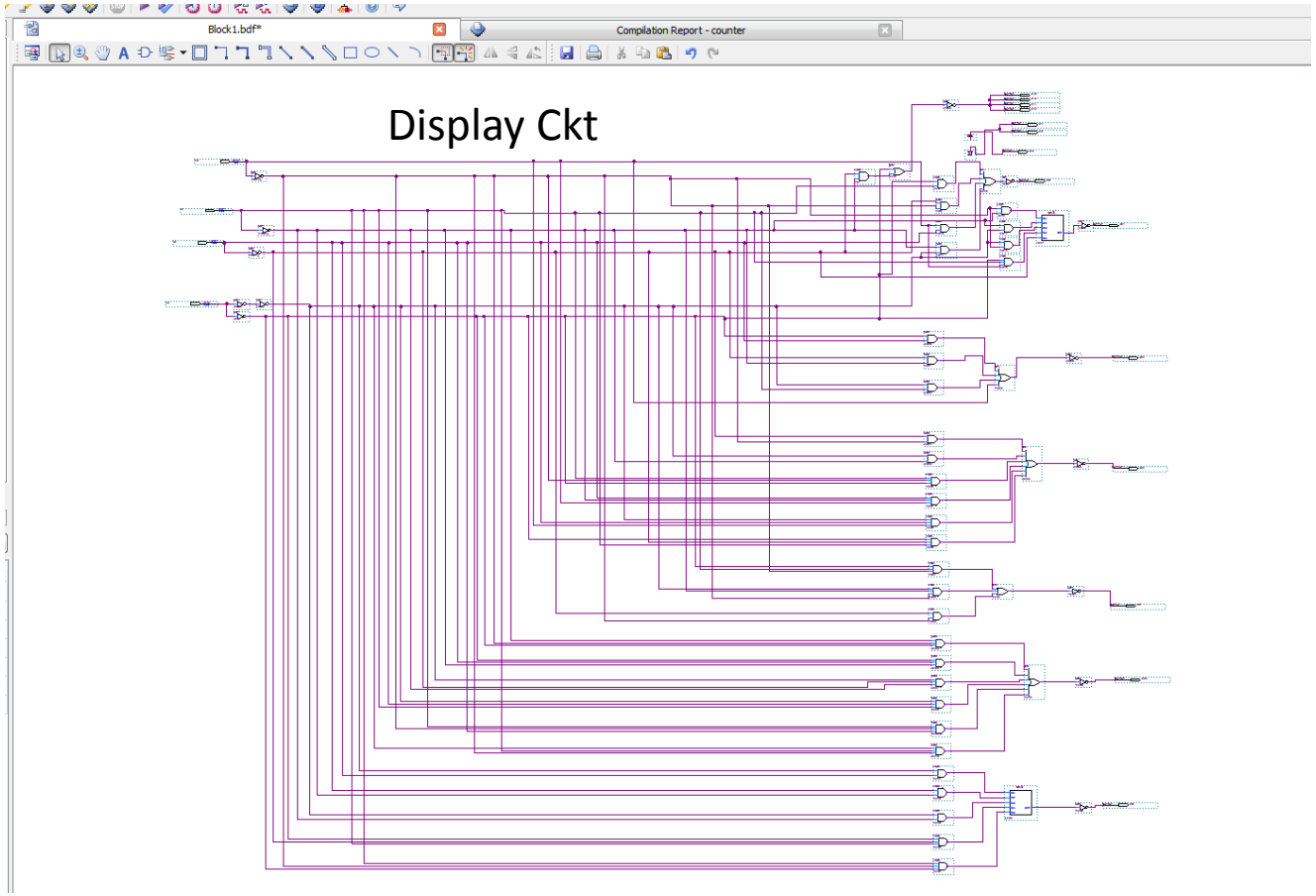


- Four 1 bit adder in series to get a 4 bit adder.



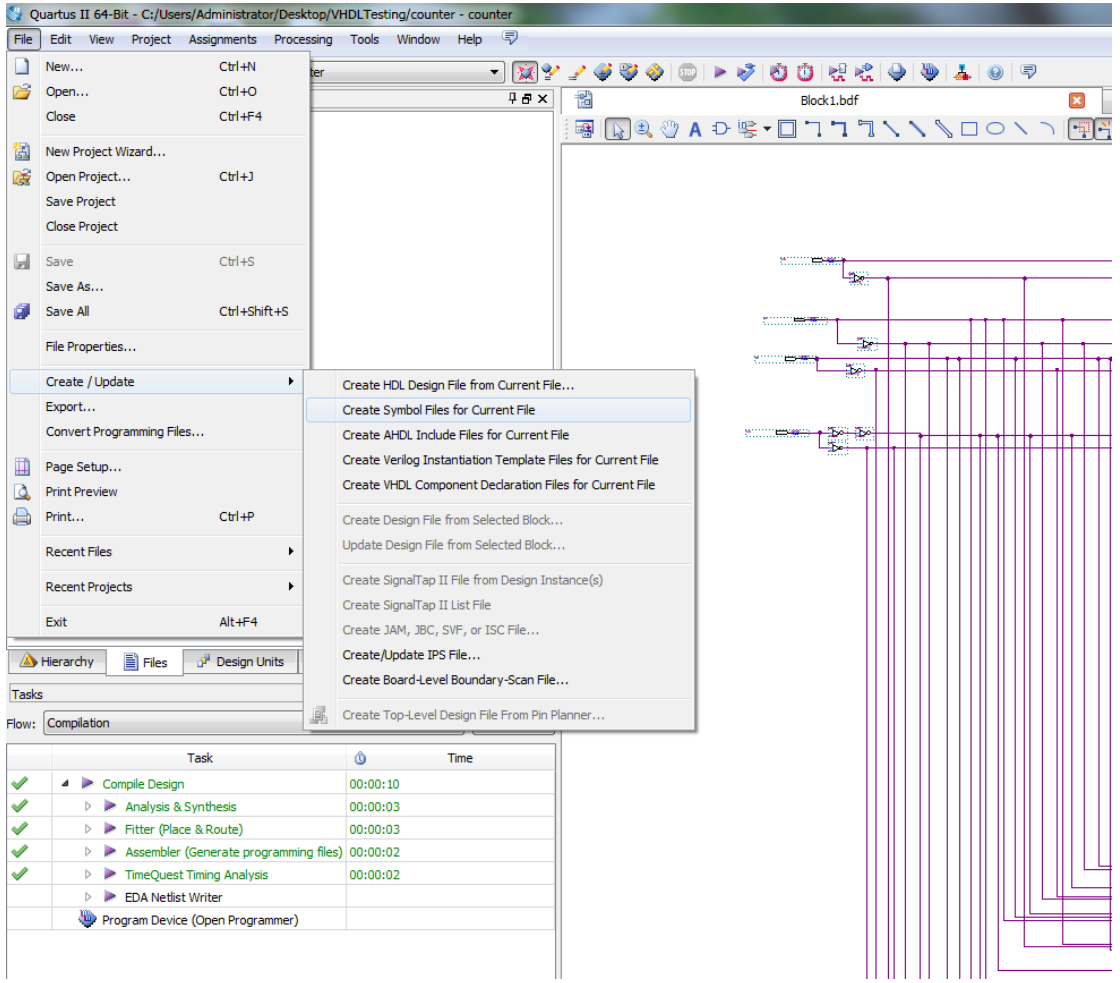
Creating a symbol block

- We can reuse the previous ckt in a new project instead of inserting the whole ckt.
- we can create the existing ckt to a symbol block and adding in other project as a block.



Creating a symbol block

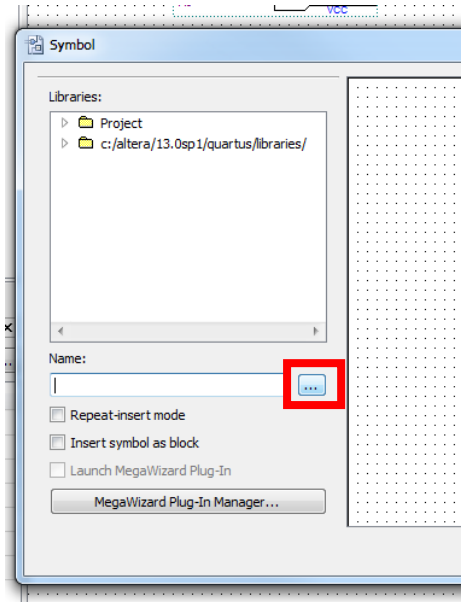
- File -> Create/Update -> Create Symbol Files for current file
- save the symbol file in your project folder. This will create a .bsf file.



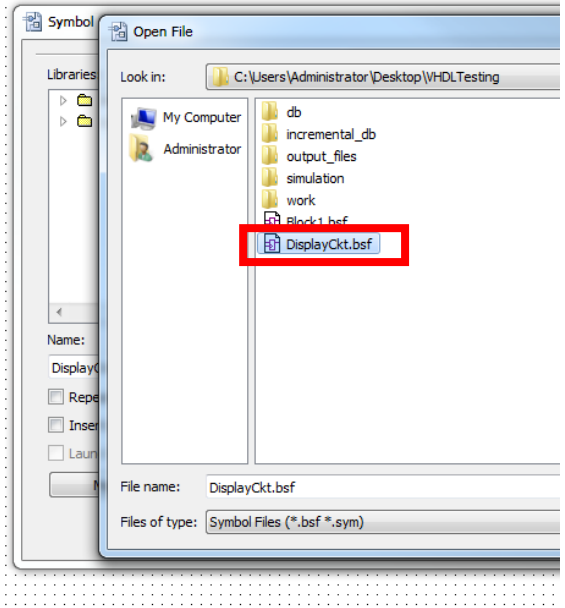
Adding Existing Ckt as a symbol to new project.

- Create a new Schematic Block file and Open Symbol window from Right Click-> Insert -> Symbol.

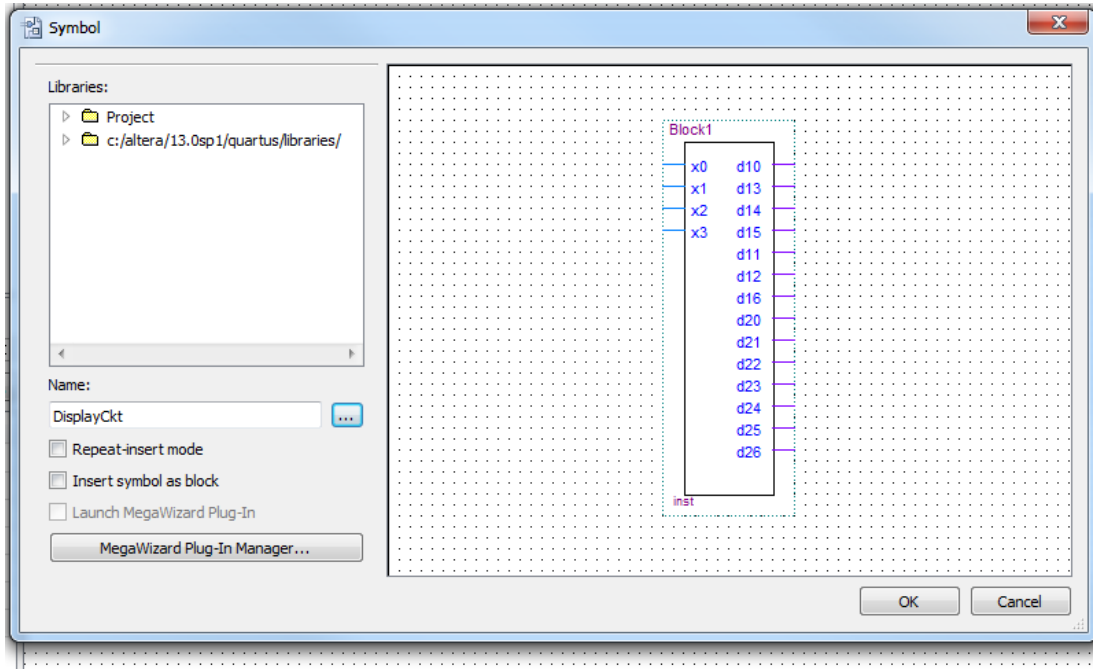
1.



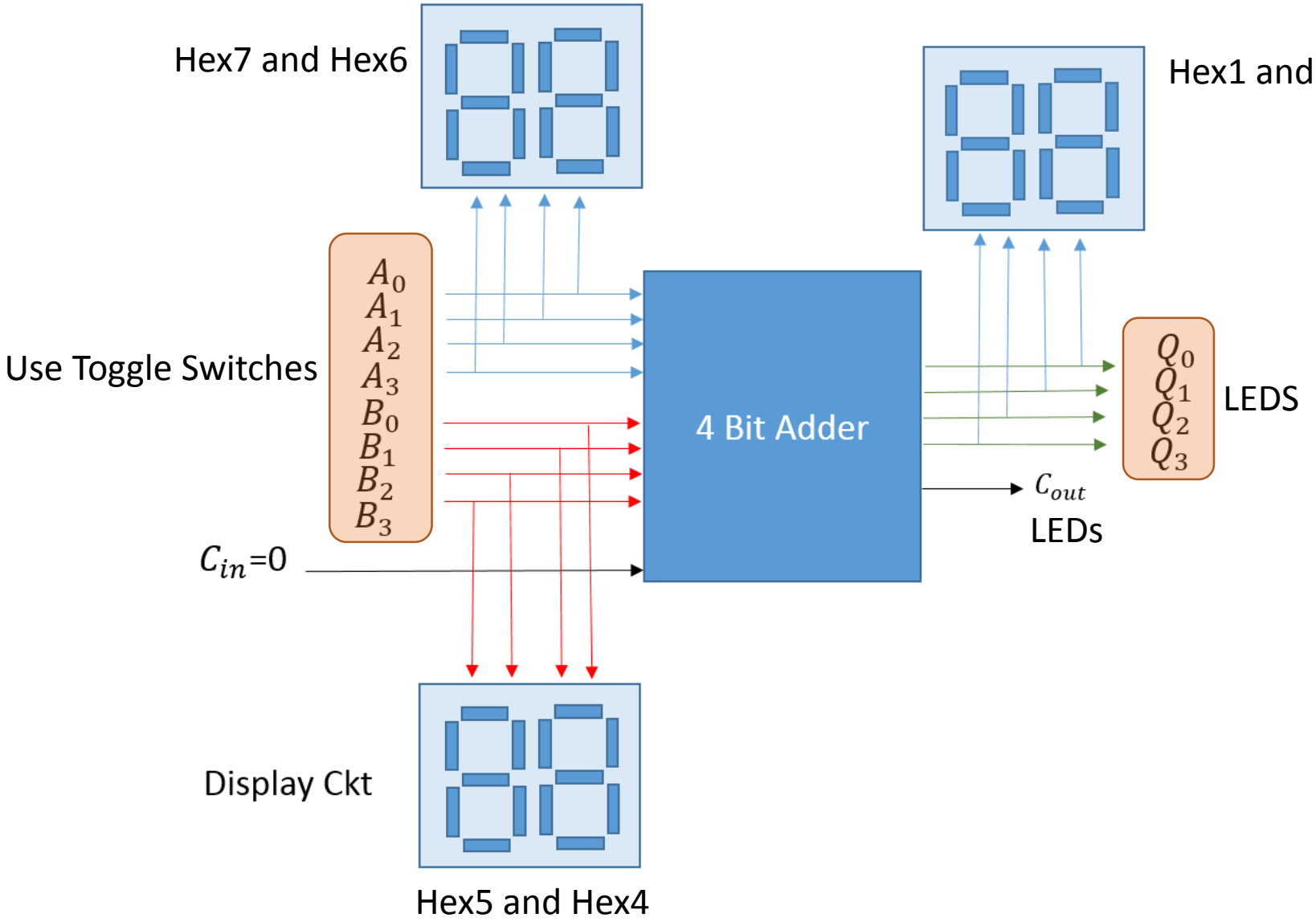
2. Select the desired .bsf file.



3. Eg. Display Ckt as a symbol block

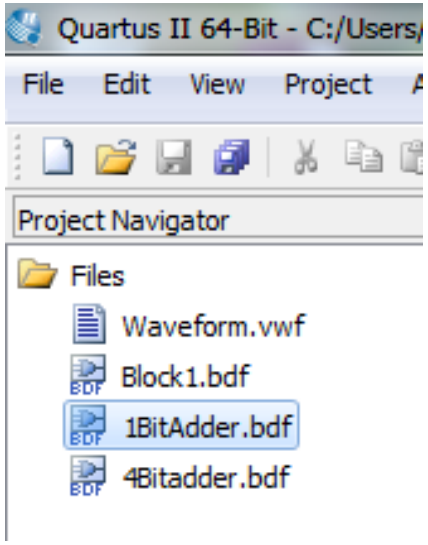


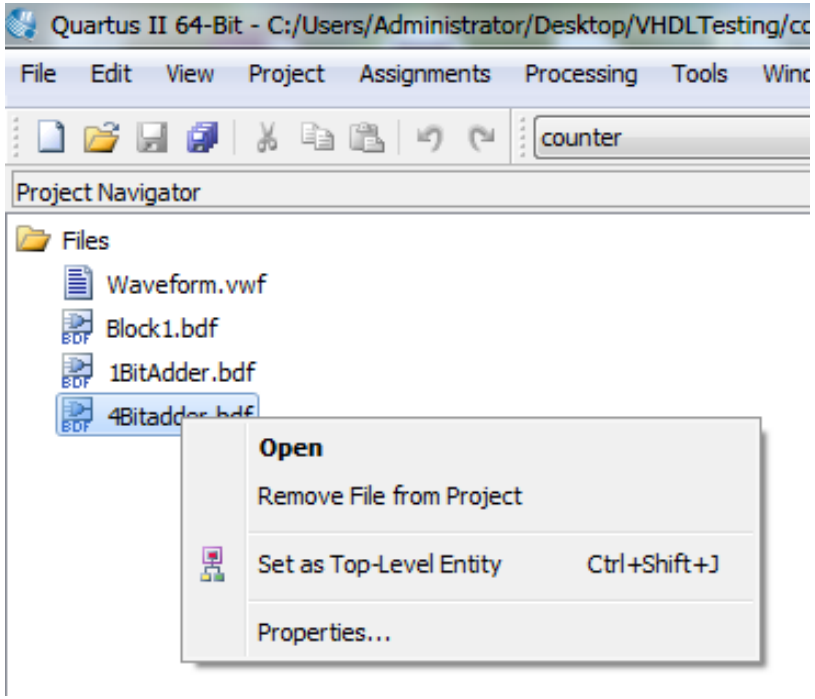
Toplevel Ckt - 4 Bit Adder and Display Ckt



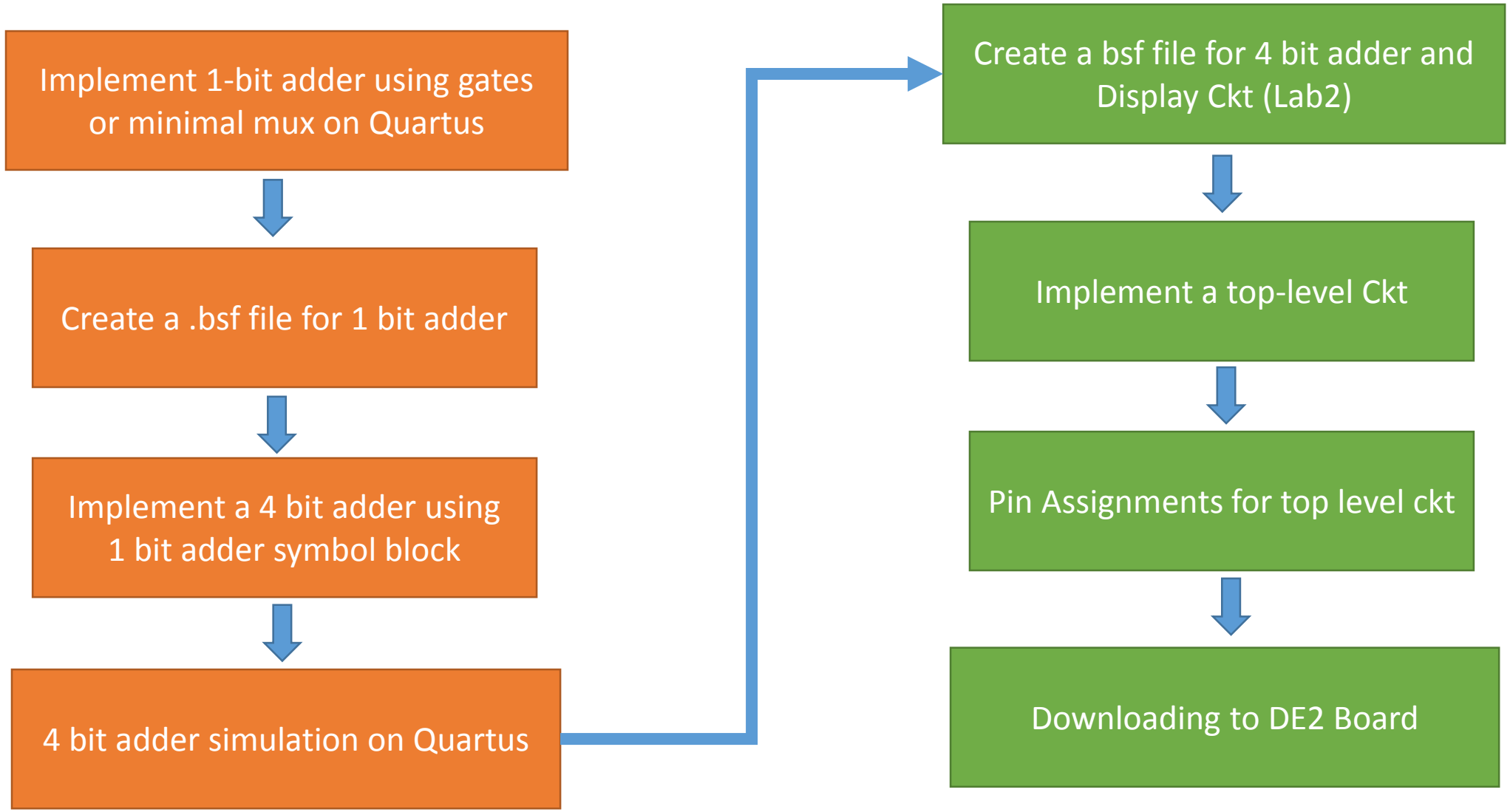
Compilation and Simulation

- When you have multiple .bdf files and to simulate a specific file.
- Right Click on the file you want to simulate and
- Select "Set as Top-Level Entity" and Compile.





Lab Implementation Flow Chart



DE 2 Pin Table

Signal Name	FPGA Pin No.
SW[0]	PIN_N25
SW[1]	PIN_N26
SW[2]	PIN_P25
SW[3]	PIN_AE14
SW[4]	PIN_AF14
SW[5]	PIN_AD13
SW[6]	PIN_AC13
SW[7]	PIN_C13
SW[8]	PIN_B13
SW[9]	PIN_A13
SW[10]	PIN_N1
SW[11]	PIN_P1
SW[12]	PIN_P2
SW[13]	PIN_T7
SW[14]	PIN_U3
SW[15]	PIN_U4
SW[16]	PIN_V1
SW[17]	PIN_V2

Signal Name	FPGA Pin No.
LEDR[0]	PIN_AE23
LEDR[1]	PIN_AF23
LEDR[2]	PIN_AB21
LEDR[3]	PIN_AC22
LEDR[4]	PIN_AD22
LEDR[5]	PIN_AD23
LEDR[6]	PIN_AD21
LEDR[7]	PIN_AC21
LEDR[8]	PIN_AA14
LEDR[9]	PIN_Y13
LEDR[10]	PIN_AA13
LEDR[11]	PIN_AC14
LEDR[12]	PIN_AD15
LEDR[13]	PIN_AE15
LEDR[14]	PIN_AF13
LEDR[15]	PIN_AE13
LEDR[16]	PIN_AE12
LEDR[17]	PIN_AD12
LEDG[0]	PIN_AE22
LEDG[1]	PIN_AF22
LEDG[2]	PIN_W19
LEDG[3]	PIN_V18
LEDG[4]	PIN_U18
LEDG[5]	PIN_U17
LEDG[6]	PIN_AA20
LEDG[7]	PIN_Y18
LEDG[8]	PIN_Y12

7 Segment Pin Table

HEX0[0]	PIN_AF10
HEX0[1]	PIN_AB12
HEX0[2]	PIN_AC12
HEX0[3]	PIN_AD11
HEX0[4]	PIN_AE11
HEX0[5]	PIN_V14
HEX0[6]	PIN_V13
HEX1[0]	PIN_V20
HEX1[1]	PIN_V21
HEX1[2]	PIN_W21
HEX1[3]	PIN_Y22
HEX1[4]	PIN_AA24
HEX1[5]	PIN_AA23
HEX1[6]	PIN_AB24
HEX2[0]	PIN_AB23
HEX2[1]	PIN_V22
HEX2[2]	PIN_AC25
HEX2[3]	PIN_AC26
HEX2[4]	PIN_AB26
HEX2[5]	PIN_AB25
HEX2[6]	PIN_Y24

HEX3[0]	PIN_Y23
HEX3[1]	PIN_AA25
HEX3[2]	PIN_AA26
HEX3[3]	PIN_Y26
HEX3[4]	PIN_Y25
HEX3[5]	PIN_U22
HEX3[6]	PIN_W24

HEX4[0]	PIN_U9
HEX4[1]	PIN_U1
HEX4[2]	PIN_U2
HEX4[3]	PIN_T4
HEX4[4]	PIN_R7
HEX4[5]	PIN_R6
HEX4[6]	PIN_T3
HEX5[0]	PIN_T2
HEX5[1]	PIN_P6
HEX5[2]	PIN_P7
HEX5[3]	PIN_T9
HEX5[4]	PIN_R5
HEX5[5]	PIN_R4
HEX5[6]	PIN_R3
HEX6[0]	PIN_R2
HEX6[1]	PIN_P4
HEX6[2]	PIN_P3
HEX6[3]	PIN_M2
HEX6[4]	PIN_M3
HEX6[5]	PIN_M5
HEX6[6]	PIN_M4

HEX7[0]	PIN_L3
HEX7[1]	PIN_L2
HEX7[2]	PIN_L9
HEX7[3]	PIN_L6
HEX7[4]	PIN_L7
HEX7[5]	PIN_P9
HEX7[6]	PIN_N9

Grading

	Implementation	Report	Final Grade	Remark
Lab 1	7.5%	7.5%	**15%**	
Lab 2- Display Ckt	7.5%	7.5%	**15%**	
Lab 3- 4 Bit Adder	7.5%	7.5%	**15%**	
Lab 4 -4 Bit Substractor	7.5%	7.5%	**15%**	
Lab 5 – 4 Bit Multiplier	7.5%	7.5%	**15%**	
Final Presentation	7.5%	7.5%	**10%**	
Test 1			**15%**	
Total			100%	