Digital Design Lab
ECN 315

Lab/Project
Lab 2 - 14 Segment Display

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Abstract

- The purpose of this lab was to create two seven segment displays that converted a four bit binary input into a visual representation of a decimal number — using boolean algebra and k-maps. In other words, we had to create a circuit that converted a four binary input into a fourteen binary output. These fourteen outputs would represent a decimal number between zero and fifteen.
- This project serves as a precursor to the four bit adder. Allowing us to see more clearly the output of our additions. Over all this lab was important because it teaches students an efficient way of representing 4 bit binary numbers in decimal. While also serving as an introduction to the Quartus 2 program.
- This lab resulted in us being able to program the inputs and outputs of the training board to create the 14 segment display.
- Overall this lab served as a good introduction to the Altera University Program and reinforce underlying logic design concepts.

Table of Contents

Overview

Seven segment displays are a simple method for converting binary numbers into decimal numbers. The output of the seven segment display is displayed visually as a decimal number that users can recognize. Having the ability to implement the seven segment displays is a useful skill for a logic designer. As they prove to be invaluable in its commercial applications.

Objectives

The main objective was to implement a circuit that displays the decimal number (0 to 15) on two 7 segment displays from 4 bit binary input. The displays can display the integer by simply turning on and off the desired LEDS.

Equipment

Description:
Quartus II software
EP2C35F672C6 University Program board
Windows 7

Description

In order to design the circuit we fist had to understand how the circuit worked. We started by looking at the total number of outputs that our circuit could generate given our inputs. Since we had four inputs and fourteen different outputs, we implemented the truth table for the two seven segment displays. We the used the truth tables to generate K-maps that would simplify our outputs equations. We decided to make our own 4 to 16 decoder to implement the circuit. This was useful because decoders are readily available and an industry standard.

Specifications

We were allowed to use multiplexers and logic gates to implement our circuit.

Design Synthesis Or VHDL Code

A	B	C	D		d0	d1	d2	d3	d4	d5	d6	d7	d8	d9	d10	d11	d12	d13
0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	1	1	0	1	1	0	1	0	0	0	0	0	0	0
0	0	1	1	3	1	1	1	1	0	0	1	0	0	0	0	0	0	0
0	1	0	0	4	0	1	1	0	0	1	1	0	0	0	0	0	0	0
0	1	0	1	5	1	0	1	1	0	1	1	0	0	0	0	0	0	0
0	1	1	0	6	1	0	1	1	1	1	1	0	0	0	0	0	0	0
0	1	1	1	7	1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	8	1	1	1	1	1	1	1	0	0	0	0	0	0	0
1	0	0	1	9	1	1	1	0	0	1	1	0	0	0	0	0	0	0
1	0	1	0	10	1	1	1	1	1	1	0	0	1	1	0	0	0	0
1	0	1	1	11	0	1	1	0	0	0	0	0	1	1	0	0	0	0
1	1	0	0	12	1	1	0	1	1	0	1	0	1	1	0	0	0	0
1	1	0	1	13	1	1	1	1	0	0	1	0	1	1	0	0	0	0
1	1	1	0	14	0	1	1	0	0	1	1	0	1	1	0	0	0	0
1	1	1	1	15	1	0	1	1	0	1	1	0	1	1	0	0	0	0

Figure 1. Truth Table

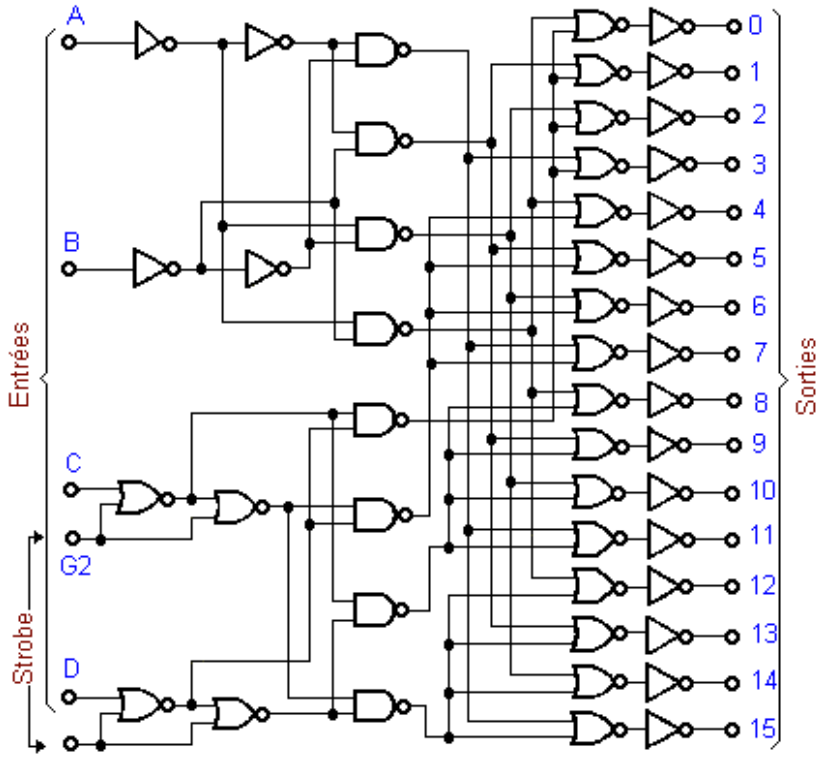

Figure 2. 4:16 Decoder

Complete Logic Diagram

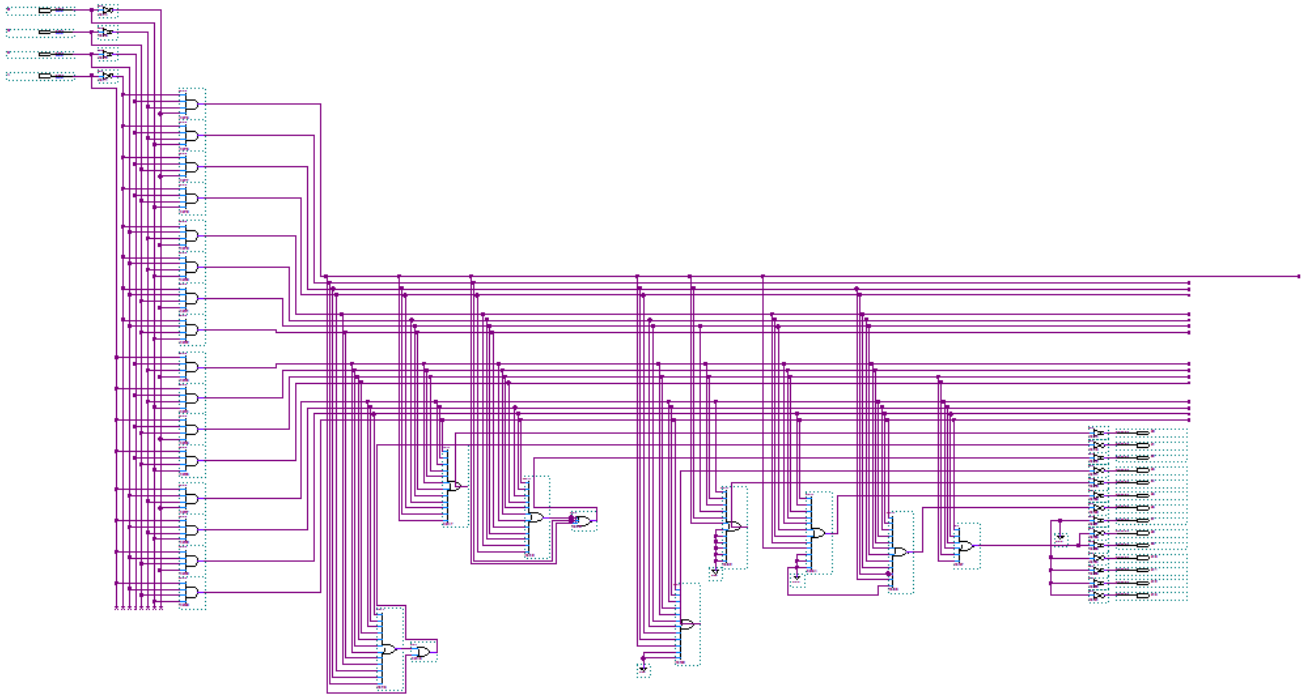

Figure 3. Seven segment display with Decoder

Results and Simulations

After debugging our circuit numerous times, we decided to build a decoder from which we can use to build our seven segment display. We decided to us the min terms since the input of the seven segment display on the board is reversed. After bring all of the outputs together, we obtained our output equations. Figure 1, represents the truth table for this lab. It serves as a guide for our project, allowing us to view how our boolean algebra should be implemented. Figure 2 is a picture of a sixteen to one decoder. Finally, Figure 3 is the final circuit for our seven segment display.

Conclusion

a. The main objective was to implement a circuit that displays the decimal number (0 to 15) on two 7 segment displays from 4 bit binary input. In order to implement the circuit we had to use boolean algebra. We started by creating a truth table with all of the possible outcomes of our circuit. Once that was done, we used a four to sixteen decoder to represent our min terms, passing them through an or gate — generating our output equations for our 14 segment display.
b. We encountered many problems with our design. Our first attempt at creating the display resulted in failure. We tried to implement the circuit using eight to one multiplexers and using k-maps to determine the input and select line equations, but it never worked. For this reason, we opted to create a decoder to simplify the process. This made it a lot easier to finalize our circuit.

c. The main limitation our segment has, is that its input is restricted to only four bits. This means that the largest number that can be represented by the display is fifteen. Having two displays could theoretically display decimal numbers up to the number ninety-nine.
d. We learned how to use the Quartus II and Altera University Program. We also learned how to create a decoder using boolean algebra and use it to implement a seven segment display. One of the greatest advantages in creating a seven segment display is that it converts binary numbers to a visual representation of decimal numbers efficiently. There are many applications where this is advantageous. This lab proved to be a useful learning experience.

Works Cited

https://www.courses.miami.edu/bbcswebdav/pid-7417271-dt-content-rid-10888994_1/courses/ECE315-E1-05939-1-20171/LAB%202%20QuartusII.pdf

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