STEPS:

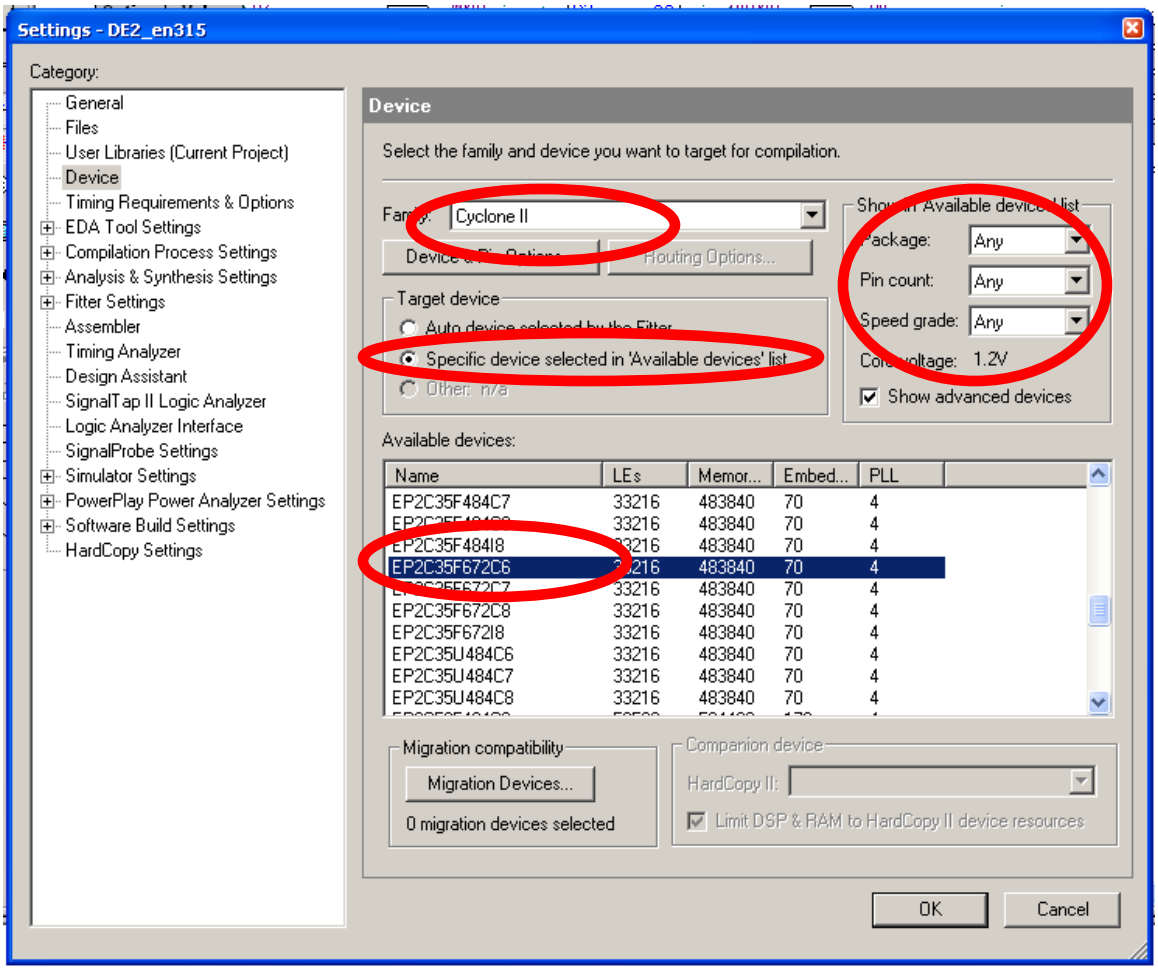
1. Connect the board:
    - make sure that the RUN/PROG switch located to the left of the LCD display is in RUN position. As a matter of fact, that switch must **always** be in RUN, so never change it.
    - Connect 9V power supply to the board.
    - Connect a USB cable to the USB port labeled **BLASTER** to any USB port on the computer. ***Make sure that you do not make a very common mistake by connecting to the USB port labeled DEVICE!***
    - **Only 32-bit PCs have the driver for the board, make sure you are NOT sitting at a 64-bit PC!**
    - Turn on the board power by pressing the **red Power button** on the board. Whenever you are downloading to the Cyclone II using the method described in this tutorial, your design is stored in Cyclone II FPGA temporarily – when you power off the board, the board will be reset.

    At this point, you should observe:

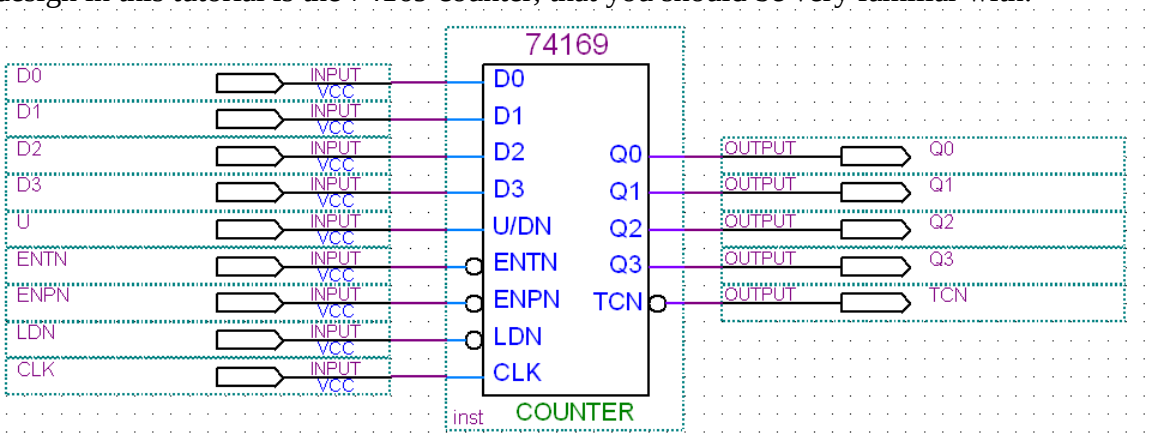
    - a default pattern on the board's LEDs,
    - a welcome message on the LCD,
    - "POWER" and "GOOD" LEDs (blue, above the LCD) on.

2. Compile your digital circuit for the device you will be downloading. In our tutorial, you will be downloading to the Cyclone II EP2C35F672C6 FPGA, on the DE2 board. If you current device is different, you must change it by going to **Assignments >> Settings**. In the **"Settings – your_project_name"** window that will appear, select the "Device" page, choose family "Cyclone II" and select the EP2C35F672C6 in the list of available devices. Make sure that:
    a. All drop-down boxes have "Any" in the **"Show in 'Available Devices' list"** box,
    b. **"Specific device selected in 'Available devices' list"** is selected.

    If you had to change your device, recompile so that the changes take effect.

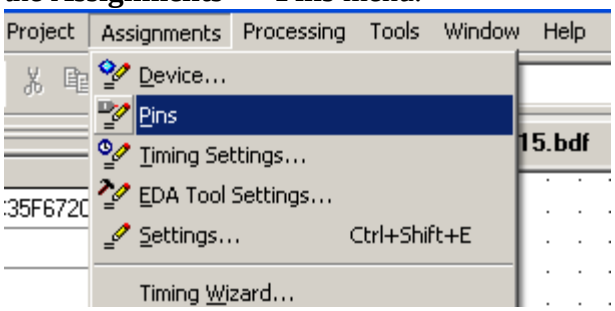


3. Now, we will assign the pins of our design to the pins of the FPGA device. The design in this tutorial is the 74169 counter, that you should be very familiar with:

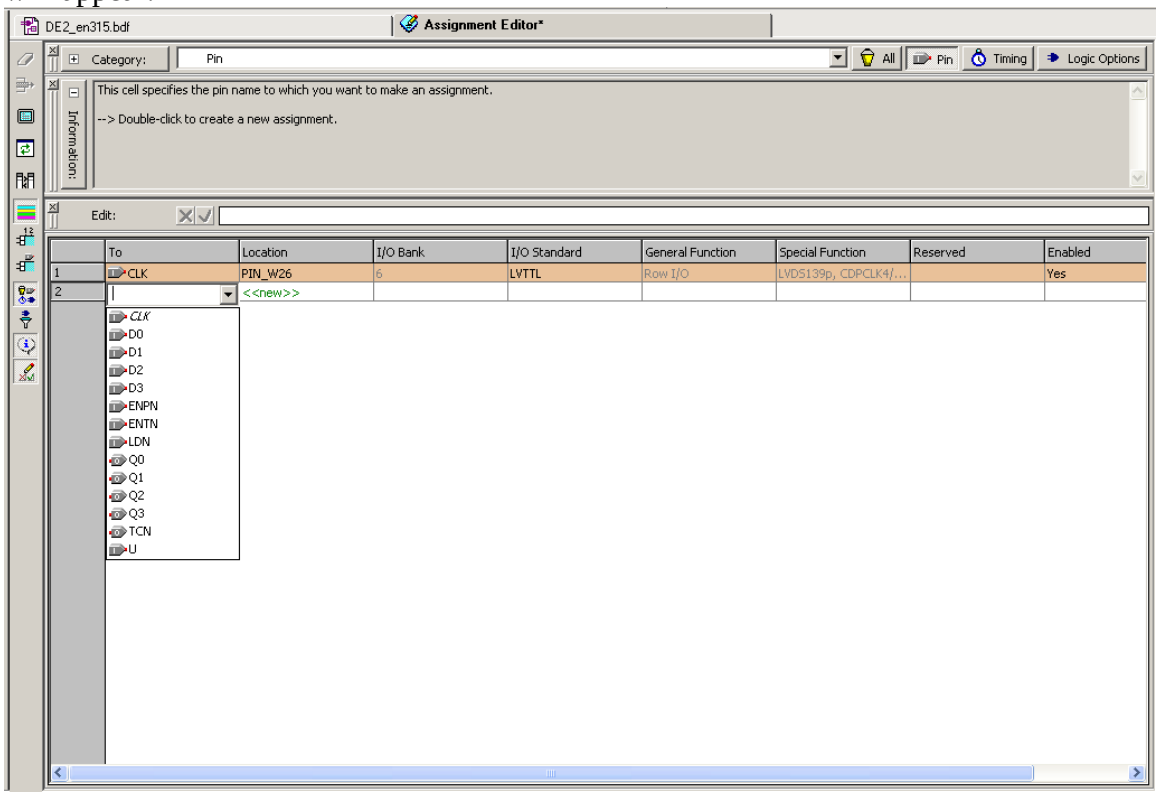


The Cyclone II device has hundreds of pins, most of which are connected to a variety of hardware of the board - switches, LEDs, push buttons, LCD display, VGA and Ethernet controllers, just to name a few (***refer to the back of this tutorial for the tables of pin assignments for switches, LEDs and pushbuttons***). We will use this hardware to implement our design. You must use your common

sense to decide what each single pin of your design must be connected to. For instance, it makes sense to connect output pins to the LEDs, so that we can see the output. It also makes sense to connect the clock of the counter to the pushbutton, and the input and controls to the switches. That is what we are going to do. Open the **Assignments >> Pins** menu.

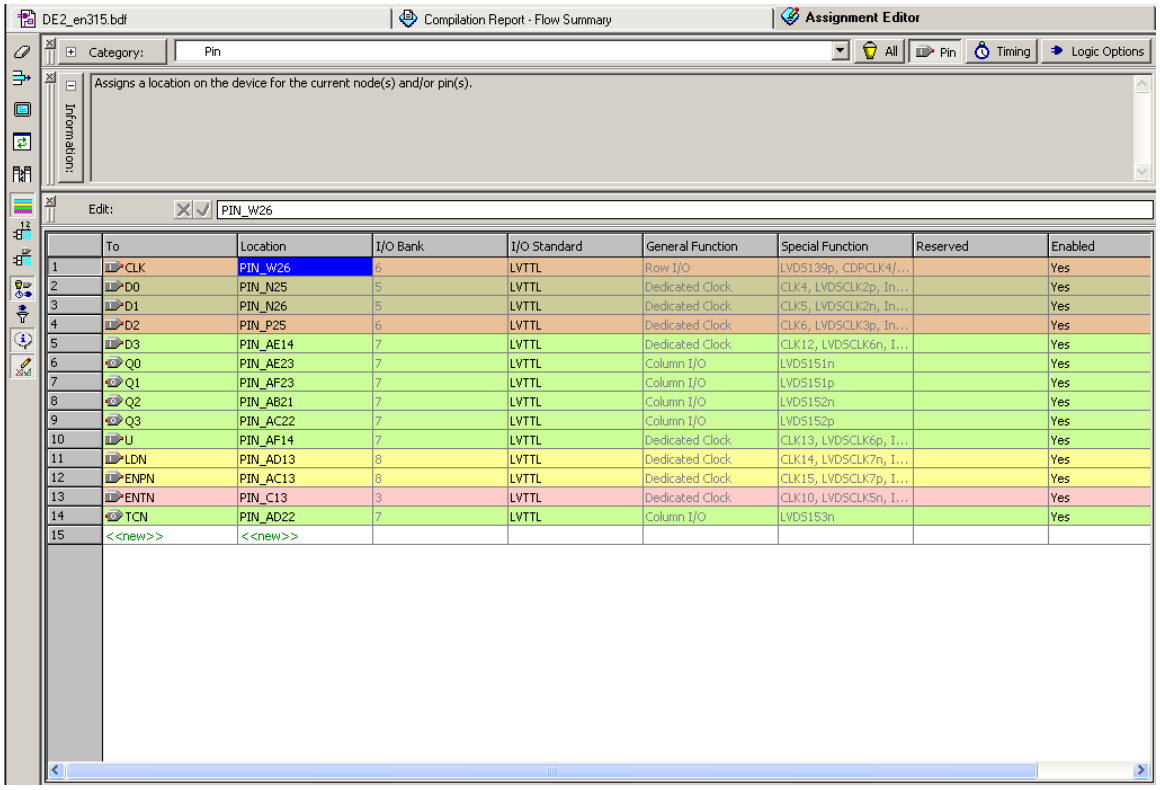


In the new window, you can assign your input and output pins to the pins of the FPGA you are programming. The "To" column will contain input/output pins of our design. The "Location" column will contain the pins of the device that we selected to represent each corresponding pin of our design. Double click on the empty cell of the "To" column, and the drop-down list with all input/output pins will appear.



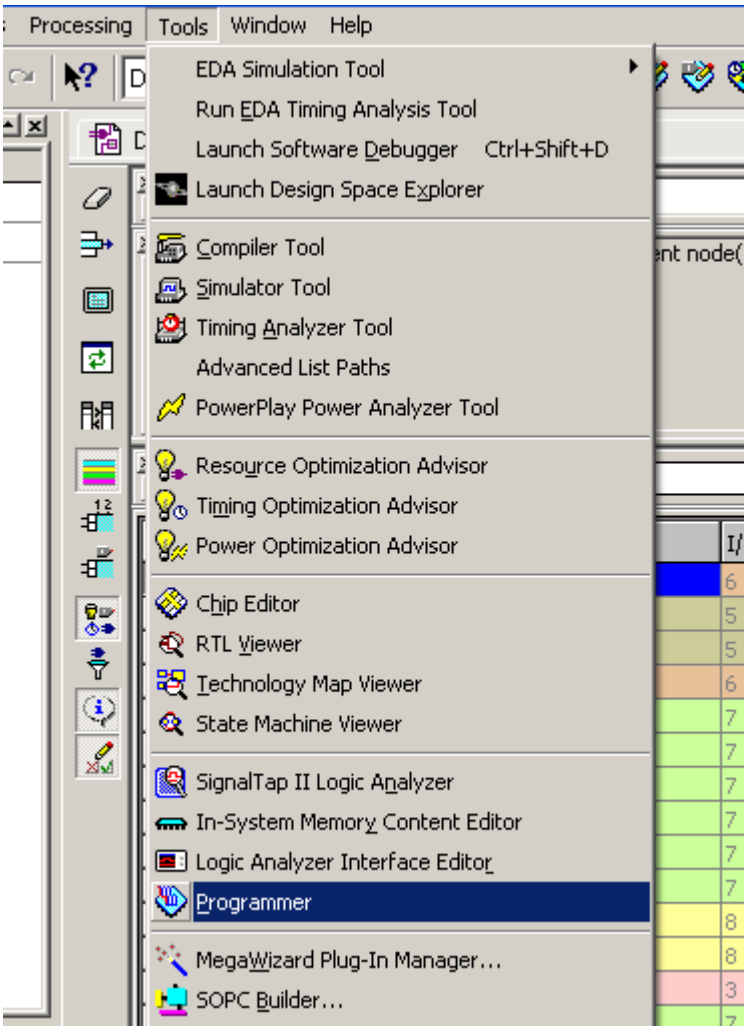
The pins that already have an assignment will be in italic font (as you can see, that is the case for CLK pin). You can select the pin by clicking, or you can also type in first letters of the pin name, and Quartus will automatically complete it for you. Pressing enter, will save that cell's entry and move you down to the next cell, which will be already selected and ready for input. Same applies for cells in "Location" column, with only difference being that the number of pins of the

Cyclone II device is in hundreds. In this column it saves time to type letters and number that identify the pin (ignore the “PIN_” prefix to pin names). For instance, to select “PIN_G1” just type “G1”. Ignore other columns and the text in them – that is beyond our tutorial.
How do you choose which device pin to assign your project pin to? Again, it is a question of function. In our project, we have five outputs, Q0 through Q3 and TCN (RCO inverted). It makes sense to see those outputs on LEDR0 through LEDR4, the red LEDs on the board above the switches. So, which pins of the Cyclone II device are these LEDs connected to? That information is contained in the back of this tutorial. You can also choose to refer to original board manual at http://www.altera.com/education/univ/materials/boards/DE2_UserManual.pdf
.
The same logic applies in case of inputs – all inputs, except for clock, are assigned to the Cyclone II pins that are hardwired to the switches. The clock is assigned to the pin of Cyclone II that is hardwired to one of the pushbuttons.
The completed pin assignments should look something like
this.



	To	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved	Enabled
1	CLK	PIN_W26	6	LVTTL	Row I/O	LVDS139p, CDPCLK4/...		Yes
2	D0	PIN_N25	5	LVTTL	Dedicated Clock	CLK4, LVDSCLK2p, In...		Yes
3	D1	PIN_N26	5	LVTTL	Dedicated Clock	CLK5, LVDSCLK2n, In...		Yes
4	D2	PIN_P25	6	LVTTL	Dedicated Clock	CLK6, LVDSCLK3p, In...		Yes
5	D3	PIN_AE14	7	LVTTL	Dedicated Clock	CLK12, LVDSCLK6n, I...		Yes
6	Q0	PIN_AE23	7	LVTTL	Column I/O	LVDS151n		Yes
7	Q1	PIN_AF23	7	LVTTL	Column I/O	LVDS151p		Yes
8	Q2	PIN_AB21	7	LVTTL	Column I/O	LVDS152n		Yes
9	Q3	PIN_AC22	7	LVTTL	Column I/O	LVDS152p		Yes
10	U	PIN_AF14	7	LVTTL	Dedicated Clock	CLK13, LVDSCLK6p, I...		Yes
11	LDN	PIN_AD13	8	LVTTL	Dedicated Clock	CLK14, LVDSCLK7n, I...		Yes
12	ENPN	PIN_AC13	8	LVTTL	Dedicated Clock	CLK15, LVDSCLK7p, I...		Yes
13	ENTN	PIN_C13	3	LVTTL	Dedicated Clock	CLK10, LVDSCLK5n, I...		Yes
14	TCN	PIN_AD22	7	LVTTL	Column I/O	LVDS153n		Yes
15	<<new>>	<<new>>						

4. Save the pin assignments and recompile the design again.
5. Now, we will download the design to the board. Go to **Tools >> Programmer**.



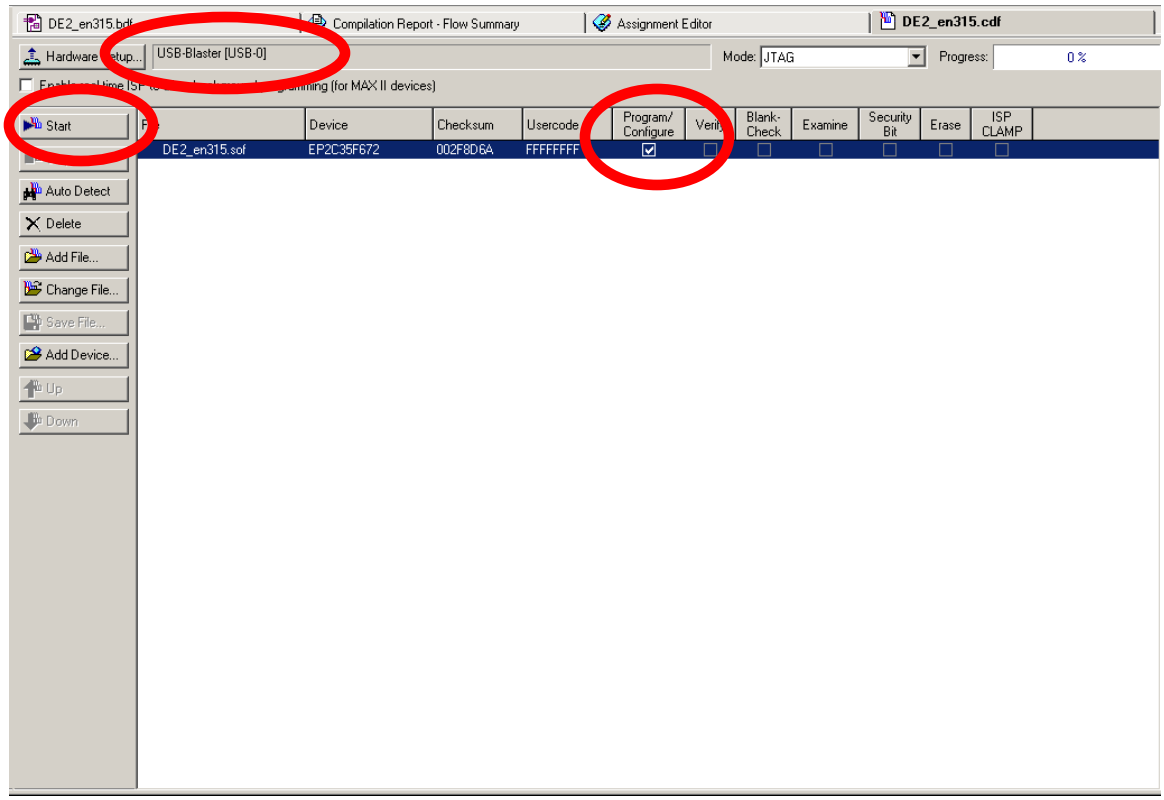
In the new window, make sure that:

a. The hardware selected is **"USB-Blaster"**, - if you see anything else, click on Hardware Setup, and choose USB-Blaster. If you connected the board to the computer and still do not see USB-Blaster as one of the options, **check to make sure that you connected the cable to the USB port labeled BLASTER.** The USB port labeled DEVICE should not be connected!

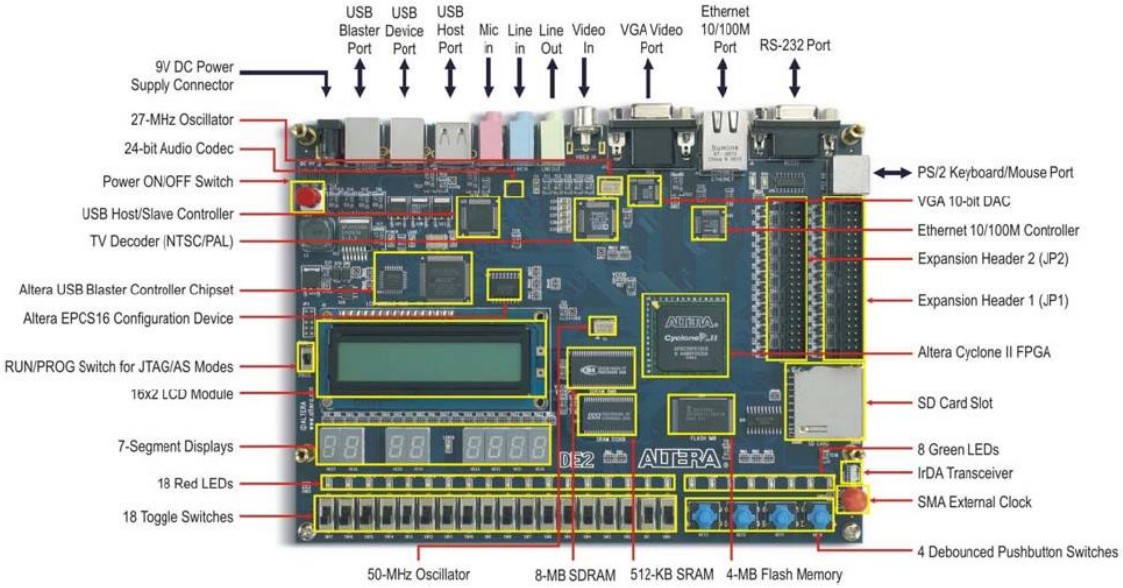
b. **"Program/Configure"** checkbox is selected.

Now, click START. When your design has finished downloading, you should observer that:

- "POWER" and "GOOD" LEDs are back on.



DE2 BOARD REFERENCE (original manual at http://www.altera.com/education/univ/materials/boards/DE2_UserManual.pdf):



Cyclone II 2C35 FPGA

- 33,216 LEs
- 105 M4K RAM blocks
- 483,840 total RAM bits
- 35 embedded multipliers
- 4 PLLs
- 475 user I/O pins
- FineLine BGA 672-pin package

Pushbutton switches

- 4 pushbutton switches
- Debounced by a Schmitt trigger circuit
- Normally high; generates one active-low pulse when the switch is pressed

Toggle switches

- 18 toggle switches for user inputs
- A switch causes logic 0 when in the DOWN (closest to the edge of the DE2 board) position and logic 1 when in the UP position

Clock inputs

- 50-MHz oscillator
- 27-MHz oscillator
- SMA external clock input

4.2 Using the LEDs and Switches

The DE2 board provides four pushbutton switches. Each of these switches is debounced using a Schmitt Trigger circuit, as indicated in Figure 4.3. The four outputs called *KEY0*, …, *KEY3* of the Schmitt Trigger device are connected directly to the Cyclone II FPGA. Each switch provides a high logic level (3.3 volts) when it is not pressed, and provides a low logic level (0 volts) when depressed. Since the pushbutton switches are debounced, they are appropriate for use as clock or reset inputs in a circuit.

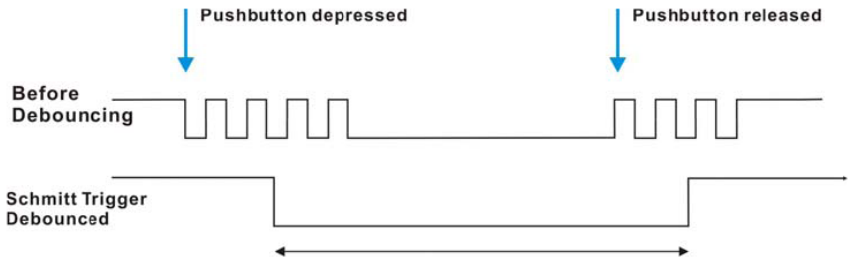


Figure 4.3. Switch debouncing.

There are also 18 toggle switches (sliders) on the DE2 board. These switches are not debounced, and are intended for use as level-sensitive data inputs to a circuit. Each switch is connected directly to a pin on the Cyclone II FPGA. When a switch is in the DOWN position (closest to the edge of the board) it provides a low logic level (0 volts) to the FPGA, and when the switch is in the UP position it provides a high logic level (3.3 volts).

There are 27 user-controllable LEDs on the DE2 board. Eighteen red LEDs are situated above the 18 toggle switches, and eight green LEDs are found above the pushbutton switches (the 9th green LED is in the middle of the 7-segment displays). Each LED is driven directly by a pin on the Cyclone II FPGA; driving its associated pin to a high logic level turns the LED on, and driving the pin low turns it off. A schematic diagram that shows the pushbutton and toggle switches is given in Figure 4.4. A schematic diagram that shows the LED circuitry appears in Figure 4.5.

Signal Name	FPGA Pin No.	Description
SW[0]	PIN_N25	Toggle Switch[0]
SW[1]	PIN_N26	Toggle Switch[1]
SW[2]	PIN_P25	Toggle Switch[2]
SW[3]	PIN_AE14	Toggle Switch[3]
SW[4]	PIN_AF14	Toggle Switch[4]
SW[5]	PIN_AD13	Toggle Switch[5]
SW[6]	PIN_AC13	Toggle Switch[6]
SW[7]	PIN_C13	Toggle Switch[7]
SW[8]	PIN_B13	Toggle Switch[8]
SW[9]	PIN_A13	Toggle Switch[9]
SW[10]	PIN_N1	Toggle Switch[10]
SW[11]	PIN_P1	Toggle Switch[11]
SW[12]	PIN_P2	Toggle Switch[12]
SW[13]	PIN_T7	Toggle Switch[13]
SW[14]	PIN_U3	Toggle Switch[14]
SW[15]	PIN_U4	Toggle Switch[15]
SW[16]	PIN_V1	Toggle Switch[16]
SW[17]	PIN_V2	Toggle Switch[17]

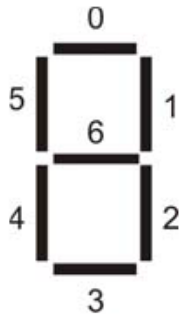
Signal Name	FPGA Pin No.	Description
KEY[0]	PIN_G26	Pushbutton[0]
KEY[1]	PIN_N23	Pushbutton[1]
KEY[2]	PIN_P23	Pushbutton[2]
KEY[3]	PIN_W26	Pushbutton[3]

Signal Name	FPGA Pin No.	Description
LEDR[0]	PIN_AE23	LED Red[0]
LEDR[1]	PIN_AF23	LED Red[1]
LEDR[2]	PIN_AB21	LED Red[2]
LEDR[3]	PIN_AC22	LED Red[3]
LEDR[4]	PIN_AD22	LED Red[4]
LEDR[5]	PIN_AD23	LED Red[5]
LEDR[6]	PIN_AD21	LED Red[6]
LEDR[7]	PIN_AC21	LED Red[7]
LEDR[8]	PIN_AA14	LED Red[8]
LEDR[9]	PIN_Y13	LED Red[9]
LEDR[10]	PIN_AA13	LED Red[10]
LEDR[11]	PIN_AC14	LED Red[11]
LEDR[12]	PIN_AD15	LED Red[12]
LEDR[13]	PIN_AE15	LED Red[13]
LEDR[14]	PIN_AF13	LED Red[14]
LEDR[15]	PIN_AE13	LED Red[15]
LEDR[16]	PIN_AE12	LED Red[16]
LEDR[17]	PIN_AD12	LED Red[17]
LEDG[0]	PIN_AE22	LED Green[0]
LEDG[1]	PIN_AF22	LED Green[1]
LEDG[2]	PIN_W19	LED Green[2]
LEDG[3]	PIN_V18	LED Green[3]
LEDG[4]	PIN_U18	LED Green[4]
LEDG[5]	PIN_U17	LED Green[5]
LEDG[6]	PIN_AA20	LED Green[6]
LEDG[7]	PIN_Y18	LED Green[7]
LEDG[8]	PIN_Y12	LED Green[8]

4.3 Using the 7-segment Displays

The DE2 Board has eight 7-segment displays. These displays are arranged into two pairs and a group of four, with the intent of displaying numbers of various sizes. As indicated in the schematic in Figure 4.6, the seven segments are connected to pins on the Cyclone II FPGA. Applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off.

Each segment in a display is identified by an index from 0 to 6, with the positions given in Figure 4.7. Note that the dot in each display is unconnected and cannot be used. Table 4.4 shows the assignments of FPGA pins to the 7-segment displays.



Signal Name	FPGA Pin No.	Description
HEX0[0]	PIN_AF10	Seven Segment Digit 0[0]
HEX0[1]	PIN_AB12	Seven Segment Digit 0[1]
HEX0[2]	PIN_AC12	Seven Segment Digit 0[2]
HEX0[3]	PIN_AD11	Seven Segment Digit 0[3]
HEX0[4]	PIN_AE11	Seven Segment Digit 0[4]
HEX0[5]	PIN_V14	Seven Segment Digit 0[5]
HEX0[6]	PIN_V13	Seven Segment Digit 0[6]
HEX1[0]	PIN_V20	Seven Segment Digit 1[0]
HEX1[1]	PIN_V21	Seven Segment Digit 1[1]
HEX1[2]	PIN_W21	Seven Segment Digit 1[2]
HEX1[3]	PIN_Y22	Seven Segment Digit 1[3]
HEX1[4]	PIN_AA24	Seven Segment Digit 1[4]
HEX1[5]	PIN_AA23	Seven Segment Digit 1[5]
HEX1[6]	PIN_AB24	Seven Segment Digit 1[6]
HEX2[0]	PIN_AB23	Seven Segment Digit 2[0]
HEX2[1]	PIN_V22	Seven Segment Digit 2[1]
HEX2[2]	PIN_AC25	Seven Segment Digit 2[2]
HEX2[3]	PIN_AC26	Seven Segment Digit 2[3]
HEX2[4]	PIN_AB26	Seven Segment Digit 2[4]
HEX2[5]	PIN_AB25	Seven Segment Digit 2[5]
HEX2[6]	PIN_Y24	Seven Segment Digit 2[6]
HEX3[0]	PIN_Y23	Seven Segment Digit 3[0]
HEX3[1]	PIN_AA25	Seven Segment Digit 3[1]
HEX3[2]	PIN_AA26	Seven Segment Digit 3[2]
HEX3[3]	PIN_Y26	Seven Segment Digit 3[3]
HEX3[4]	PIN_Y25	Seven Segment Digit 3[4]
HEX3[5]	PIN_U22	Seven Segment Digit 3[5]
HEX3[6]	PIN_W24	Seven Segment Digit 3[6]
HEX4[0]	PIN_U9	Seven Segment Digit 4[0]
HEX4[1]	PIN_U1	Seven Segment Digit 4[1]
HEX4[2]	PIN_U2	Seven Segment Digit 4[2]
HEX4[3]	PIN_T4	Seven Segment Digit 4[3]
HEX4[4]	PIN_R7	Seven Segment Digit 4[4]
HEX4[5]	PIN_R6	Seven Segment Digit 4[5]
HEX4[6]	PIN_T3	Seven Segment Digit 4[6]

HEX5[0]	PIN_T2	Seven Segment Digit 5[0]
HEX5[1]	PIN_P6	Seven Segment Digit 5[1]
HEX5[2]	PIN_P7	Seven Segment Digit 5[2]
HEX5[3]	PIN_T9	Seven Segment Digit 5[3]
HEX5[4]	PIN_R5	Seven Segment Digit 5[4]
HEX5[5]	PIN_R4	Seven Segment Digit 5[5]
HEX5[6]	PIN_R3	Seven Segment Digit 5[6]
HEX6[0]	PIN_R2	Seven Segment Digit 6[0]
HEX6[1]	PIN_P4	Seven Segment Digit 6[1]
HEX6[2]	PIN_P3	Seven Segment Digit 6[2]
HEX6[3]	PIN_M2	Seven Segment Digit 6[3]
HEX6[4]	PIN_M3	Seven Segment Digit 6[4]
HEX6[5]	PIN_M5	Seven Segment Digit 6[5]
HEX6[6]	PIN_M4	Seven Segment Digit 6[6]
HEX7[0]	PIN_L3	Seven Segment Digit 7[0]
HEX7[1]	PIN_L2	Seven Segment Digit 7[1]
HEX7[2]	PIN_L9	Seven Segment Digit 7[2]
HEX7[3]	PIN_L6	Seven Segment Digit 7[3]
HEX7[4]	PIN_L7	Seven Segment Digit 7[4]
HEX7[5]	PIN_P9	Seven Segment Digit 7[5]
HEX7[6]	PIN_N9	Seven Segment Digit 7[6]

4.4 Clock Inputs

The DE2 board includes two oscillators that produce 27 MHz and 50 MHz clock signals. The board also includes an SMA connector which can be used to connect an external clock source to the board. The schematic of the clock circuitry is shown in Figure 4.8, and the associated pin assignments appear in Table 4.5.

Important: To use the 27 MHz clock, the TD_RESET pin (PIN_C4) must be asserted to a high logic level.

Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D13	27 MHz clock input
CLOCK_50	PIN_N2	50 MHz clock input
EXT_CLOCK	PIN_P26	External (SMA) clock input

4.5 Using the LCD Module

The LCD module has built-in fonts and can be used to display text by sending appropriate commands to the display controller, which is called HD44780. Detailed information for using the display is available in its datasheet, which can be found on the manufacturer's web site, and from the *Datasheet* folder on the **DE2 System CD-ROM**. A schematic diagram of the LCD module showing connections to the Cyclone II FPGA is given in Figure 4.9. The associated pin assignments appear in Table 4.6.

Signal Name	FPGA Pin No.	Description
LCD_DATA[0]	PIN_J1	LCD Data[0]
LCD_DATA[1]	PIN_J2	LCD Data[1]
LCD_DATA[2]	PIN_H1	LCD Data[2]
LCD_DATA[3]	PIN_H2	LCD Data[3]
LCD_DATA[4]	PIN_J4	LCD Data[4]
LCD_DATA[5]	PIN_J3	LCD Data[5]
LCD_DATA[6]	PIN_H4	LCD Data[6]
LCD_DATA[7]	PIN_H3	LCD Data[7]
LCD_RW	PIN_K4	LCD Read/Write Select, 0 = Write, 1 = Read
LCD_EN	PIN_K3	LCD Enable
LCD_RS	PIN_K1	LCD Command/Data Select, 0 = Command, 1 = Data
LCD_ON	PIN_L4	LCD Power ON/OFF
LCD_BLON	PIN_K2	LCD Back Light ON/OFF