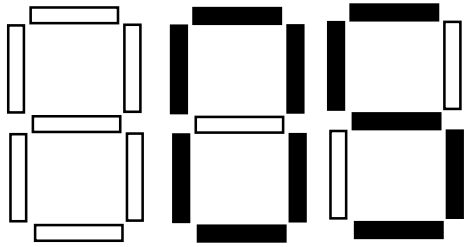
Tentative Lab Schedule

- 02/20
  - Revision on Lab 1,2 and 3.
  - Lab 4 – 4 Bit Adder/Subtractor
- 02/27 --- Test 1.
- 03/06 – Deadlines for Lab 4 implementation
  - No class on (03/06).
- 03/07 Deadlines for Lab 4 report.
- The class will resume on 03/20 with Lab 5- A
- 03/27 Lab 5-B and Final Implementation.
- Final Presentation on April 13.

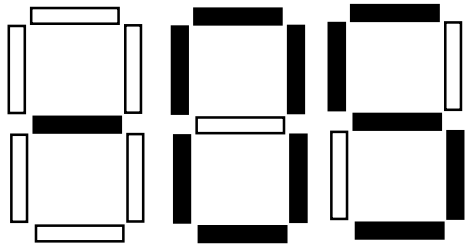
LAB-4 4 Bit Adder/Subtractor

Deliverables:

- Implement a 4 bit Adder/Subtractor using Quartus II Schematic Block using the 4 bit adder from Lab 3.
  - Use the 2nd complement system to represent negative number and perform addition.
  - Eg. $14 - 9$ $14 + (-9)$.
- Compilation and Simulation on Quartus II
- Implement a display ckt which displays a negative binary number into a negative decimal number.
  - Eg. + 5



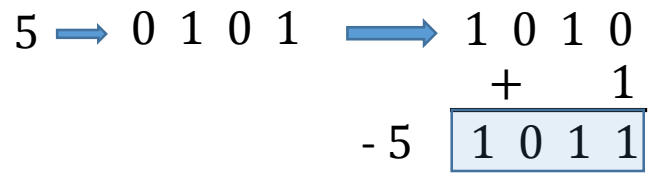
-5



- Implement a fully functional the 4 bit Adder/Subtractor with the 7 segment display and test it on DE2 Board.

2^{nd} Complement

- Binary representation of a negative number.
- Eg.

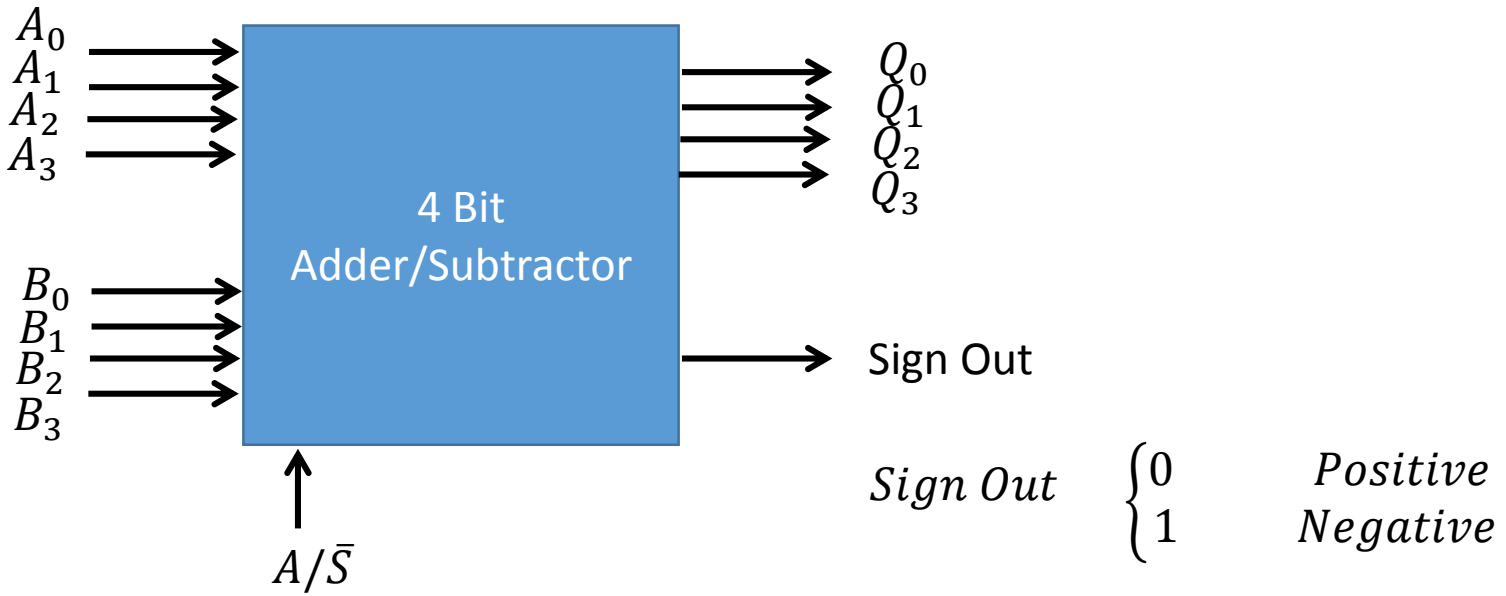


- In the 2^{nd} complement system, MSB is used as a sign bit.
  - MSB = 0 represents the binary number is a positive integer.
  - MSB = 1 represents the binary number is a negative integer.
- N Binary Bit can represent $2^{N-1} - 1$ positive integer and 2^{N-1} negative integer.
  - Eg. 4 bit binary number can represent up to $(2^{4-1}-1 = 7)$ and $(-2^{4-1} = -8)$

Example of Negative Number Representation for 4 bit system

Binary				Integer
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	-1
1	0	0	1	-2
1	0	1	0	-3
1	0	1	1	-4
1	1	0	0	-5
1	1	0	1	-6
1	1	1	0	-7
1	1	1	1	-8

4 Bit Adder/Subtractor



$Sign\ Out$ $\begin{cases} 0 & Positive \\ 1 & Negative \end{cases}$

$A/\bar{S}$ $\begin{cases} 1 & Adder \\ 0 & Subtractor \end{cases}$

4 Bit Adder/Subtractor

- $(A_3A_2A_1A_0) - (B_3B_2B_1B_0)$
- A B
- Design a subtractor such that A-B = A + (-B)
- The max integer we can input from B is 15, 1111.
- To represent (-15) in binary we need a 5 bit binary system.
- Eg.

15 → 1 1 1 1 → 0 0 0 0

+ 1

This is wrong!!!! 0 0 0 1

15 → 0 1 1 1 1 → 1 0 0 0 0

+ 1

-15 in Binary.. 1 0 0 0 1

Sign Bit

- In a 4 bit system, add one MSB bit for Sign Bit

4 Bit Adder/Subtractor

- Eg. A = 9, B =14 : A- B
- $(A_3A_2A_1A_0) = 1001, (B_3B_2B_1B_0) = 1110$
- First convert A and B with a 5 bit system.
  - $A_3A_2A_1A_0 \Rightarrow 0\ A_3A_2A_1A_0, (B_3B_2B_1B_0) = 0\ B_3B_2B_1B_0$
- Find the 2nd complement of $0\ B_3B_2B_1B_0$.
- $01110 = 10001$ which is $(1\ \overline{B_3}\ \overline{B_2}\ \overline{B_1}\ \overline{B_0})$.
- Add (00001) and then add $0\ A_3A_2A_1A_0$ to get the final answer.

$$\begin{array}{rl} & 10001 \\ + & 00001 \\ \hline & 10010 \end{array}$$

-15 ⇒ 10010

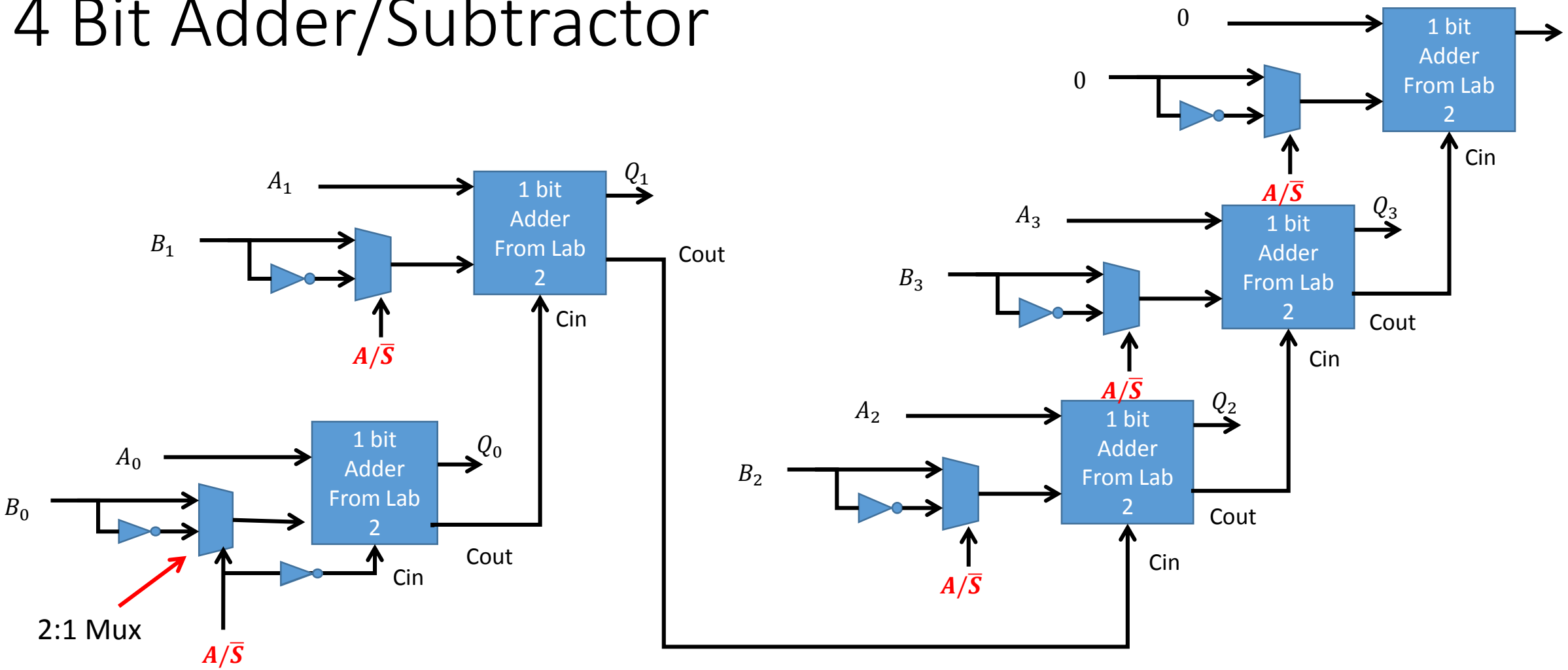
$$\begin{array}{rl} & 01001 \\ + & \\ \hline & \end{array}$$

-5 ⇒ 11011

Sign bit tells the result is a negative number.

$SignOut$

4 Bit Adder/Subtractor



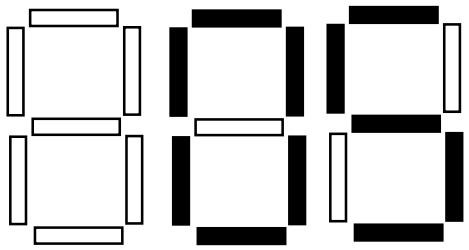
For 2:1 Mux, search as 21MUX in Quartus Schematic. Connect B to A of the mux of the 2:1 Mux, $\overline{B}$ to B of the mux.

$A/\overline{S}$ controls the select line of 2:1 Mux.

4 Bit Adder/Subtractor

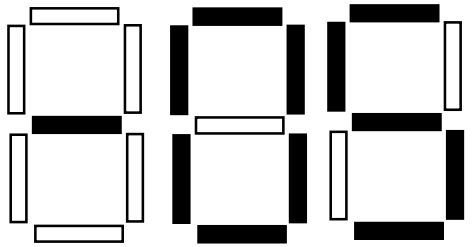
- The Sign bit output tells us whether the result is positive or negative.
- If positive (sign out = 0) , then we can directly display $(Q_3Q_2Q_1Q_0)$ using Display Ckt from Lab 2.
- If the result is negative (sign out = 1), we need to convert the negative binary value to minus sign and positive magnitude to display.
- Eg

$Signout\ Q_3Q_2Q_1Q_0 = 00101$

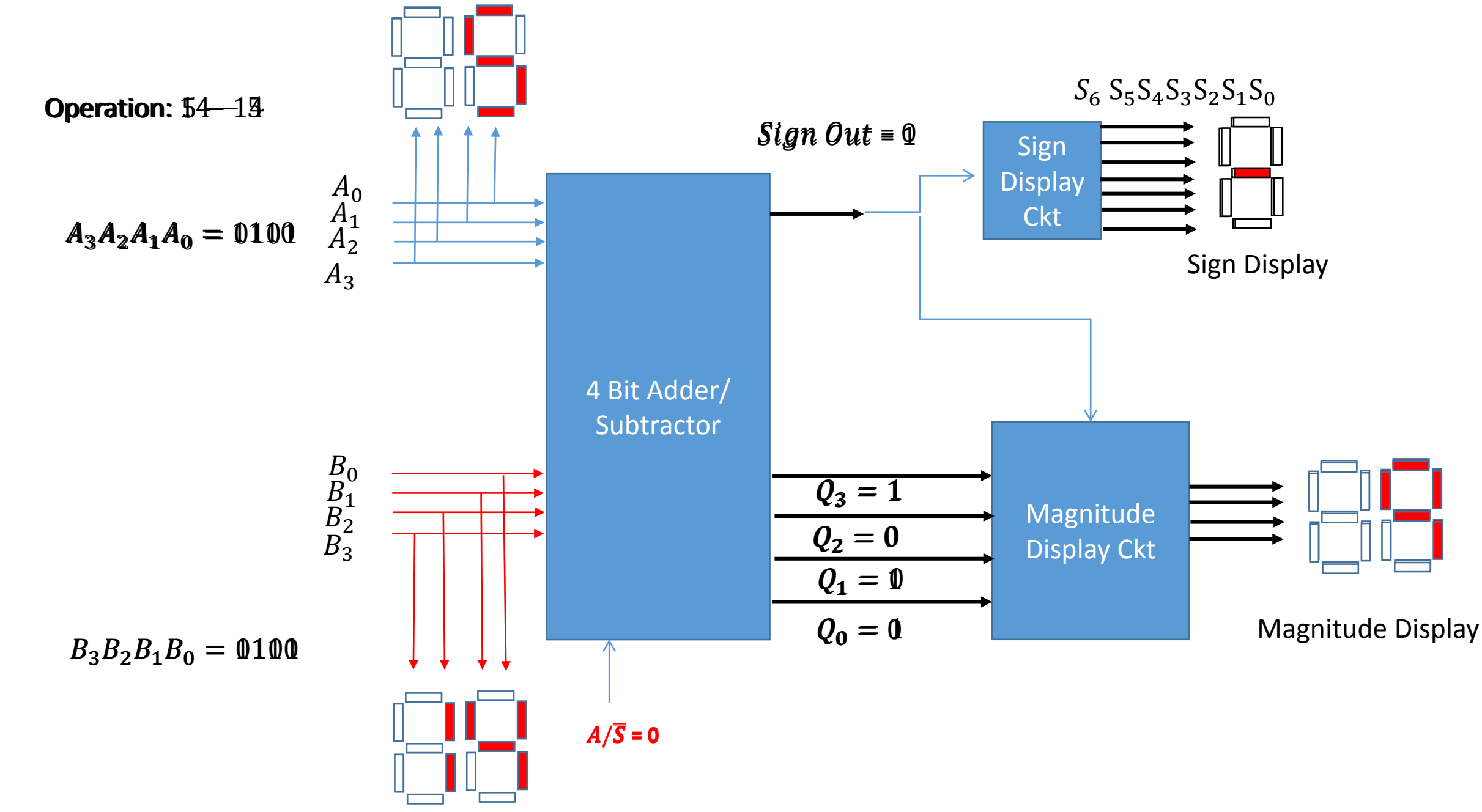


Sign Magnitude

$Signout\ Q_3Q_2Q_1Q_0 = 11011$

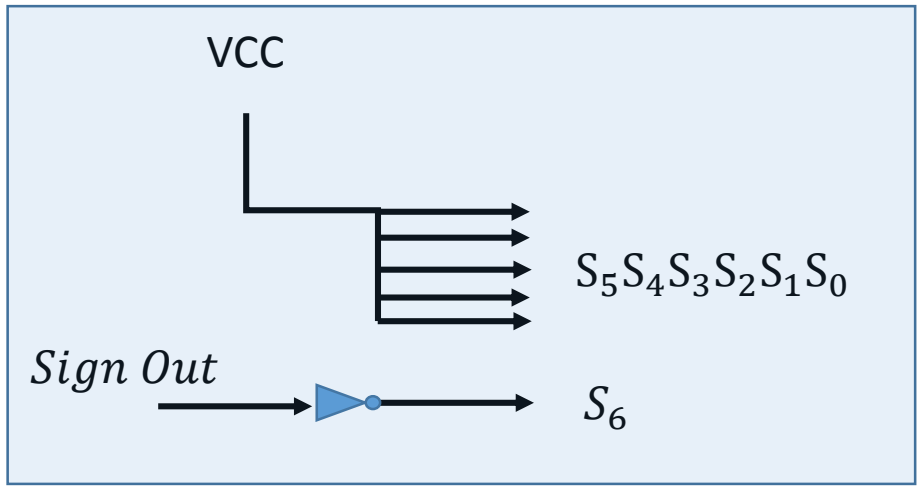


Sign Magnitude

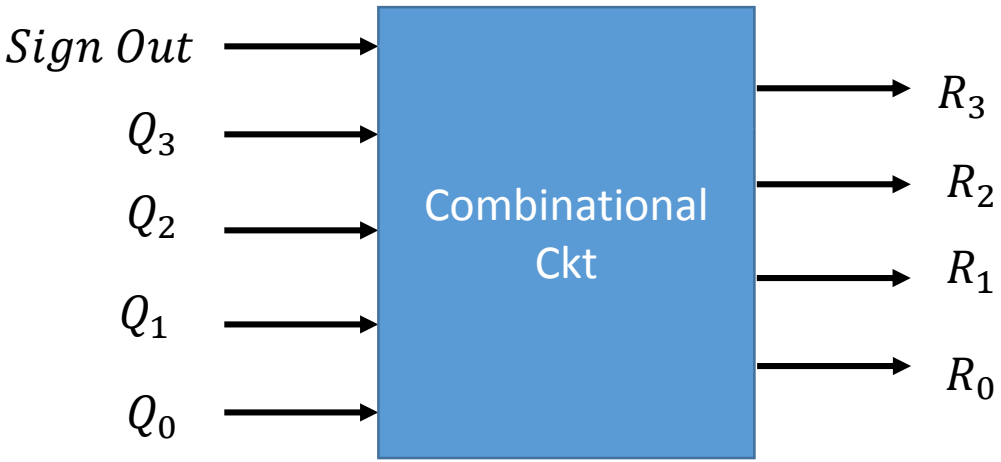

Operation: 5 – 4
$A_3A_2A_1A_0 = 0100$
$B_3B_2B_1B_0 = 0100$
A_0
A_1
A_2
A_3
B_0
B_1
B_2
B_3
4 Bit Adder/ Subtractor
$A/\overline{S} = 0$
Sign Out ≡ 0
Sign Display Ckt
$S_6\ S_5S_4S_3S_2S_1S_0$
Sign Display
$Q_3 = 1$
$Q_2 = 0$
$Q_1 = 0$
$Q_0 = 0$
Magnitude Display Ckt
Magnitude Display

Sign Display Ckt

Input *Sign Out*	*Output* $S_6\ S_5S_4S_3S_2S_1S_0$
0	1 1 1 1 1 1 1
1	0 1 1 1 1 1 1



Magnitude Display

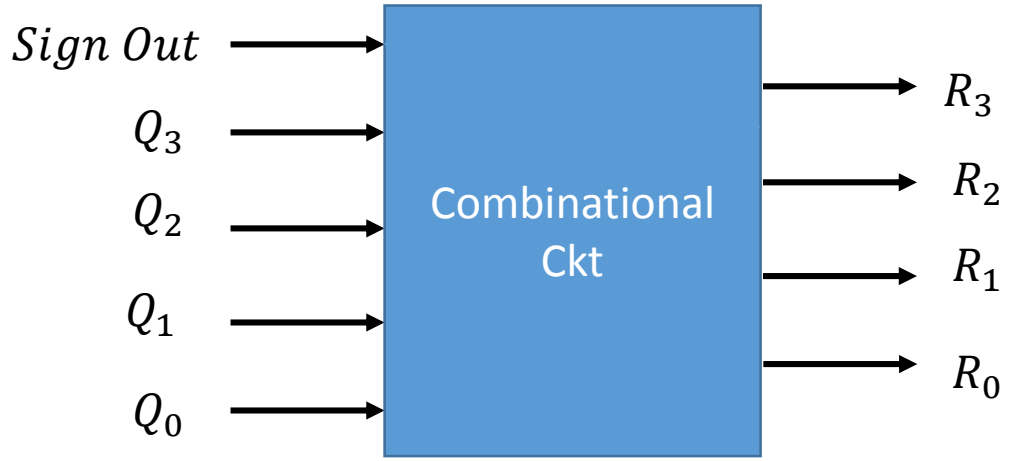


$R_3R_2R_1R_0$ are connected to $X_3X_2X_1X_0$ of Display ckt from Lab 2.

Magnitude Display

Positive Number

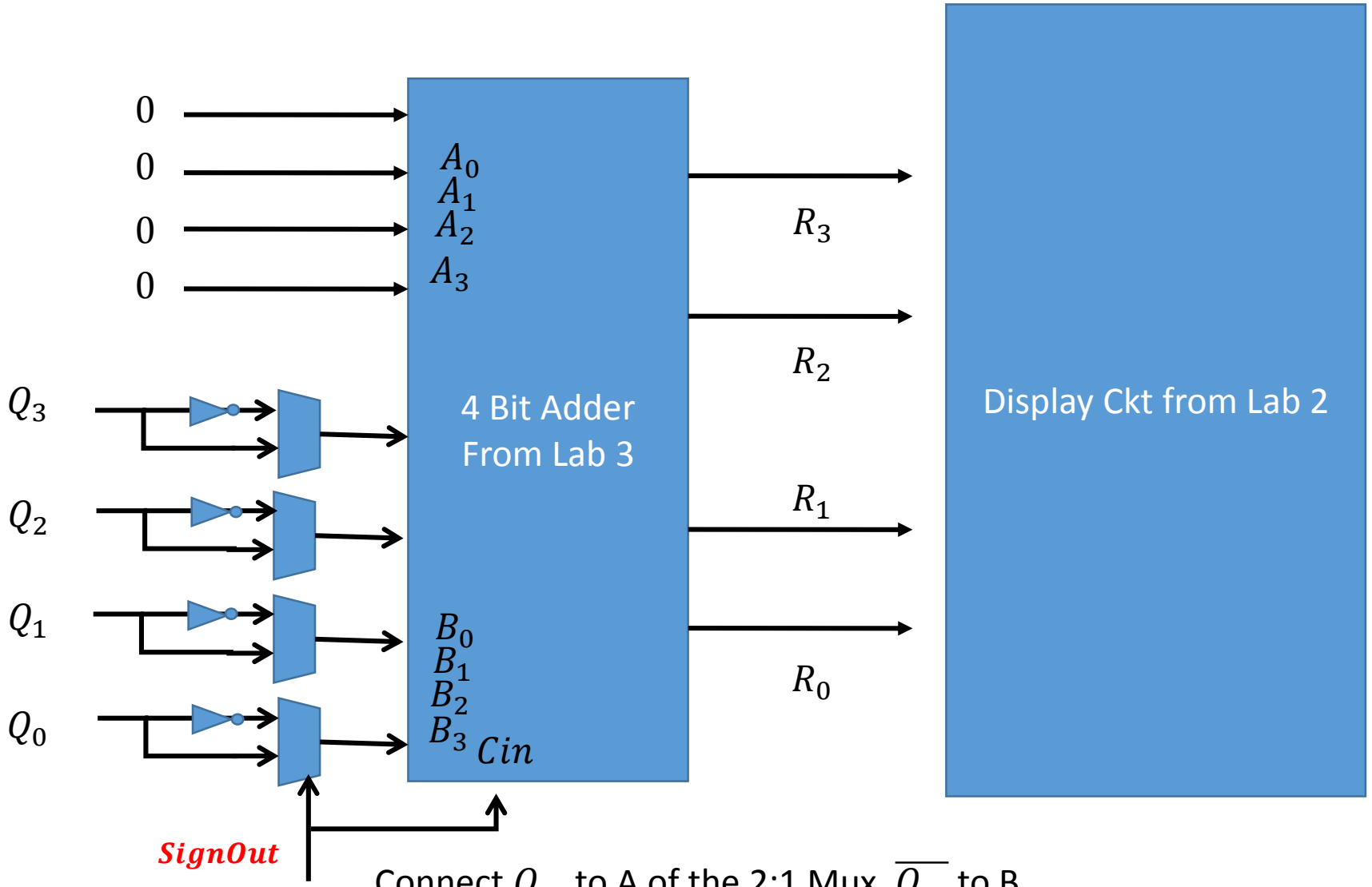
Sign Out	Q3	Q2	Q1	Q0	Magnitude	R3	R2	R1	R0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	1
0	0	0	1	0	2	0	0	1	0
0	0	0	1	1	3	0	0	1	1
0	0	1	0	0	4	0	1	0	0
0	0	1	0	1	5	0	1	0	1
0	0	1	1	0	6	0	1	1	0
0	0	1	1	1	7	0	1	1	1
0	0	0	0	0	8	0	0	0	0
0	0	0	0	1	9	0	0	0	1
0	0	0	1	0	10	0	0	1	0
0	0	0	1	1	11	0	0	1	1
0	0	1	0	0	12	0	1	0	0
0	0	1	0	1	13	0	1	0	1
0	0	1	1	0	14	0	1	1	0
0	0	1	1	1	15	0	1	1	1



- When the result Q3Q2Q1Q0 is positive number,
  R3R2R1R0 = Q3Q2Q1Q0
- We can get the magnitude value of negative binary number
- 1. Flip 0 to 1 and 1 to 0. Eg 11011 => 00100
- 2. Add with 00001
  - 00100 + 00001 => 00101 which is 5.

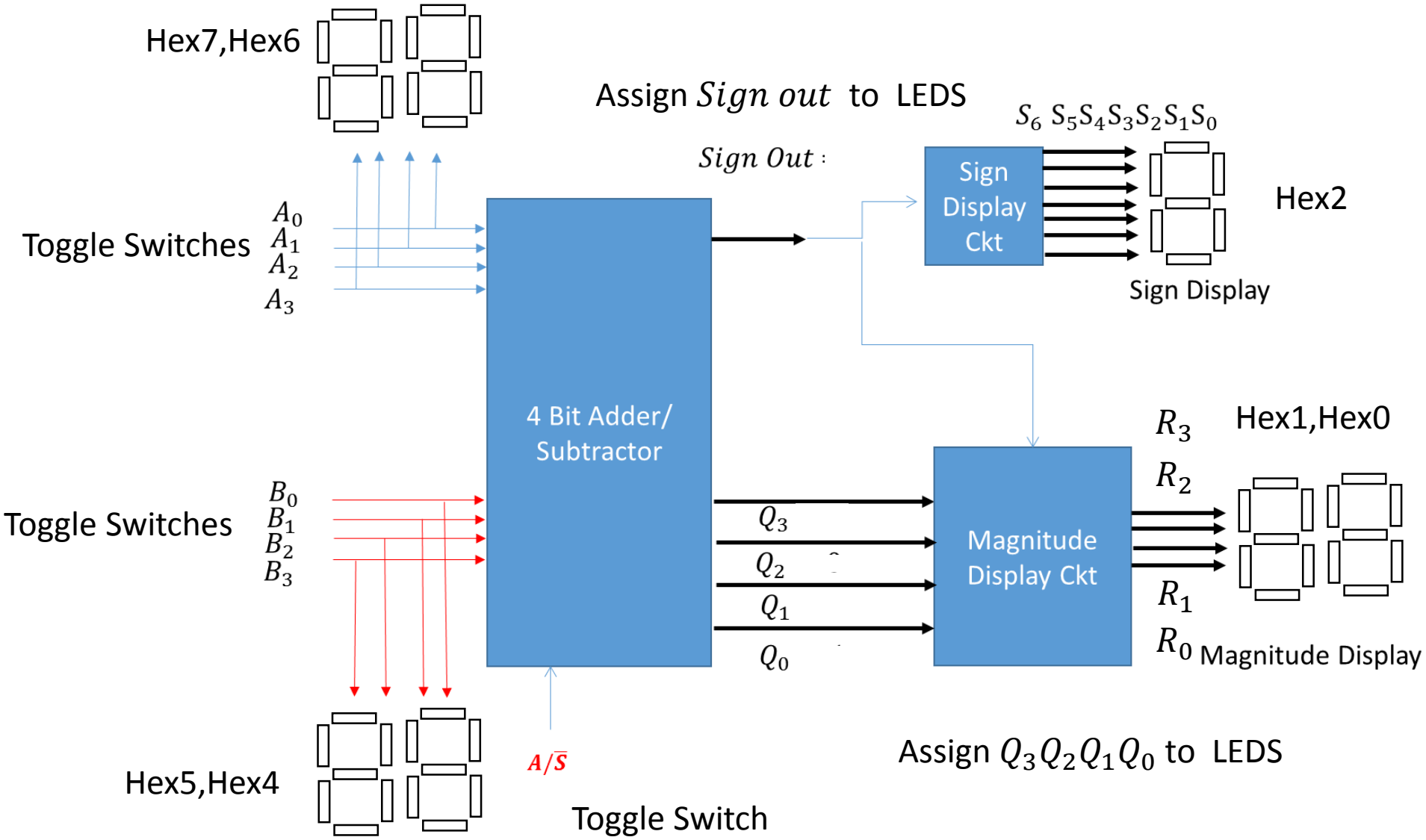
- If Sign Bit = 0
  - R = Q
- Else
  - R = not(Q) + 00001
- End if;

Magnitude Display Ckt



Connect Q to A of the 2:1 Mux, $\overline{Q}$ to B .

Toplevel Ckt - 4 Bit Add/Sub and Display Ckt



Project Flow Chart

1. Implement 4 bit Add/Subtractor
2. Simulation waveform on Quartus II
3. Implement Sign Display Ckt and Magnitude Display Ckt.
4. Implement Top Level Ckt.
5. Pin Assignment
6. Download the Top Level ckt to DE2 Board.

DE 2 Pin Table

Signal Name	FPGA Pin No.
SW[0]	PIN_N25
SW[1]	PIN_N26
SW[2]	PIN_P25
SW[3]	PIN_AE14
SW[4]	PIN_AF14
SW[5]	PIN_AD13
SW[6]	PIN_AC13
SW[7]	PIN_C13
SW[8]	PIN_B13
SW[9]	PIN_A13
SW[10]	PIN_N1
SW[11]	PIN_P1
SW[12]	PIN_P2
SW[13]	PIN_T7
SW[14]	PIN_U3
SW[15]	PIN_U4
SW[16]	PIN_V1
SW[17]	PIN_V2

Signal Name	FPGA Pin No.
LEDR[0]	PIN_AE23
LEDR[1]	PIN_AF23
LEDR[2]	PIN_AB21
LEDR[3]	PIN_AC22
LEDR[4]	PIN_AD22
LEDR[5]	PIN_AD23
LEDR[6]	PIN_AD21
LEDR[7]	PIN_AC21
LEDR[8]	PIN_AA14
LEDR[9]	PIN_Y13
LEDR[10]	PIN_AA13
LEDR[11]	PIN_AC14
LEDR[12]	PIN_AD15
LEDR[13]	PIN_AE15
LEDR[14]	PIN_AF13
LEDR[15]	PIN_AE13
LEDR[16]	PIN_AE12
LEDR[17]	PIN_AD12
LEDG[0]	PIN_AE22
LEDG[1]	PIN_AF22
LEDG[2]	PIN_W19
LEDG[3]	PIN_V18
LEDG[4]	PIN_U18
LEDG[5]	PIN_U17
LEDG[6]	PIN_AA20
LEDG[7]	PIN_Y18
LEDG[8]	PIN_Y12

7 Segment Pin Table

HEX0[0]	PIN_AF10
HEX0[1]	PIN_AB12
HEX0[2]	PIN_AC12
HEX0[3]	PIN_AD11
HEX0[4]	PIN_AE11
HEX0[5]	PIN_V14
HEX0[6]	PIN_V13
HEX1[0]	PIN_V20
HEX1[1]	PIN_V21
HEX1[2]	PIN_W21
HEX1[3]	PIN_Y22
HEX1[4]	PIN_AA24
HEX1[5]	PIN_AA23
HEX1[6]	PIN_AB24
HEX2[0]	PIN_AB23
HEX2[1]	PIN_V22
HEX2[2]	PIN_AC25
HEX2[3]	PIN_AC26
HEX2[4]	PIN_AB26
HEX2[5]	PIN_AB25
HEX2[6]	PIN_Y24

HEX3[0]	PIN_Y23
HEX3[1]	PIN_AA25
HEX3[2]	PIN_AA26
HEX3[3]	PIN_Y26
HEX3[4]	PIN_Y25
HEX3[5]	PIN_U22
HEX3[6]	PIN_W24

HEX4[0]	PIN_U9
HEX4[1]	PIN_U1
HEX4[2]	PIN_U2
HEX4[3]	PIN_T4
HEX4[4]	PIN_R7
HEX4[5]	PIN_R6
HEX4[6]	PIN_T3
HEX5[0]	PIN_T2
HEX5[1]	PIN_P6
HEX5[2]	PIN_P7
HEX5[3]	PIN_T9
HEX5[4]	PIN_R5
HEX5[5]	PIN_R4
HEX5[6]	PIN_R3
HEX6[0]	PIN_R2
HEX6[1]	PIN_P4
HEX6[2]	PIN_P3
HEX6[3]	PIN_M2
HEX6[4]	PIN_M3
HEX6[5]	PIN_M5
HEX6[6]	PIN_M4

HEX7[0]	PIN_L3
HEX7[1]	PIN_L2
HEX7[2]	PIN_L9
HEX7[3]	PIN_L6
HEX7[4]	PIN_L7
HEX7[5]	PIN_P9
HEX7[6]	PIN_N9

Report

- Lab Description
- Design (Boolean expression and truth table).
- Schematic diagram from Quartus II.
- Quartus II simulation waveform.
- Photo of lab running on DE2 board.
- Conclusion.