Lab 1B - Tone Generator

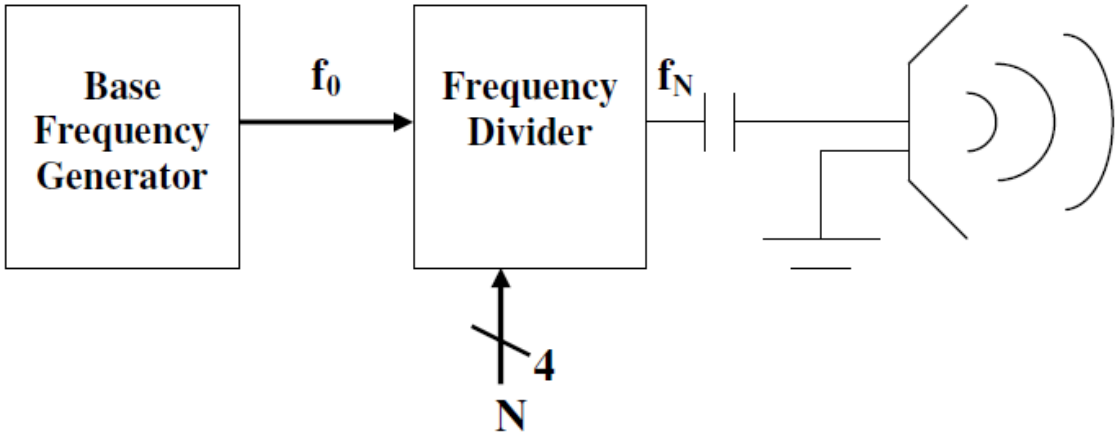
Implementation LAB 1

Deliverables:

2. **Tone generator:**

- 555 timer to achieve an output signal with a base frequency $f_b = 16kHz$ and a duty cycle of 60%. Implement this circuit using the closest resistance values and capacitance available.
- Implement a circuit that will take this base frequency and divide it to achieve a value $F_{out} = \begin{cases} \frac{1}{2(N+1)} f_b \\ \frac{1}{2(16-N)} f_b \end{cases}$.
- This circuit will accept a four-bit number N from the sequence generator implemented in part A. Use a 74LS169, and a 74LS76 J-K flip-flop to implement the T flip-flop.
- Connect the output of the previous circuit to a speaker through a capacitor.

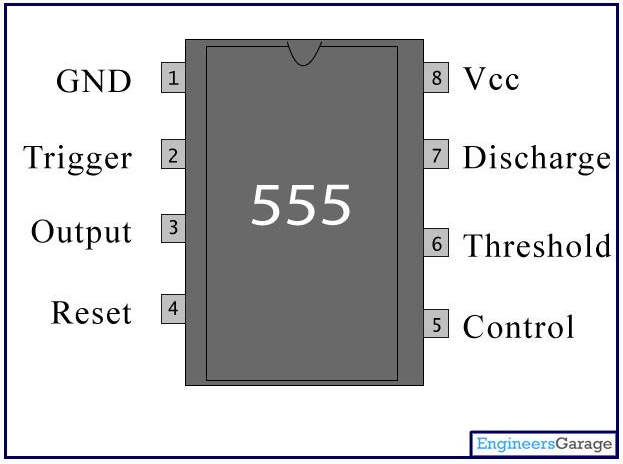
Tone Generator

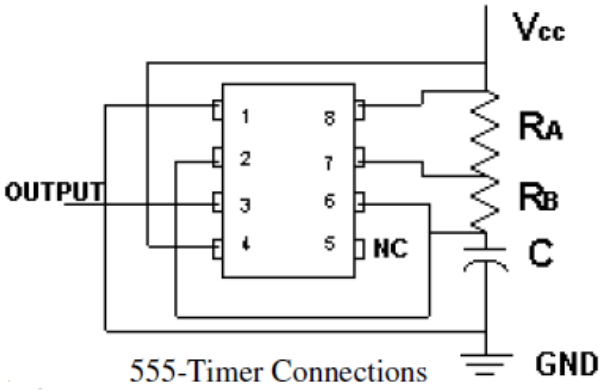


Frequency Generator:

555 Timer: The frequency and duty cycle are adjustable by varying the values of two biasing resistors and a capacitor. This IC is very flexible, being able to generate signals with a frequency range from well under 1Hz to 500kHz. We will use the 555 timer in its astable mode; that is, generating a signal that has a constant frequency.

Tone Generator(Contd.)





In astable mode, the 555 timer is connected as shown in Figure. Connected in this way, the output signal will have a high time:

And a low time:

$$t_H = 0.693\ (R_A + R_B)C$$
$$t_L = 0.693\ R_B C$$

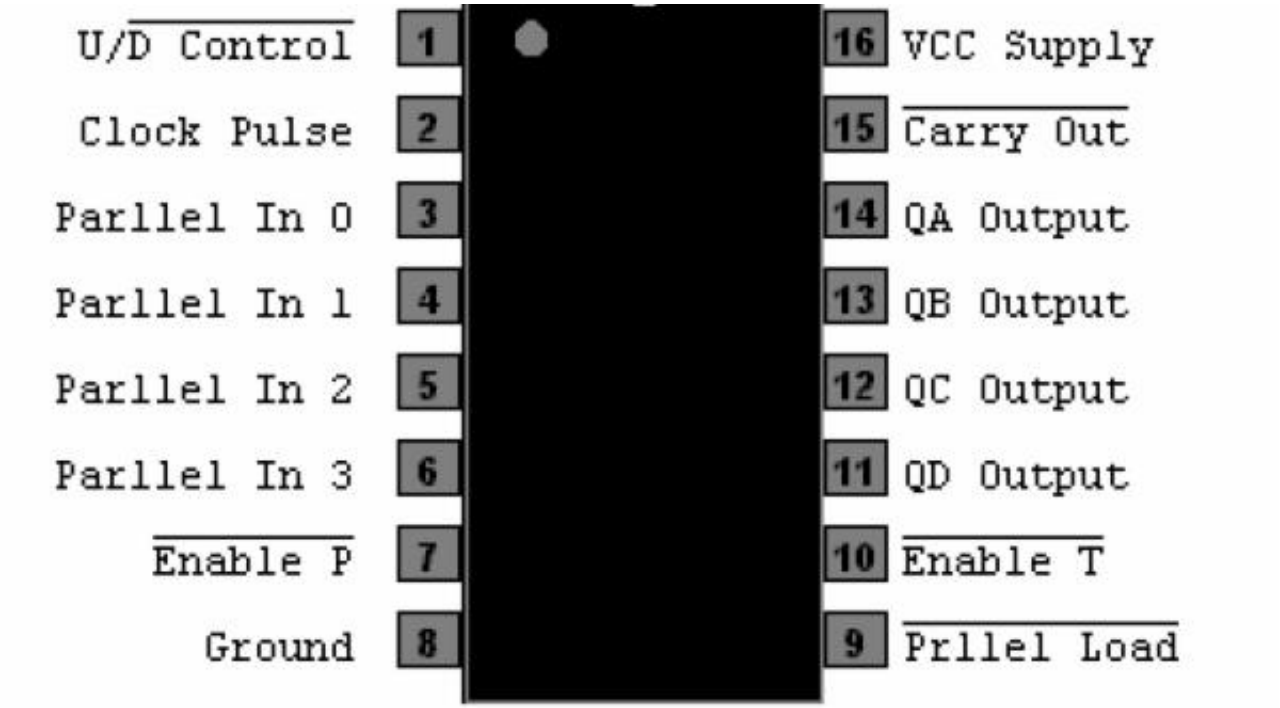
The period of this signal is:

$$T = t_H + t_L \qquad T = \frac{1}{frequency}$$

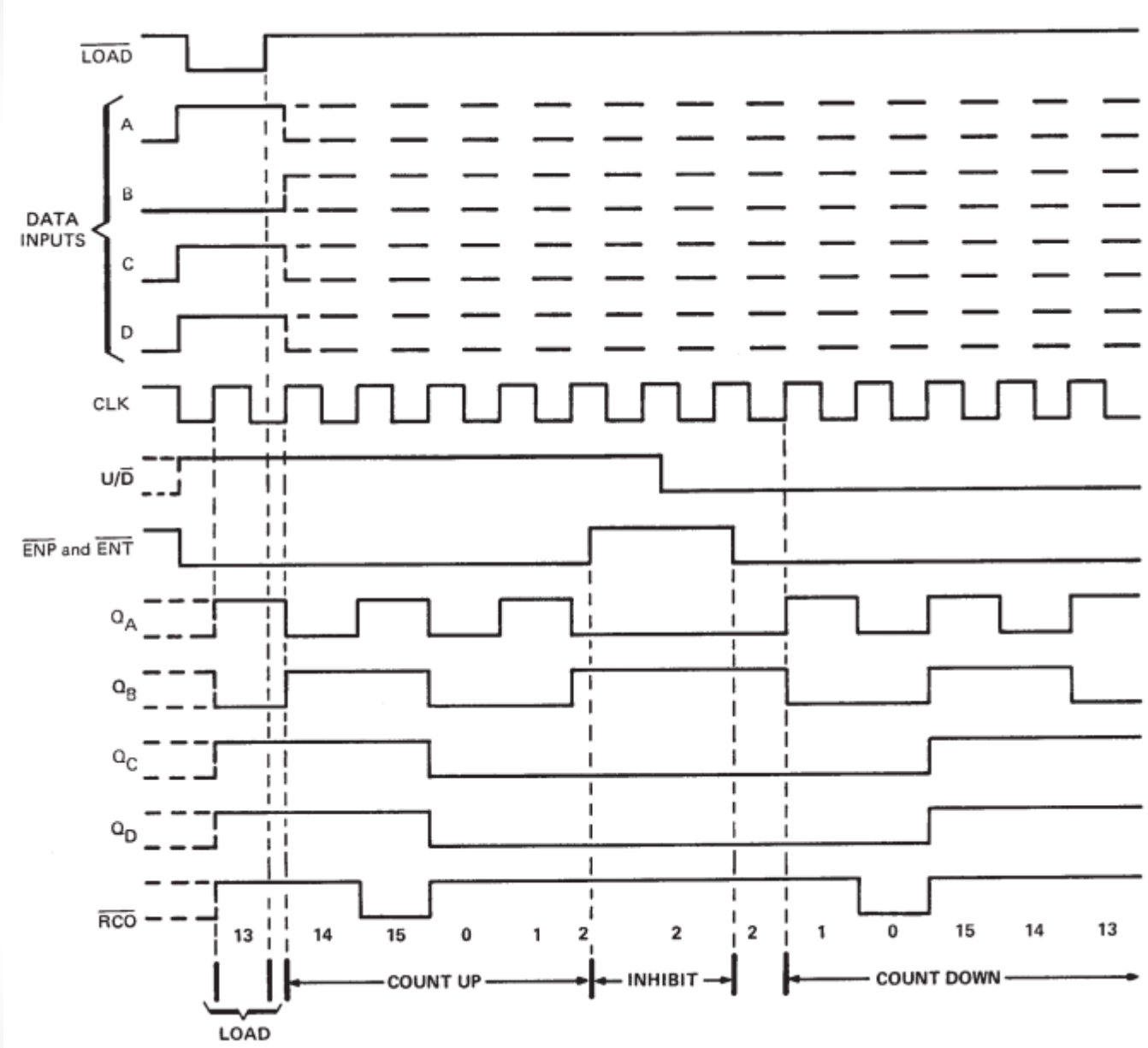
$$\text{duty cycle} = t_H/T * 100$$

Use $C = 10nF$.

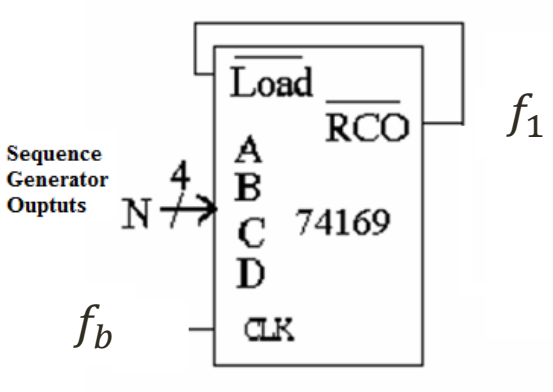
74LS169 Modulo-N Counter



Output => Carry Out
Input => In0, In1, In2, In3 (Sequence generator outputs)
$\overline{\text{Enable P}}$, $\overline{\text{Enable T}}$ => $\overline{\text{GND}}$


LOAD
A
B
DATA INPUTS
C
D
CLK
U/D
ENP and ENT
QA
QB
QC
QD
RCO
13
14
15
0
1
2
2
2
1
0
15
14
13
COUNT UP
INHIBIT
COUNT DOWN
LOAD

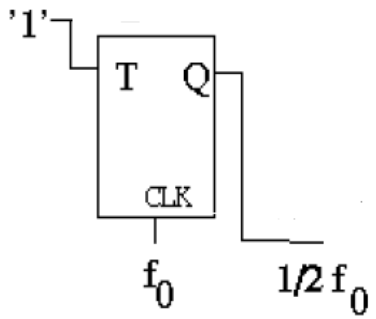
Frequency Division (Modulo N Counter)



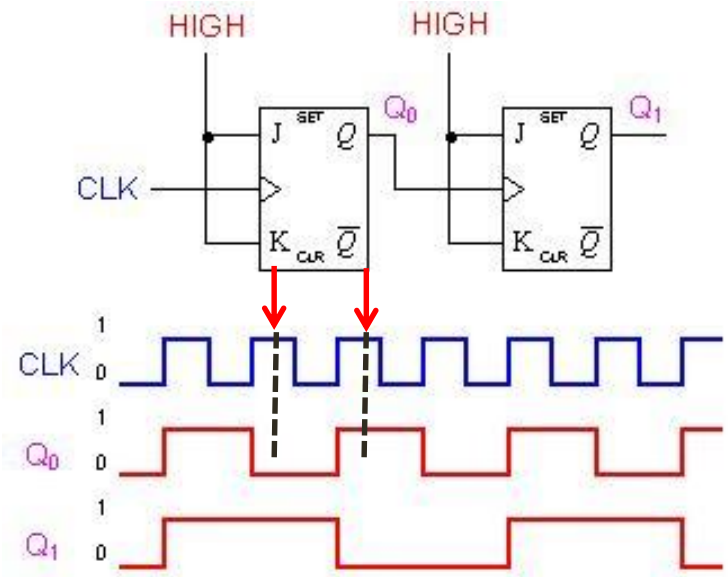
- A modulo-N counter 74169 can be used as a frequency divider,
- $f_1 = \frac{f_b}{N+1}, 1 \leq N \leq 15\ (for\ Down\ counting)$
- $f_1 = \frac{f_b}{16-N}, 0 \leq N \leq 14\ (for\ Up\ counting)$

- When $U/\overline{D}$ is Low, the counter is counting down and up counting when it is high.

Frequency Division (T-FF)



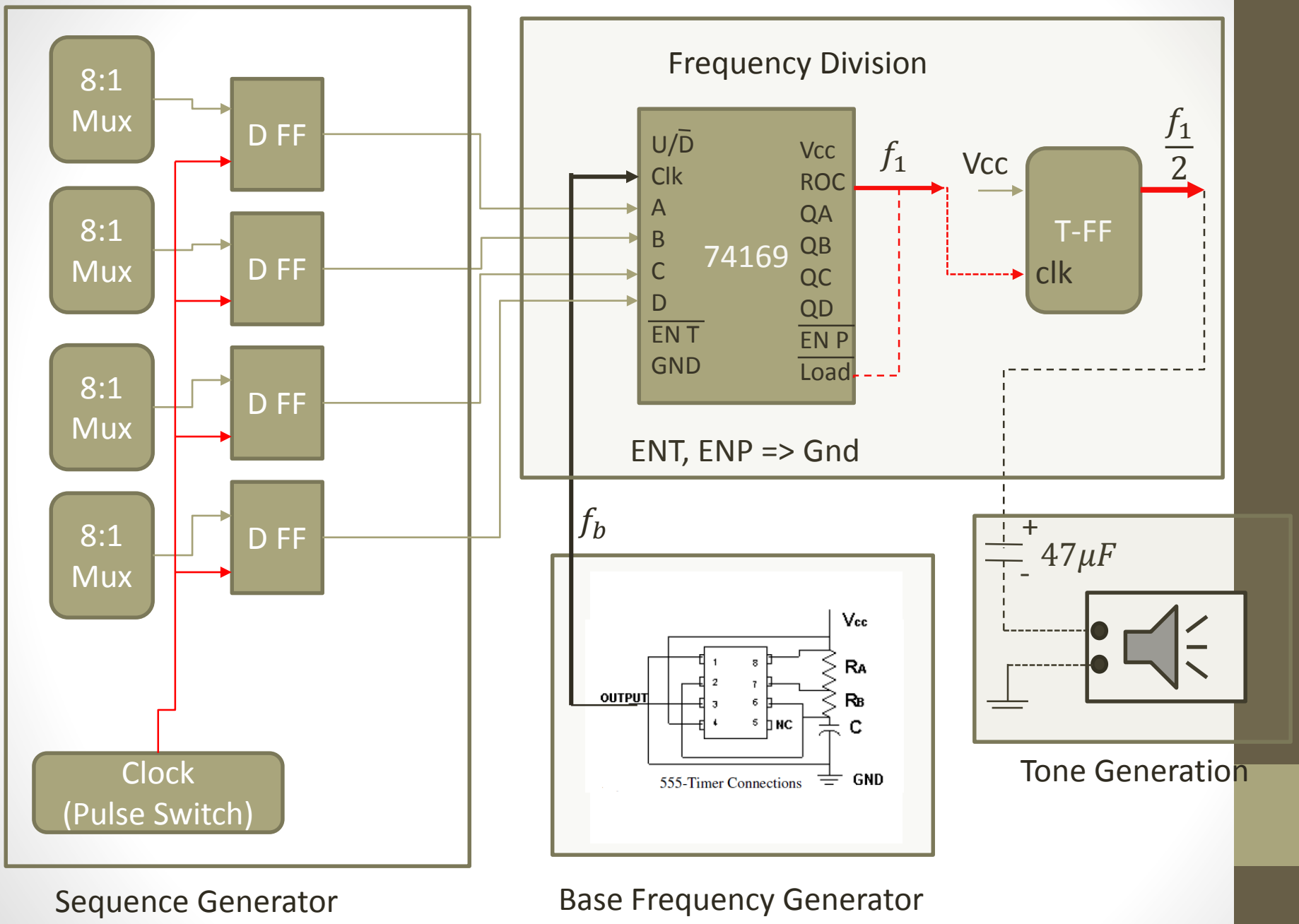
T	Q
0	Q
1	$\overline{Q}$



Correct the output waveform duty cycle to 50% by connecting with T-FF.

By Using a T flip flop we can divide the frequency by 2.

The T flip flop should be designed using a JK (7476) Flip Flop. (FF Conversion)


8:1 Mux
8:1 Mux
8:1 Mux
8:1 Mux
D FF
D FF
D FF
D FF
Clock (Pulse Switch)
Sequence Generator
Frequency Division
U/D
Clk
A
B
C
D
EN T
GND
74169
Vcc
ROC
QA
QB
QC
QD
EN P
Load
f_1
Vcc
T-FF
clk
$\frac{f_1}{2}$
ENT, ENP => Gnd
f_b
Vcc
R_A
R_B
C
OUTPUT
NC
GND
555-Timer Connections
Base Frequency Generator
+
$47\mu F$
-
Tone Generation