

Performance of Arithmetic Shifting Vs. IMUL and IDIV i486 Instructions

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Integer division or multiplication by a power of 2 can be accomplished by bit shifting instructions. The goal was to determine if the AMD Phenom II, codename “Deneb”, used internal optimizations within the i486 IDIV and IMUL assembly instructions to increase the performance of integer division and multiplication.

Implementation

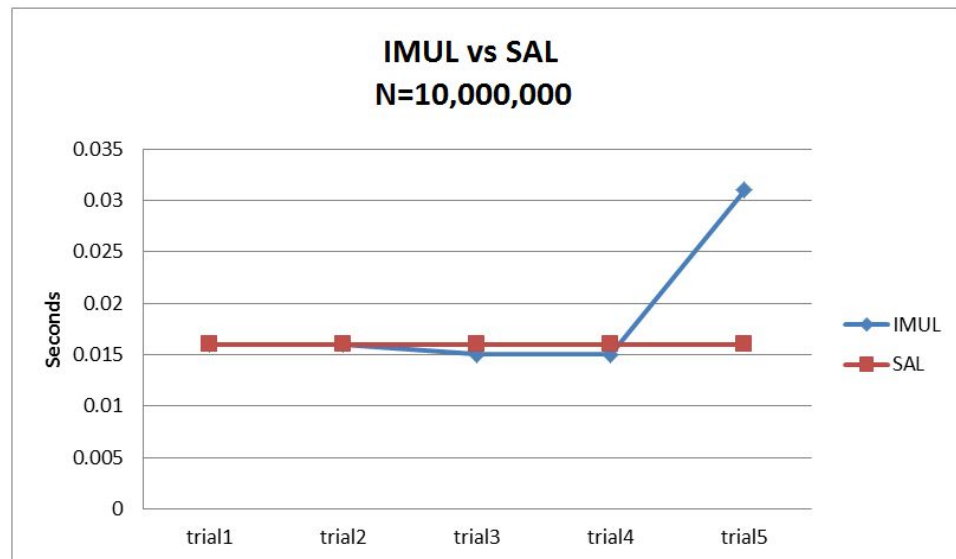
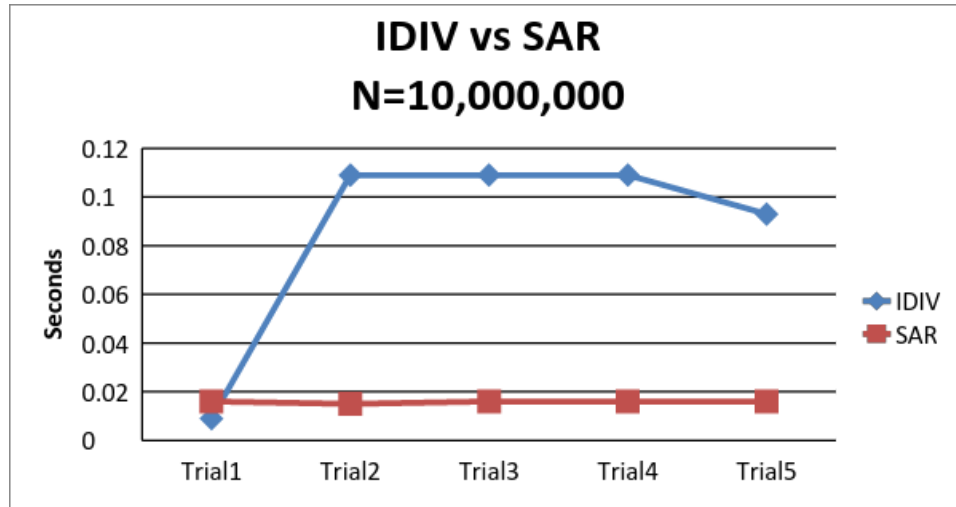
Shifting was performed on the 32-bit EAX register. The divisor and multiplier were set to the 16-bit value 2d to ensure the attributes and results didn’t exceed 32-bit. The multiplicand and dividend were set to 500d prior to each arithmetic operation. The loop was performed 10,000,000 times, and the start and stop times were recorded. Five trials were performed. The process priority was set to High to minimize the number of interrupts.

Results

When using IDIV and IMUL, the best case scenario took the equivalent time as their respective shifting instruction. This suggests that the AMD “Deneb” core does use bit shifting within these arithmetic instructions. However, the variability of the time required for the arithmetic instructions was significantly higher. The Variance (σ^2) for IDIV was $1.51 \times 10^{-3} \text{sec}^2$ while the variance for SAR was $1.59 \times 10^{-7} \text{sec}^2$, which is negligible. Similarly the variance for IMUL was $4.24 \times 10^{-5} \text{sec}^2$ while the variance for SAL was 0sec^2 . Although the best case for all four instructions was the same, the average run-time for shifting instructions was lower. The average for IDIV was 0.0858 sec and the average for SAR was 0.0158 sec. The average for IMUL was 0.0188 sec and the average for SAL was 0.016 sec.

Summary

The IDIV and IMUL operations are capable of performing as fast as SAR and SAL, however their worst case run-time is significantly higher. Shifting instructions are more consistent when multiplying or dividing integers by a power of 2.



Elapsed Time of .486 Assembly Instructions (sec)					
N=10,000,000					
	Trial1	Trial2	Trial3	Trial4	Trial5
IDIV	0.009	0.109	0.109	0.109	0.093
SAR	0.016	0.015	0.016	0.016	0.016
IMUL	0.016	0.016	0.015	0.015	0.032
SAL	0.016	0.016	0.016	0.016	0.016

Source code: Assembled and Linked with MASM 5.10

```

13 .486 ;Generates the Assembly instruction set
14 .model flat ;Generates the 32-bit code but without using
15 .stack 100h ;allocates 100h bytes to the stack
16 ExitProcess PROTO Near32 stdcall, dVal:dword
17 getch PROTO Near32 stdcall
18 putstring PROTO Near32 stdcall, lpStringToPrint:dword
19 putch PROTO Near32 stdcall, bVal:byte
20 getTime PROTO Near32 stdcall, lpStringToHold:dword
21 pressEnterToContinue PROTO Near32 stdcall, lpStringToPrint:dword
22 newline macro
23     INVOKE putch, 10
24     INVOKE putch, 13
25 endm
26 .data
27     loopThrough dword 10000000d ;times to repeat loops
28     enterToStart byte 10,13,9,"Press ENTER to start",0
29     t1 byte 40 dup(?)
30     t2 byte 40 dup(?)
31     t3 byte 40 dup(?)
32     t4 byte 40 dup(?)
33 .code
34 _start:
35     INVOKE pressEnterToContinue, addr enterToStart
36     newline
37     mov bx, 2d ;bx is divisor and multiplicand
38     mov ecx, loopThrough ;repeat idiv N times
39
40     push ecx
41     INVOKE getTime, addr t1 ;record start time for idiv / imul
42     pop ecx
43 divloop:
44     mov eax, 500d
45     CWD ;dx:ax
46     idiv bx
47     loop divloop
48
49     INVOKE getTime, addr t2 ;record end time for idiv / imul
50
51     mov ecx, loopThrough ;repeat shift N times
52
53     push ecx
54     INVOKE getTime, addr t3 ;record start time for shift operations
55     pop ecx
56 shiftLoop:
57     mov eax, 500d
58     CWD ;dx:ax
59     SAR eax, 1
60     loop shiftLoop
61     INVOKE getTime, addr t4 ;record end time for shift operations
62
63     INVOKE putstring, addr t1
64     newline
65     INVOKE putstring, addr t2
66     newline
67     newline
68     INVOKE putstring, addr t3
69     newline
70     INVOKE putstring, addr t4

```