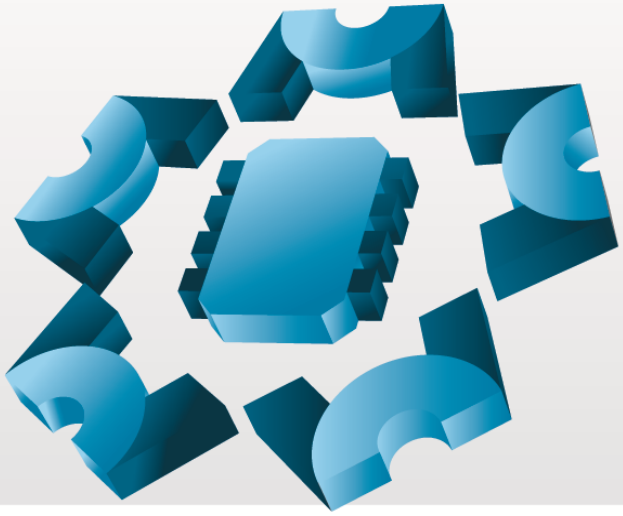

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ING. ROBERTO ISAAC SUASTE MARTINEZ

CONTENIDO

- CONFIGURACIÓN DEL ADC DEL PIC16F1827

Subrutina de Inicialización

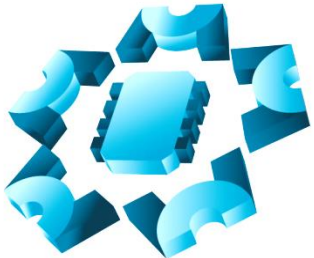

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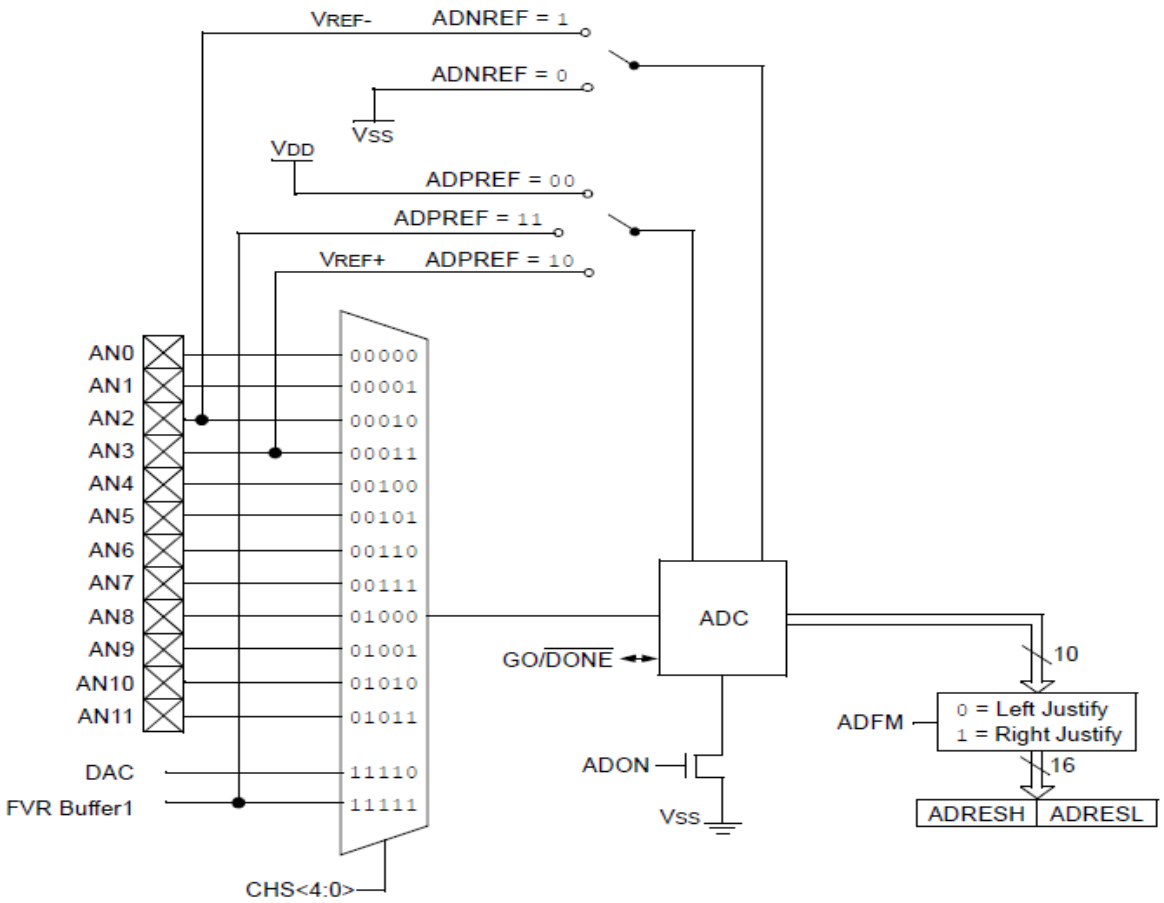
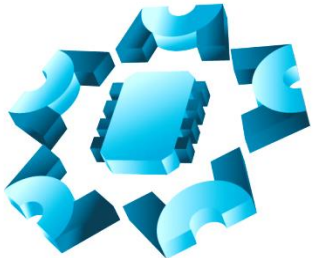
Diagrama de Bloques del ADC



Note: When ADON = 0, all multiplexer inputs are disconnected.

CONFIGURACIÓN DEL ADC



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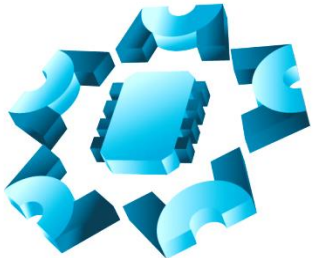
Para configurar y poder usar el ADC, es necesario considerar los siguientes requerimientos:

- Configuración de Puertos
- Selección del Canal
- Selección del Voltaje de Referencia del ADC
- Selección de la Fuente de Reloj para la Conversión
- ~~Control de Interrupción~~
- Selección del Formato del Resultado



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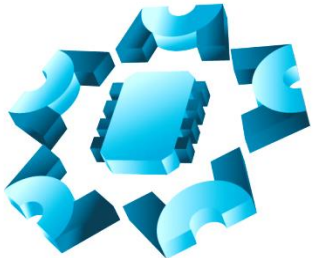
Configuración de Puertos



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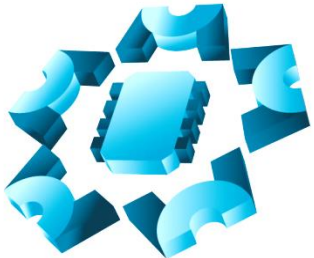
- Habilitar los Pines de los Puertos A y B como Analógicos
- REGISTROS ASOCIADOS

  Puerto A: ANSELA y TRISA

  Puerto B: ANSELB y TRISB



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Configuración del Registro ANSELA

REGISTER 12-7: ANSELA: PORTA ANALOG SELECT REGISTER

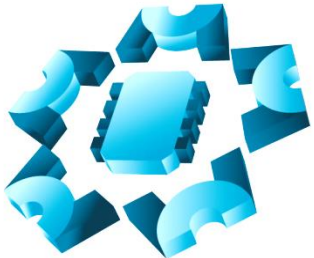
U-0	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **ANSA<4:0>**: Analog Select between Analog or Digital Function on pins RA<4:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

0	0	0	1	1	1	1	1



MECATRONICA DIGITAL

Configuración del Registro ANSELB

REGISTER 12-12: ANSELB: PORTB ANALOG SELECT REGISTER

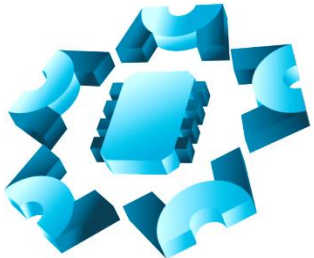
R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0
ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	—
bit 7							bit 0

bit 7-1 **ANSB<7:1>**: Analog Select between Analog or Digital Function on Pins RB<7:1>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

bit 0 **Unimplemented:** Read as '0'

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

1	1	1	1	1	1	1	0



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Configuración del Registro TRISA

REGISTER 12-4: TRISA: PORTA TRI-STATE REGISTER

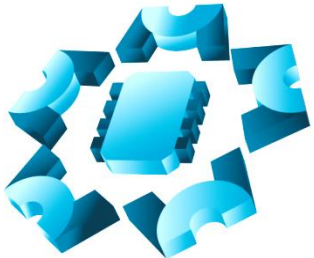
R/W-1/1	R/W-1/1	R-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

bit 7-6 **TRISA<7:6>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

bit 5 **TRISA5:** RA5 Port Tri-State Control bit
This bit is always '1' as RA5 is an input only

bit 4-0 **TRISA<4:0>:** PORTA Tri-State Control bit
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

0	0	0	1	1	1	1	1



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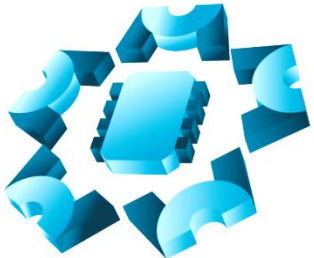
Configuración del Registro TRISB

REGISTER 12-9: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

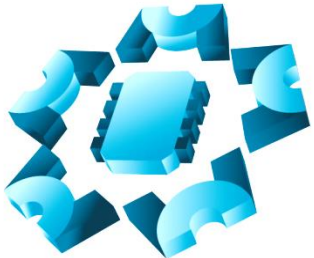
bit 7-0 **TRISB<7:0>:** PORTB Tri-State Control bit
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

1	1	1	1	1	1	1	0



MECATRONICA DIGITAL

Selección del Canal



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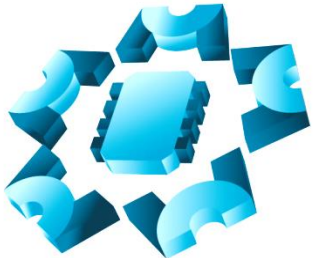
Existen 14 selecciones de canal disponibles:

- Pines Analógicos – AN<11:0>
- Salida DAC (Convertidor Digital Analógico)
- Salida FVR (Voltaje de Referencia Fijo)



MECATRONICA
DIGITAL

Los bits CHS del Registro ADCON0 determinan que canal esta conectado al circuito de muestreo:

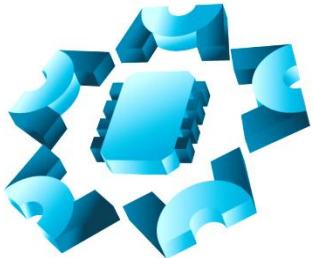
- **Cuando se cambian los canales, un retardo es requerido antes de la siguiente conversión.

Configuración del Registro ADCON0

REGISTER 15-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

0	0	0	0	0	0	0	1



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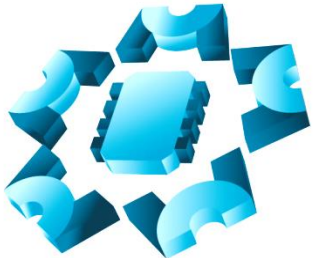
Configuración del Registro ADCON0

bit 7 **Unimplemented:** Read as '0'

bit 6-2 **CHS<4:0>:** Analog Channel Select bits

00000 = AN0
00001 = AN1
00010 = AN2
00011 = AN3
00100 = AN4
00101 = AN5
00110 = AN6
00111 = AN7
01000 = AN8
01001 = AN9
01010 = AN10
01011 = AN11
01100 = Reserved. No channel connected.
•
•
•
11101 = Reserved. No channel connected.
11110 = DAC output(1)
11111 = FVR (Fixed Voltage Reference) Buffer 1 Output(2)

0	0	0	0	0	0		



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Configuración del Registro ADCON0

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.

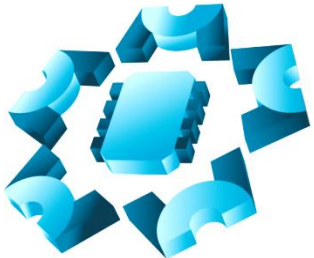
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit

1 = ADC is enabled

0 = ADC is disabled and consumes no operating current

0	0	0	0	0	0	0	1



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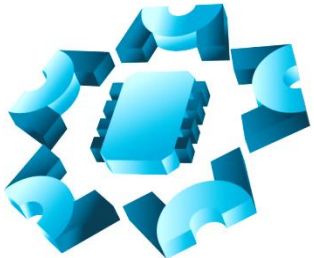
Selección del Voltaje de Referencia



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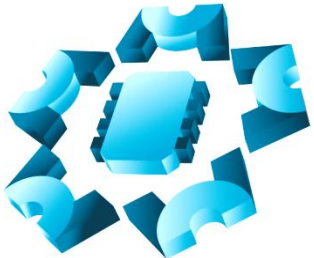
- El Voltaje de Referencia del ADC puede ser generado internamente por software o externamente suministrado.

- En esta ocasión se trabajará con el voltaje externamente suministrado por el programador.

- Para manejar generar internamente un voltaje, vea la seccion 14.0 “FRV (Voltaje de Referencia Fijo)



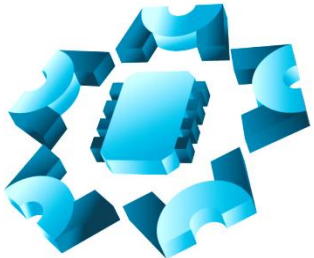
MECATRONICA
DIGITAL

- **Los Bits ADPREF del registro ADCON1 proporcionan el control del Voltaje de Referencia Positivo. El cual puede ser:**

- VREF + Pin
- VDD
- FVR 2.028V
- FVR 4.096V

- **Los Bits ADNREF del registro ADCON1 proporcionan el control del Voltaje de Referencia Negativo. El cual puede ser:**

- VREF + Pin
- VSS



MECATRONICA
DIGITAL

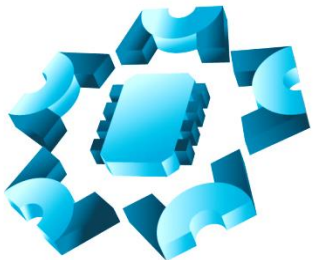
Configuración del Registro ADCON1

Voltaje de Referencia

REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

				0	0	0	0



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Configuración del Registro ADCON1

Voltaje de Referencia

REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

bit 3 **Unimplemented:** Read as '0'

bit 2 **ADNREF:** A/D Negative Voltage Reference Configuration bit
0 = V_{REF-} is connected to V_{SS}
1 = V_{REF-} is connected to external V_{REF-} pin(1)

bit 1-0 **ADPREF<1:0>:** A/D Positive Voltage Reference Configuration bits
00 = V_{REF+} is connected to V_{DD}
01 = Reserved
10 = V_{REF+} is connected to external V_{REF+} pin(1)
11 = V_{REF+} is connected to internal Fixed Voltage Reference (FVR) module

				0	0	0	0

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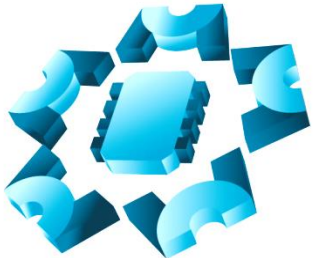
Selección de la Fuente de Reloj para la Conversión



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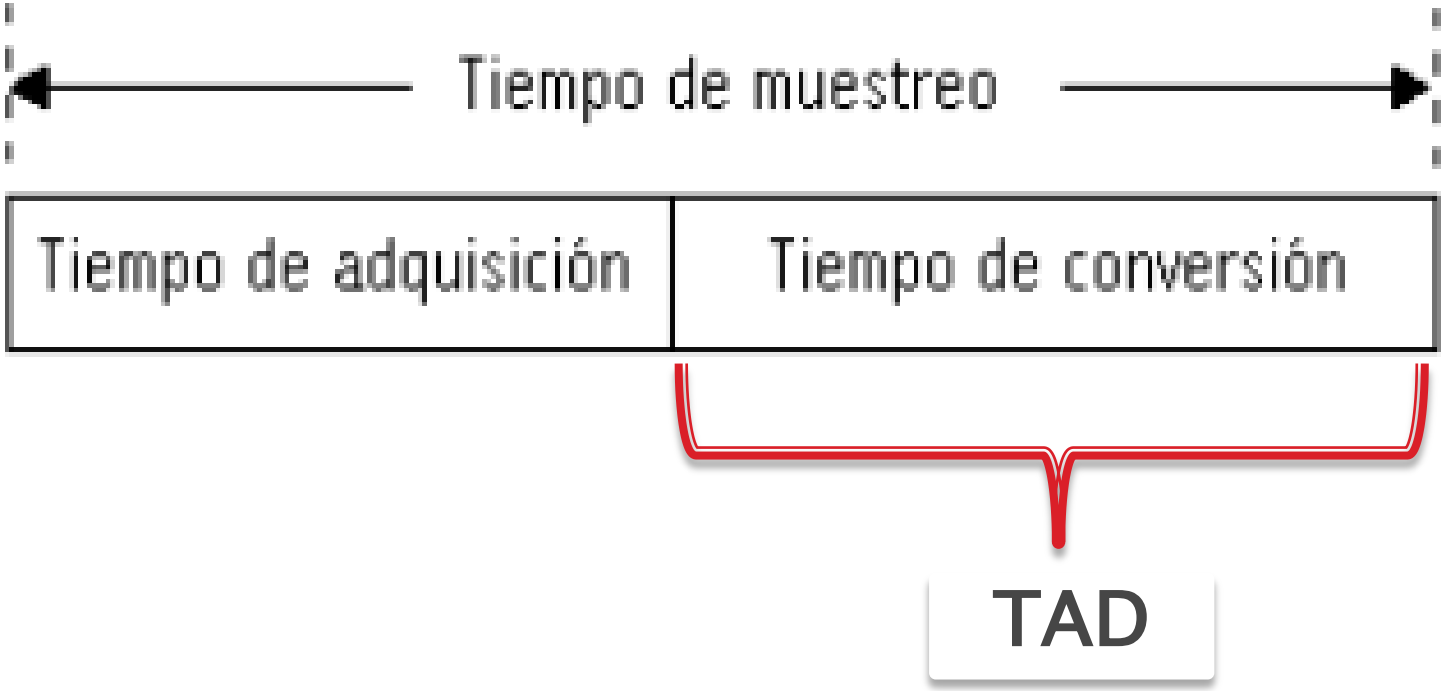

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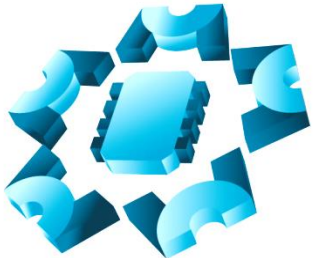
- **La Fuente de Reloj de Conversión es ajustable por software a través de los bits ADCS del registro ADCON1. Existen 7 posibles opciones de Reloj.**

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (Oscilador Interno Dedicado)



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- El tiempo para completar una conversión de bits se define como TAD.

- Una conversión de 10 bits requiere 11.5 periodos TAD.

FIGURE 15-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

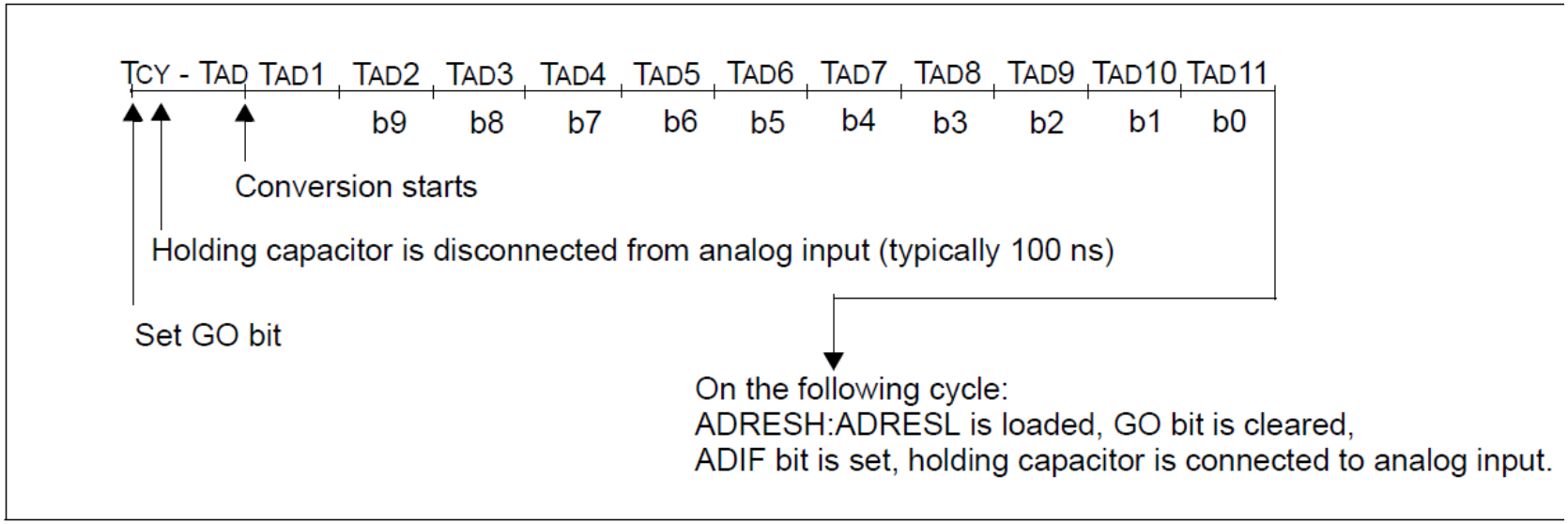

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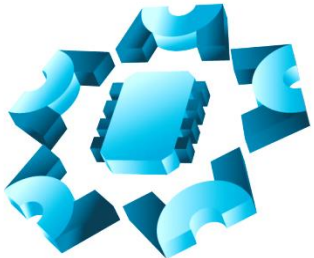
TABLE 15-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

ADC Clock Period (TAD)		Device Frequency (FOSC)					
ADC Clock Source	ADCS<2:0>	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
Fosc/2	000	62.5ns(2)	100 ns(2)	125 ns(2)	250 ns(2)	500 ns(2)	2.0 µs
Fosc/4	100	125 ns(2)	200 ns(2)	250 ns(2)	500 ns(2)	1.0 µs	4.0 µs
Fosc/8	001	0.5 µs(2)	400 ns(2)	0.5 µs(2)	1.0 µs	2.0 µs	8.0 µs(3)
Fosc/16	101	800 ns	800 ns	1.0 µs	2.0 µs	4.0 µs	16.0 µs(3)
Fosc/32	010	1.0 µs	1.6 µs	2.0 µs	4.0 µs	8.0 µs(3)	32.0 µs(3)
Fosc/64	110	2.0 µs	3.2 µs	4.0 µs	8.0 µs(3)	16.0 µs(3)	64.0 µs(3)
FRC	x11	1.0-6.0 µs(1,4)	1.0-6.0 µs(1,4)	1.0-6.0 µs(1,4)	1.0-6.0 µs(1,4)	1.0-6.0 µs(1,4)	1.0-6.0 µs(1,4)

- Las celdas sombreadas están fuera del rango recomendado.

- La fuente FRC tiene un tiempo TAD típico de 1.6 s por VDD.
- Para tiempos de conversiones mas rápidas se recomienda la selección de otra fuente de reloj.



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Configuración del Registro ADCON1

Fuente de Reloj del ADC

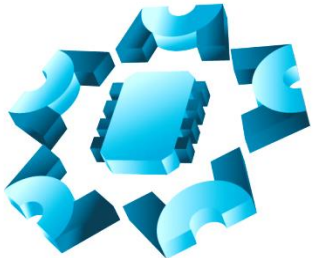
REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = Fosc/2
001 = Fosc/8
010 = Fosc/32
011 = FRC (clock supplied from a dedicated RC oscillator)
100 = Fosc/4
101 = Fosc/16
110 = Fosc/64
111 = FRC (clock supplied from a dedicated RC oscillator)

	1	1	1	0	0	0	0



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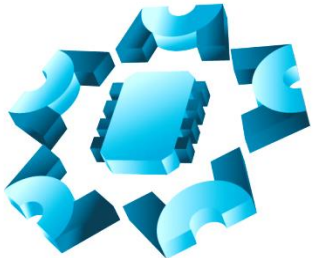
Selección del Formato del Resultado



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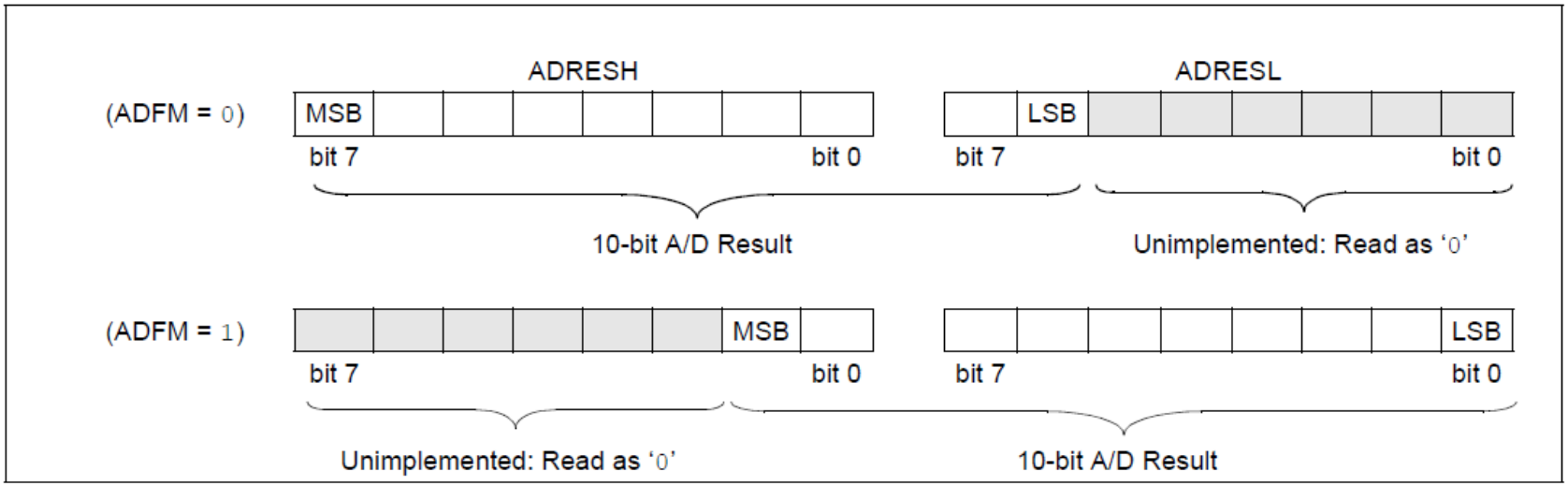
- **El resultado de la conversión analógica a digital de 10 bits, puede ser suministrada en 2 formatos:**

- Justificación a la Izquierda
- Justificación a la Derecha

- **El bit ADFM del registro ADCON1 controla el formato de salida**

FIGURE 15-3: 10-BIT A/D CONVERSION RESULT FORMAT



Configuración del Registro ADCON1
Selección del Formato de Resultado

REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

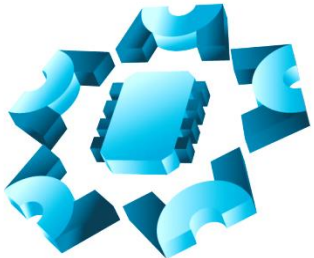
R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six Most Significant bits of ADRESH are set to '0' when the conversion result is loaded.

0 = Left justified. Six Least Significant bits of ADRESL are set to '0' when the conversion result is loaded.

0	1	1	1	0	0	0	0



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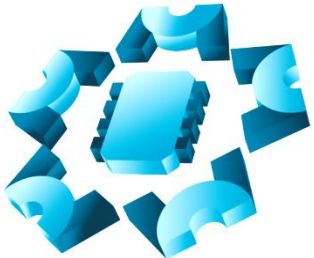
Configuración del Registro ADCON1

Valor Final

REGISTER 15-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

0	1	1	1	0	0	0	0



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GRACIAS POR SU ATENCION