200118X-UMUL simulation

Test bench for ALU

```
module ALU_tb;

 // Inputs
 logic [31:0] SrcA;
 logic [31:0] SrcB;
 logic [3:0]  Operation;

 // Outputs
 logic [31:0] ALUResult;
 logic Con_BLT;
 logic Con_BGT;
 logic zero;

 // Instantiate the ALU module
 ALU uut (
  .SrcA(SrcA),
  .SrcB(SrcB),
  .Operation(Operation),
  .ALUResult(ALUResult),
  .Con_BLT(Con_BLT),
  .Con_BGT(Con_BGT),
  .zero(zero)
 );

 // Initial block to apply test vectors
 initial begin
  // Test vector 1: UMUL
  SrcA = 10;
  SrcB = 5;
  Operation = 4'b1111; // UMUL
```

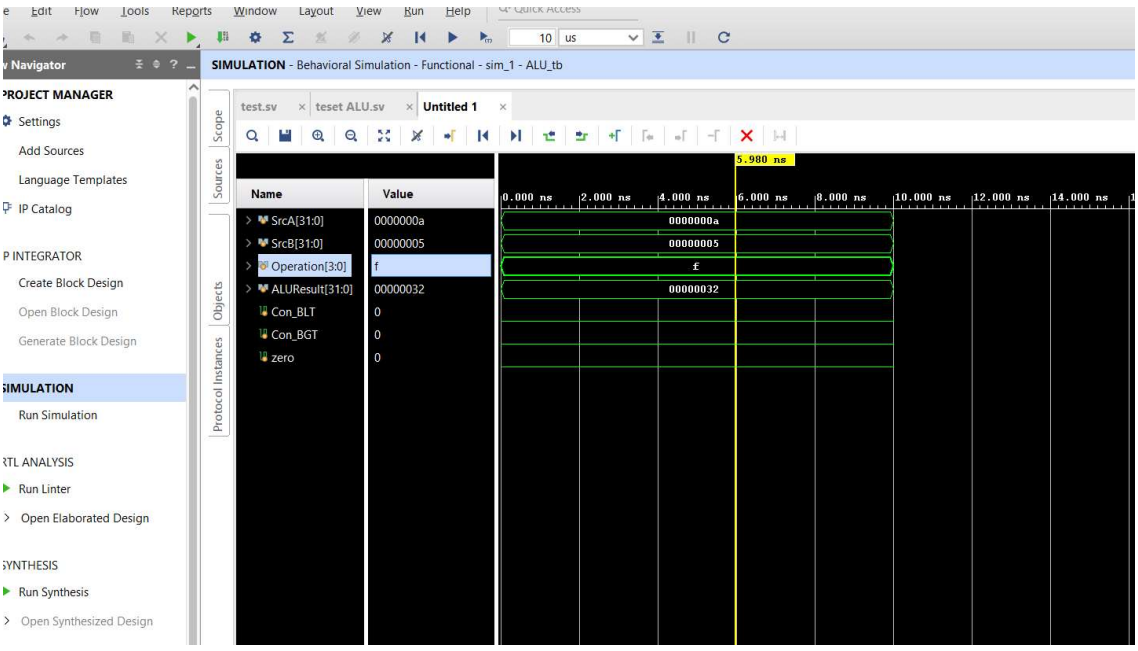
```
#10; // Wait for a few simulation cycles

// Check the result
if (ALUResult !== 50) begin
  $display("Test 1 failed! Expected ALUResult = 50, Actual ALUResult = %0d", ALUResult);
end else begin
  $display("Test 1 passed! ALUResult = %0d", ALUResult);
end

// Add more test vectors as needed

// Finish simulation
$finish;
end

endmodule
```



Another results for different Test bench

```
module ALU_tb;

 // Inputs
 logic [31:0] SrcA;
 logic [31:0] SrcB;
 logic [3:0]  Operation;

 // Outputs
 logic [31:0] ALUResult;
 logic Con_BLT;
 logic Con_BGT;
 logic zero;

 // Instantiate the ALU module
 ALU uut (
  .SrcA(SrcA),
  .SrcB(SrcB),
  .Operation(Operation),
  .ALUResult(ALUResult),
  .Con_BLT(Con_BLT),
  .Con_BGT(Con_BGT),
  .zero(zero)
 );

 // Initial block to apply test vectors
 initial begin
  // Test vector 1: AND
  SrcA = 32'hAAAA_5555;
  SrcB = 32'h5555_AAAA;
  Operation = 4'b0000; // AND
```

```
    #10; // Wait for a few simulation cycles

    // Check the result
    if (ALUResult !== 32'h0000_5055) begin
      $display("Test 1 failed! Expected ALUResult = 32'h0000_5055, Actual ALUResult = %h",
ALUResult);
    end else begin
      $display("Test 1 passed! ALUResult = %h", ALUResult);
    end

    // Test vector 2: UMUL
    SrcA = 6;
    SrcB = 5;
    Operation = 4'b1111; // UMUL

    #10; // Wait for a few simulation cycles


     // Test vector 2: UMUL
    SrcA = 2;
    SrcB = 5;
    Operation = 4'b1111; // UMUL

    #10; // Wait for a few simulation cycles
     // Test vector 2: UMUL
    SrcA = 6;
    SrcB = 10;
    Operation = 4'b1111; // UMUL

    #10; // Wait for a few simulation cycles
```

```
  // Check the result
  if (ALUResult !== 50) begin
    $display("Test 2 failed! Expected ALUResult = 50, Actual ALUResult = %0d", ALUResult);
  end else begin
    $display("Test 2 passed! ALUResult = %0d", ALUResult);
  end

  // Add more test vectors as needed

  // Finish simulation
  $finish;
 end

endmodule
```