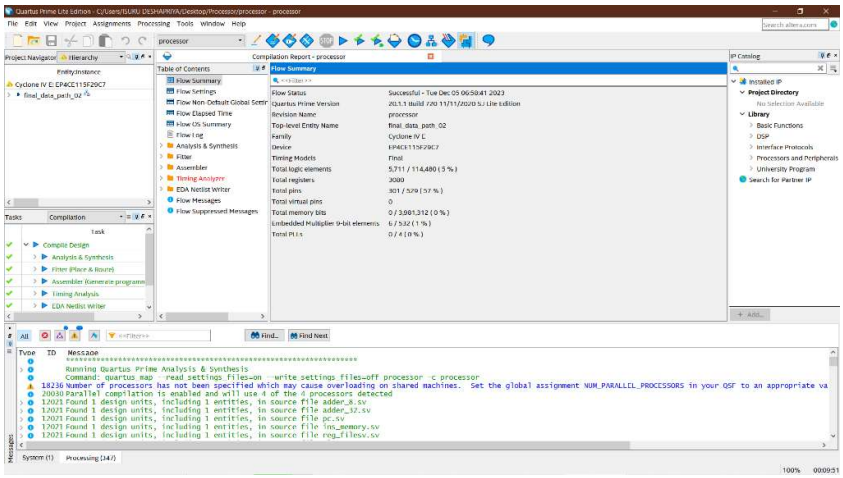
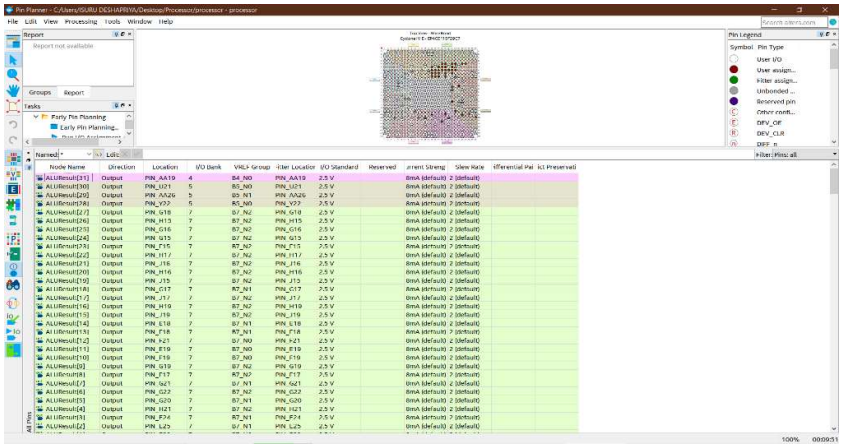
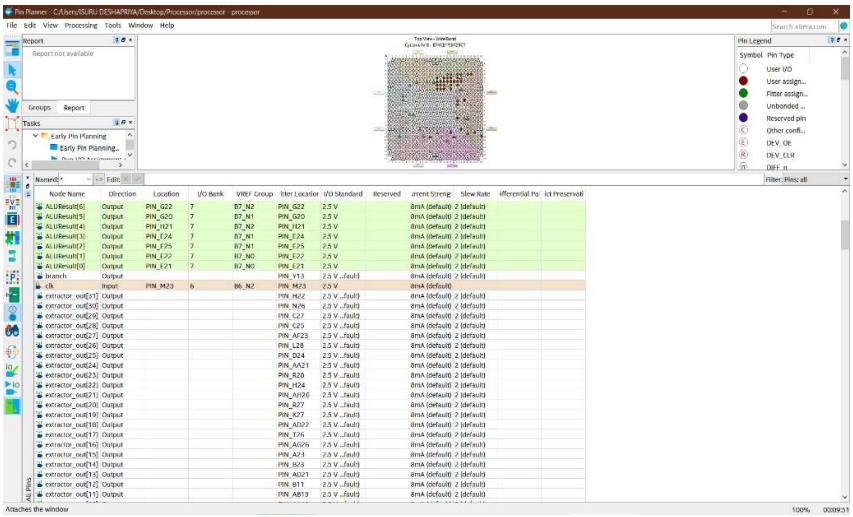
200118X-Deshapriya G.I

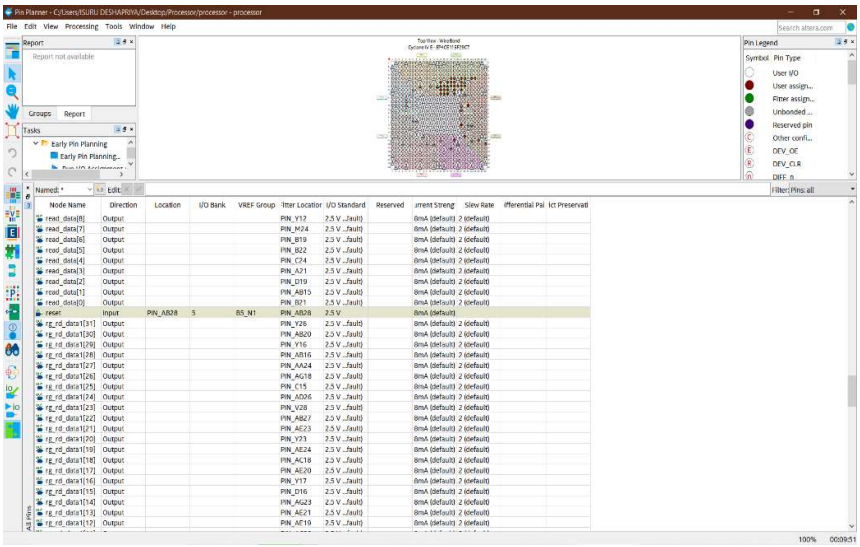
Implementation process



Pin assignment



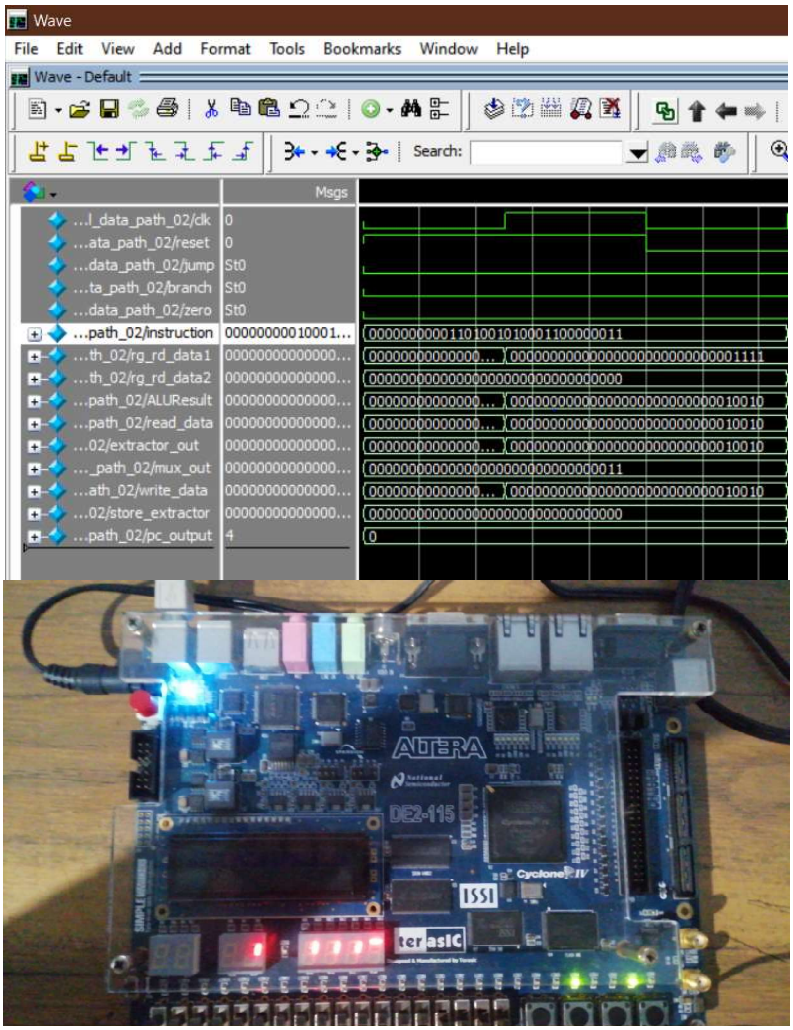




Simulation results, Implementation Results

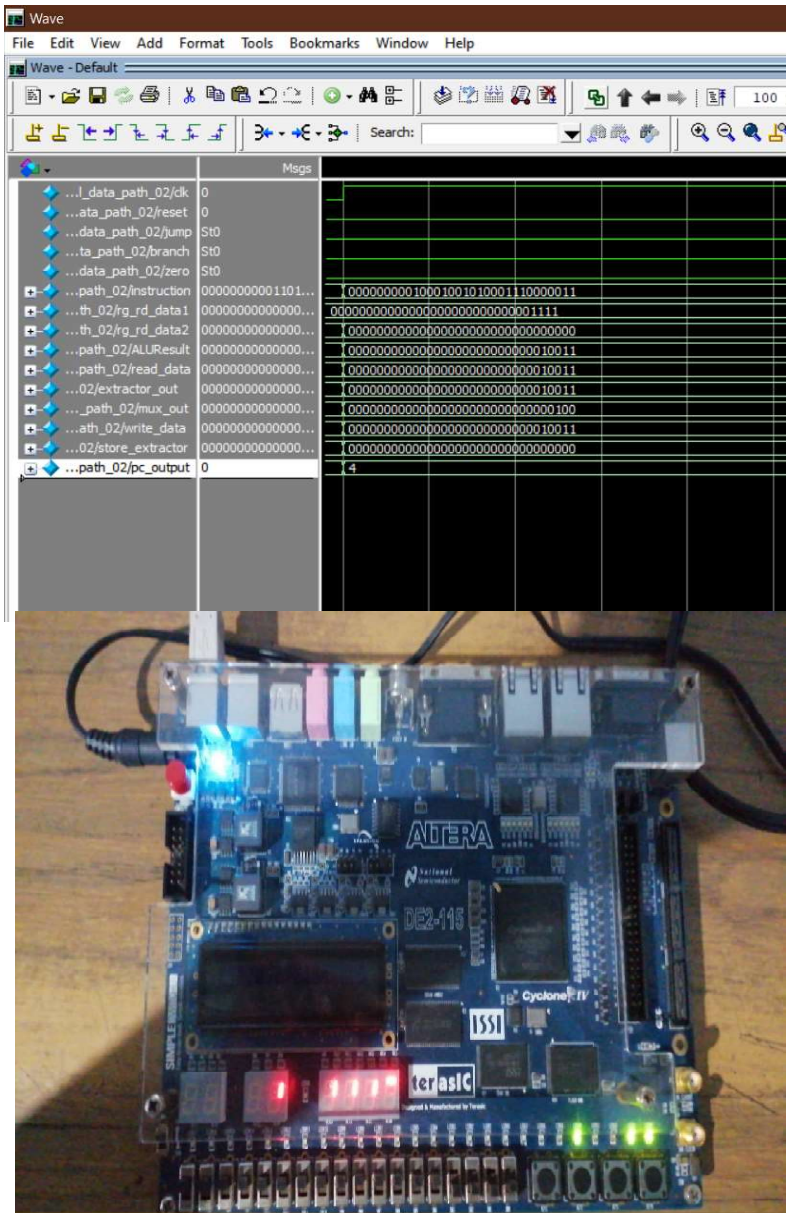
ins_mem[0] = 32'b000000000011_01001_010_00110_0000011; -----lw

Rs1 – 1001, rd = 110 Imm Value – 11 ,ALUResult = 11 + 1111 = 10010 .Read data = 10010 (store this in 110 register)



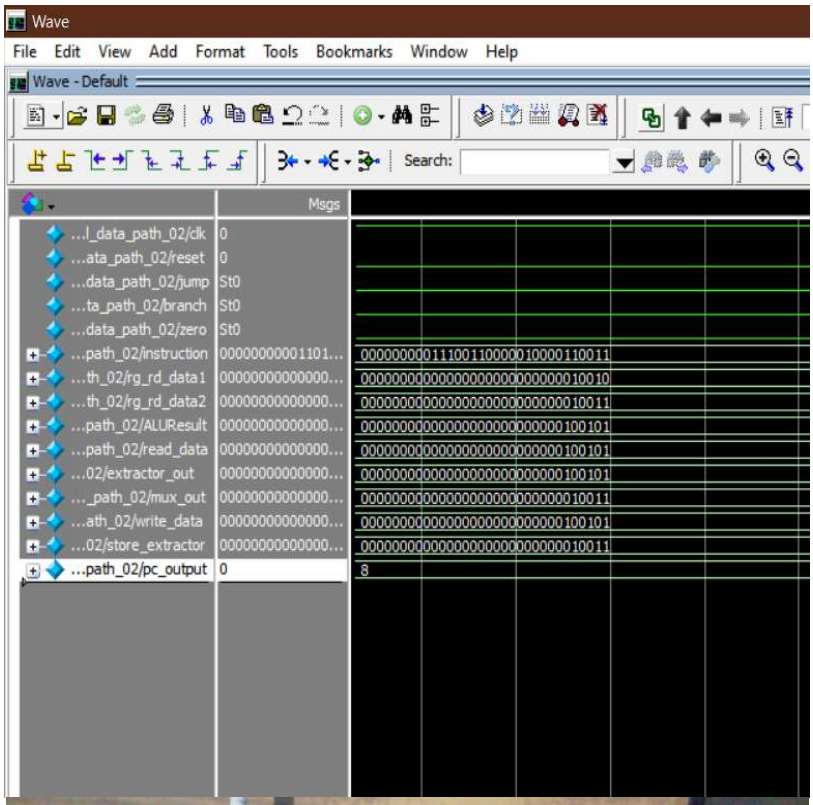
ins_mem[4] = 32'b000000000100_01001_010_00111_0000011; -----lw

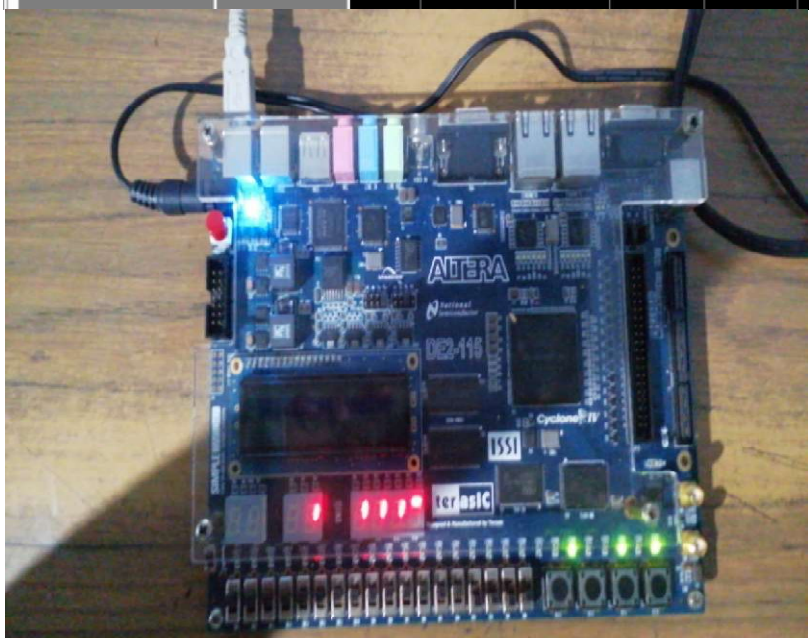
Rs1 – 1001 ,rd = 111, Imm Value – 100 ,ALUResult = 100 + 1111 = 10011 ,Read data = 10011 (store this in 111 register)



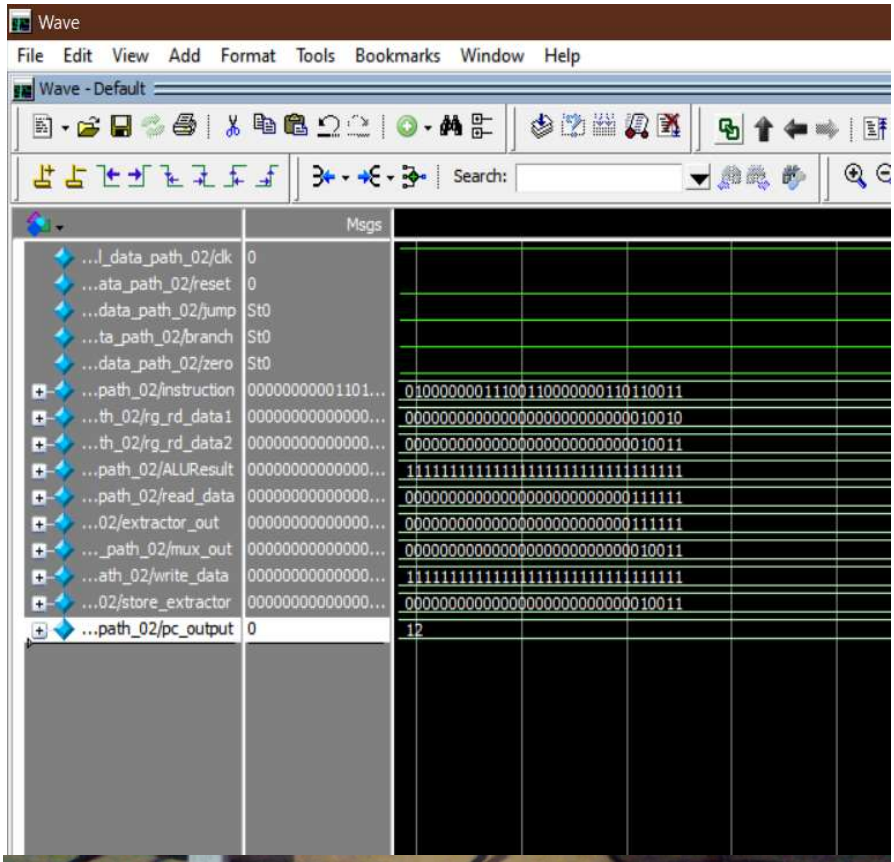
ins_mem[8] = 32'b0000000_00111_00110_000_01000_0110011; ----add

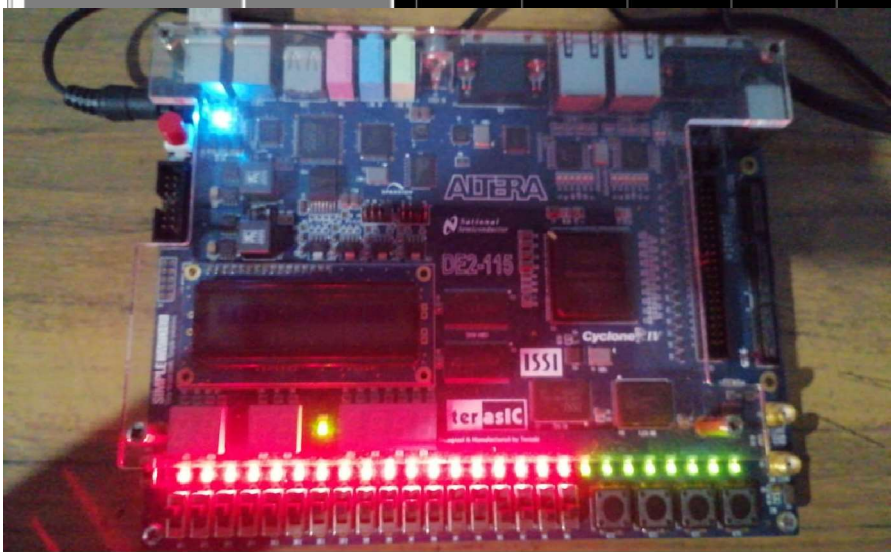
Rs1 – 110 (store value 10010), Rs2 - 111 (store value 10011) ,AluResult – 10010 + 10011 = 100101 (This shown in below) ,Rd – 1000 (store alu result in this register)



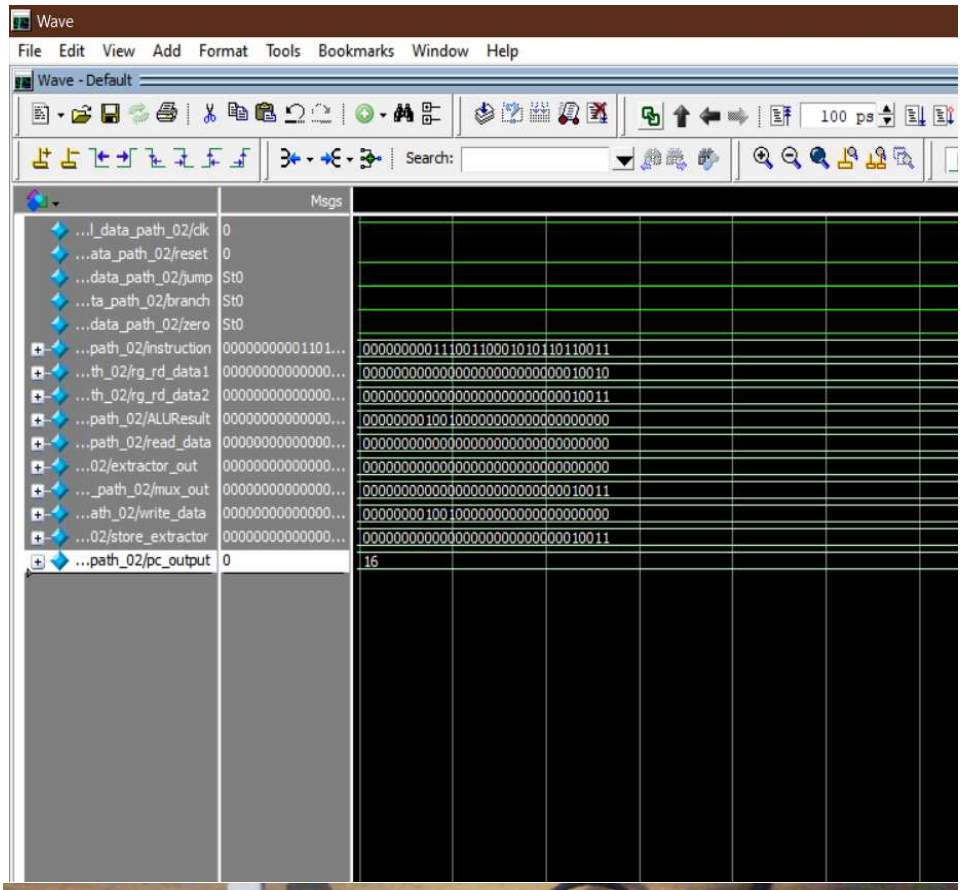


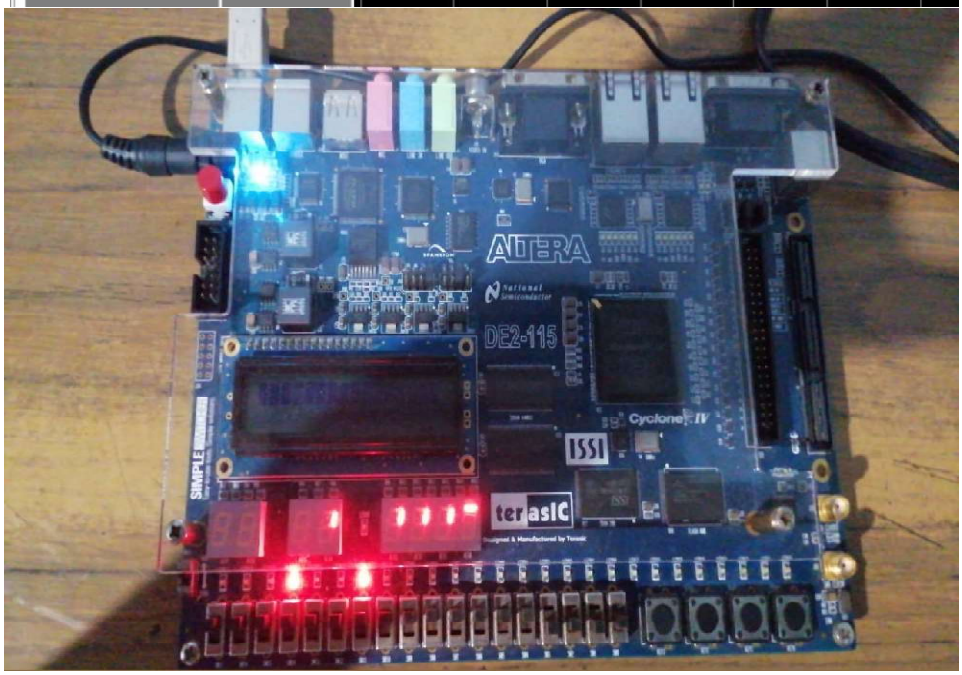
ins_mem[12] = 32'b0100000_00111_00110_000_00011_0110011; -----sub





ins_mem[16] = 32'b0000000_00111_00110_001_01011_0110011; //sll





assign ins_mem[20] = 32'b0000000_00111_00110_010_01000_0110011; //slt

assign ins_mem[24] = 32'b0000000_00111_00110_011_01111_0110011; //sltu

assign ins_mem[28] = 32'b0000000_00111_00110_100_01011_0110011; // xor

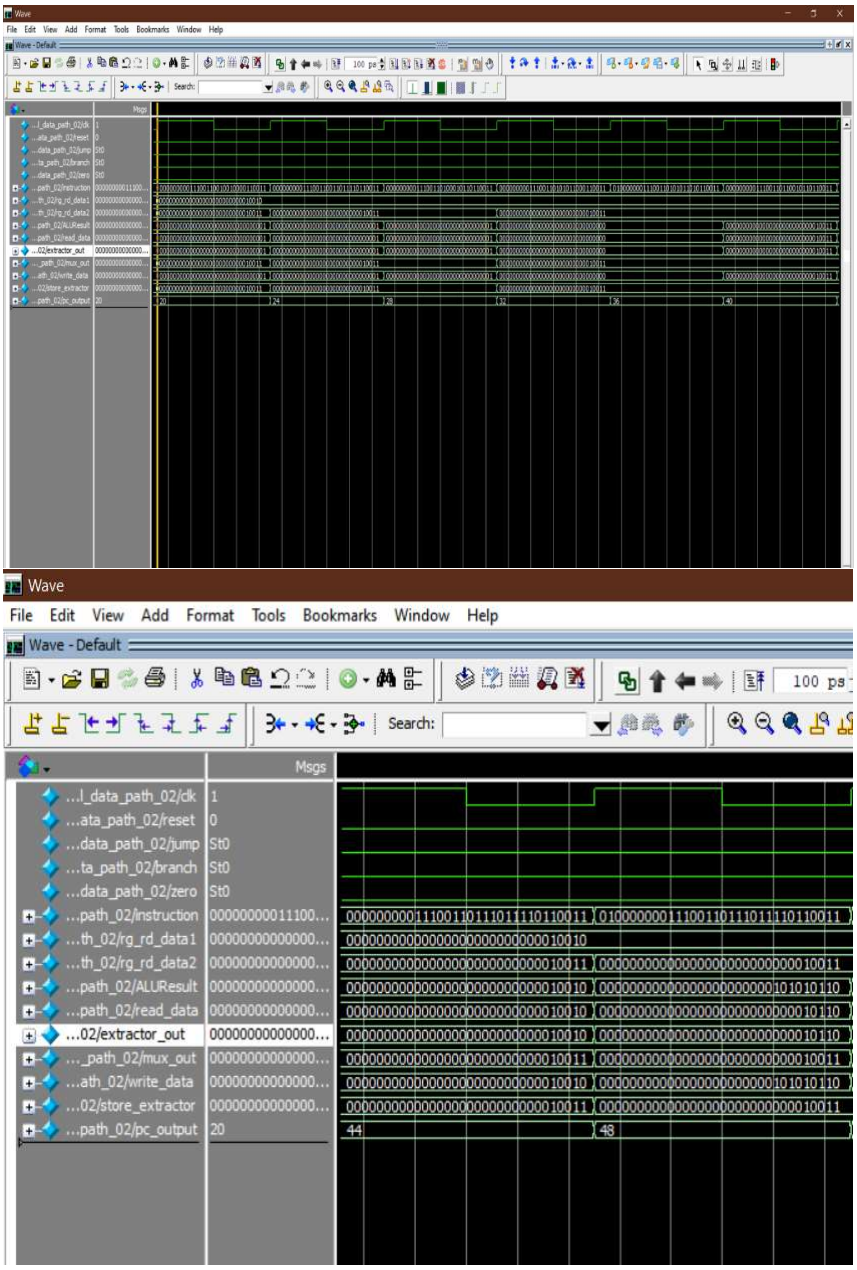
assign ins_mem[32] = 32'b0000000_00111_00110_101_01100_0110011;// srl

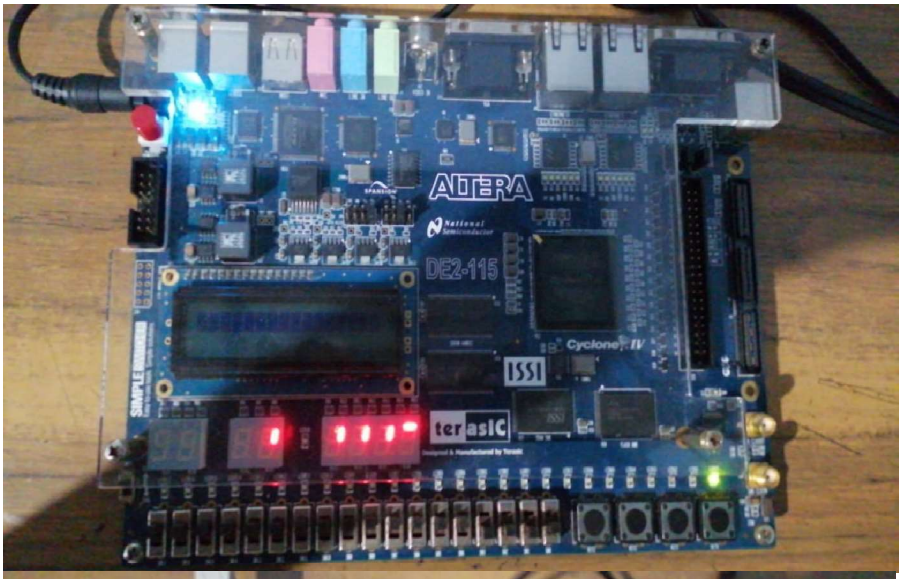
assign ins_mem[36] = 32'b0100000_00111_00110_101_01101_0110011;// sra

assign ins_mem[40] = 32'b0000000_00111_00110_110_01011_0110011;// or

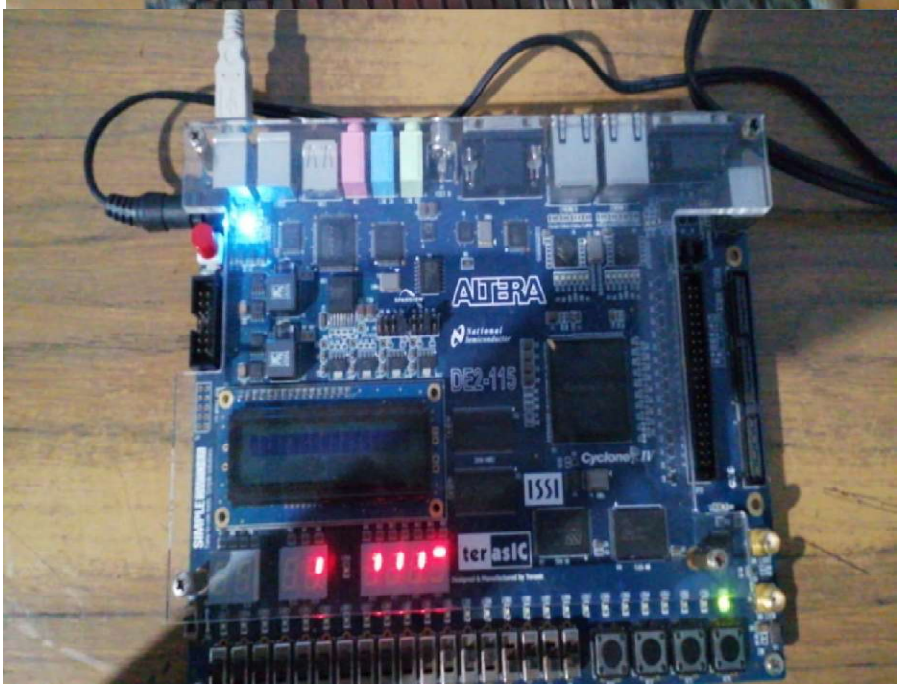
assign ins_mem[44] = 32'b0000000_00111_00110_111_01111_0110011;// and

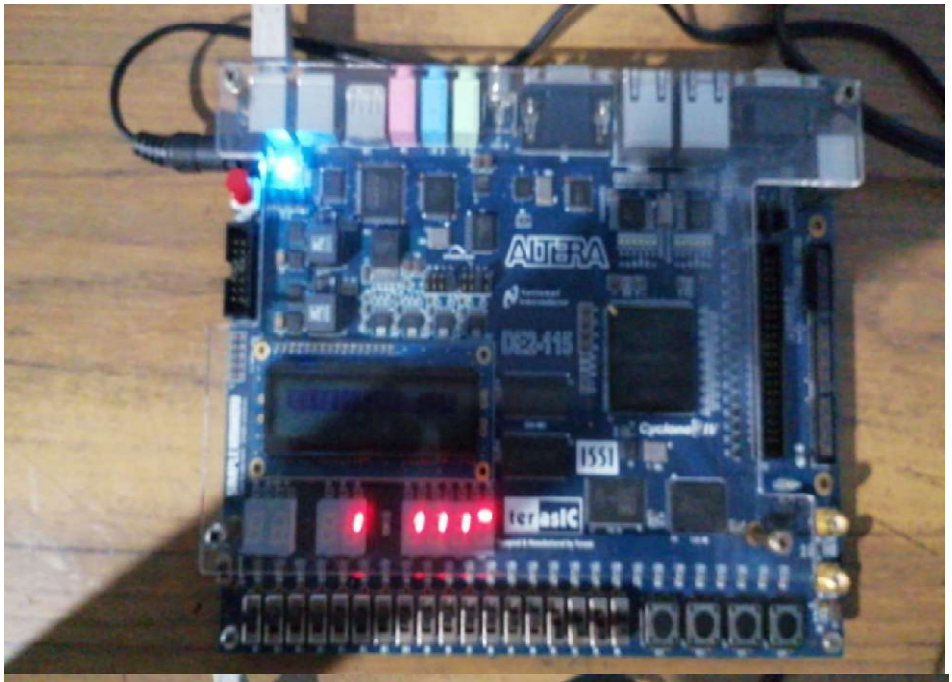
assign ins_mem[48] = 32'b0100000_00111_00110_111_01111_0110011;// mul




ALTERA
DE2-115
Cyclone IV
ISSI
terasIC


ALTERA
terasIC


ALTERA
DE2-115
Cyclone IV
ISSI
terasIC


ALTERA
DE2-115
ISSI
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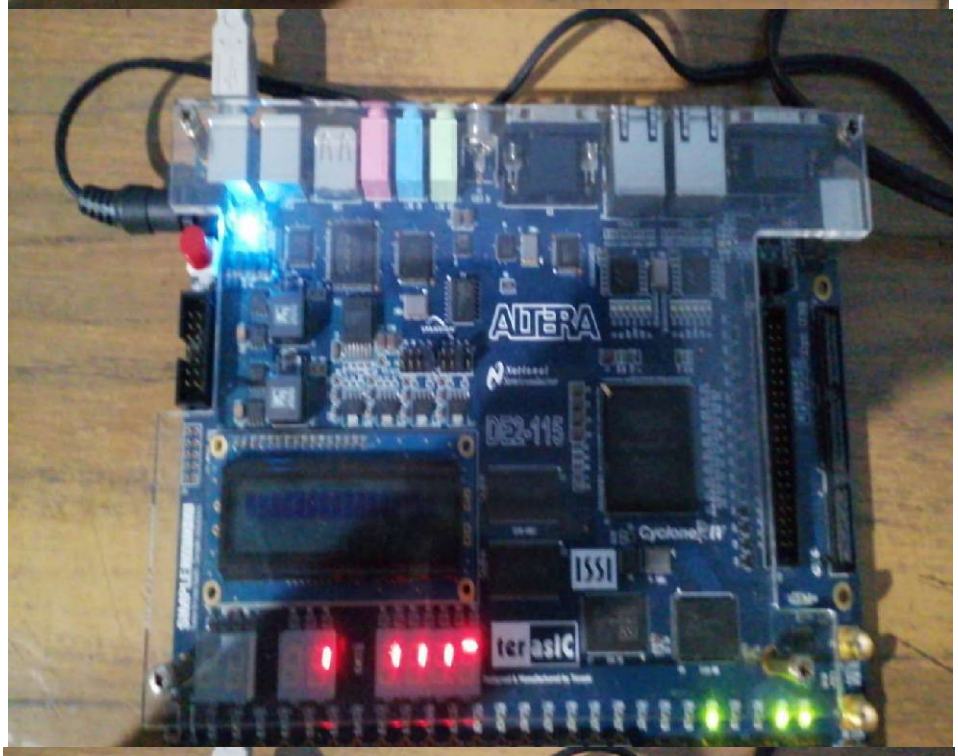
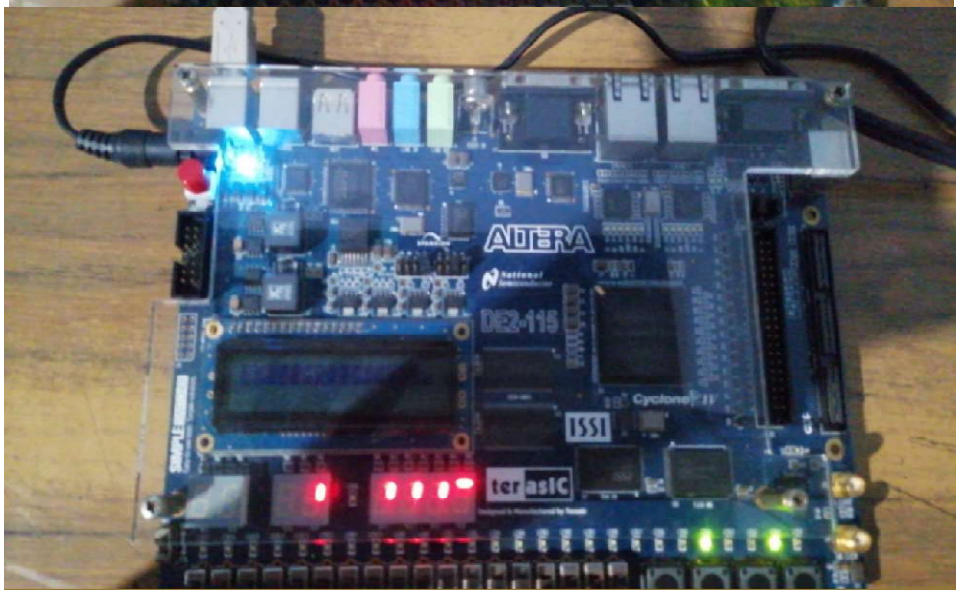
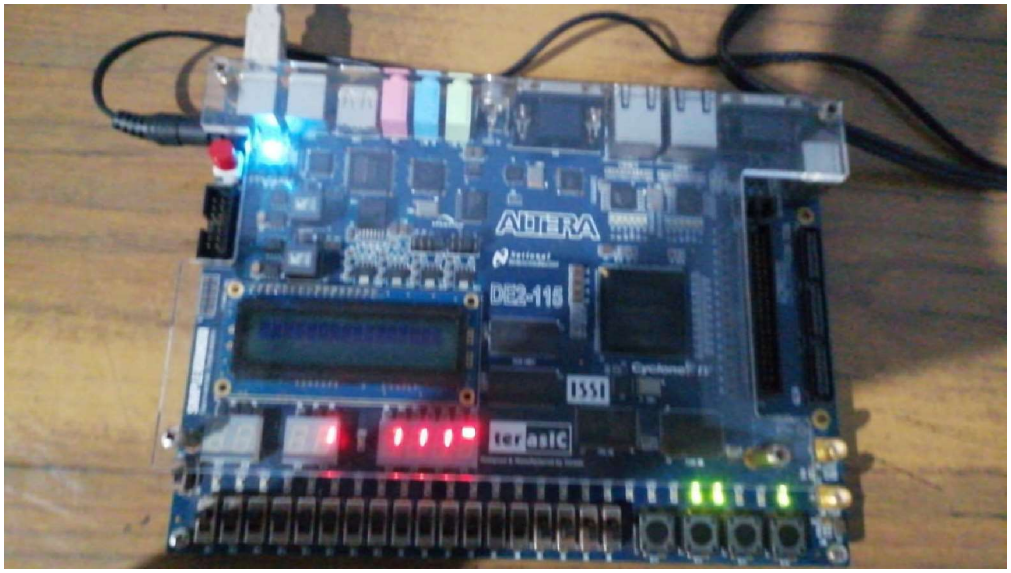

ALTERA
DE2-115
ISSI
terasIC


ALTERA
DE2-115
ISSI
terasIC

assign ins_mem[52] = 32'b000000000111_00110_000_00100_0010011;//addi//

----addi----Rs1 – 110 (store value 10010) Rd – 100 Immediate – 111, ALUResult – 11001



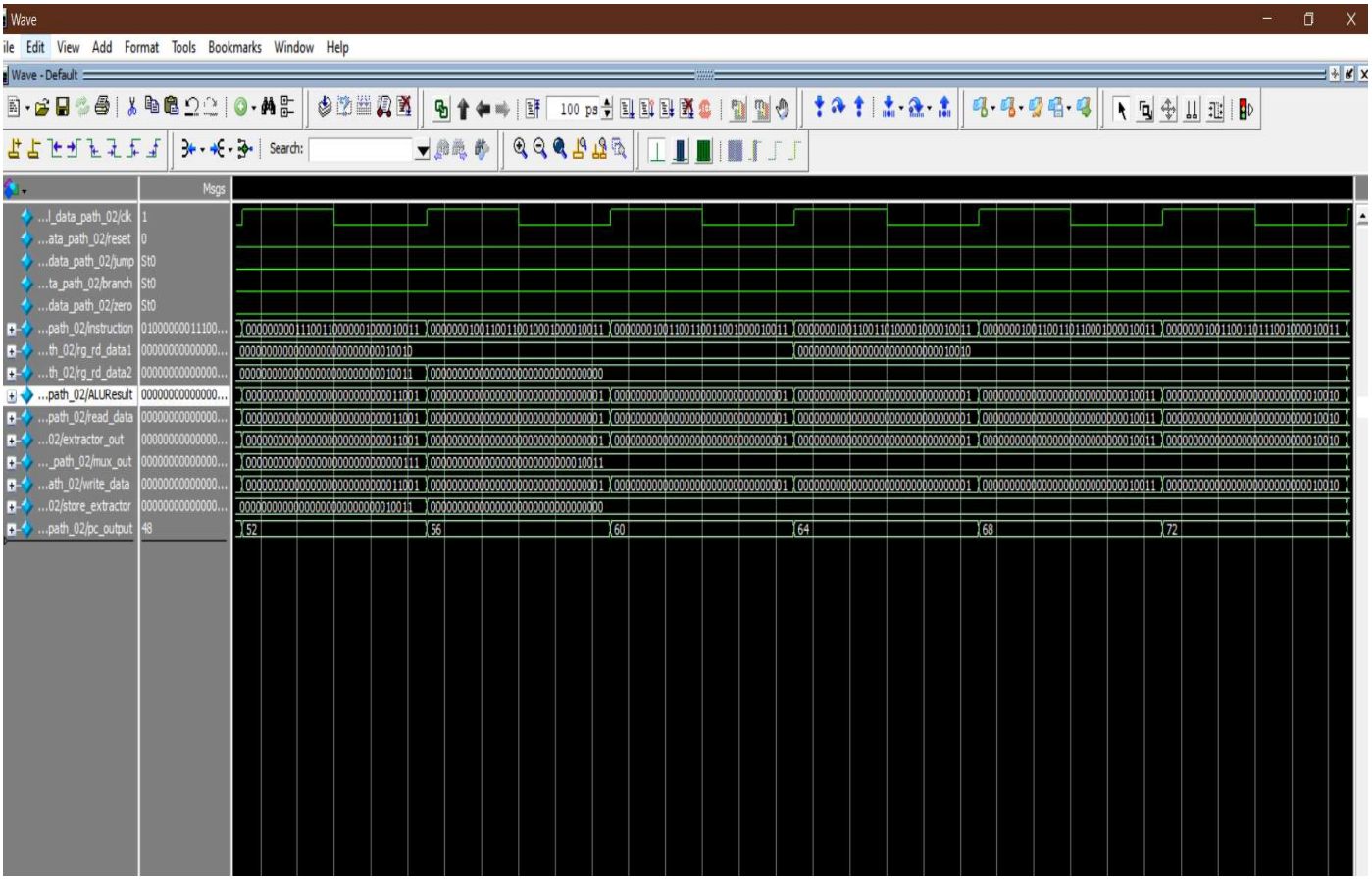
assign ins_mem[56] = 32'b000000010011_00110_010_00100_0010011;//slti

assign ins_mem[60] = 32'b000000010011_00110_011_00100_0010011;//sltiu

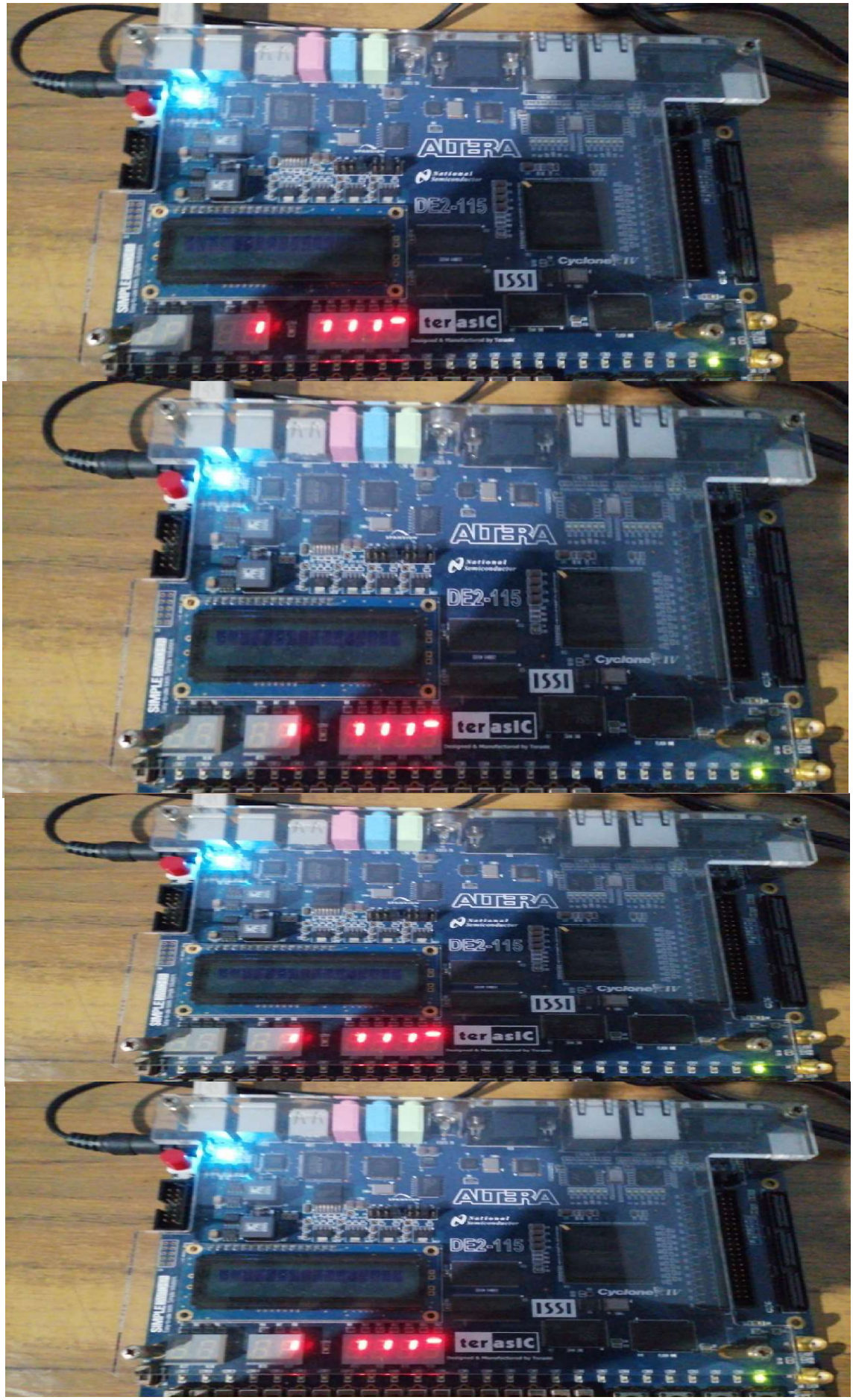
assign ins_mem[64] = 32'b000000010011_00110_100_00100_0010011;//xori

assign ins_mem[68] = 32'b000000010011_00110_110_00100_0010011;//ori

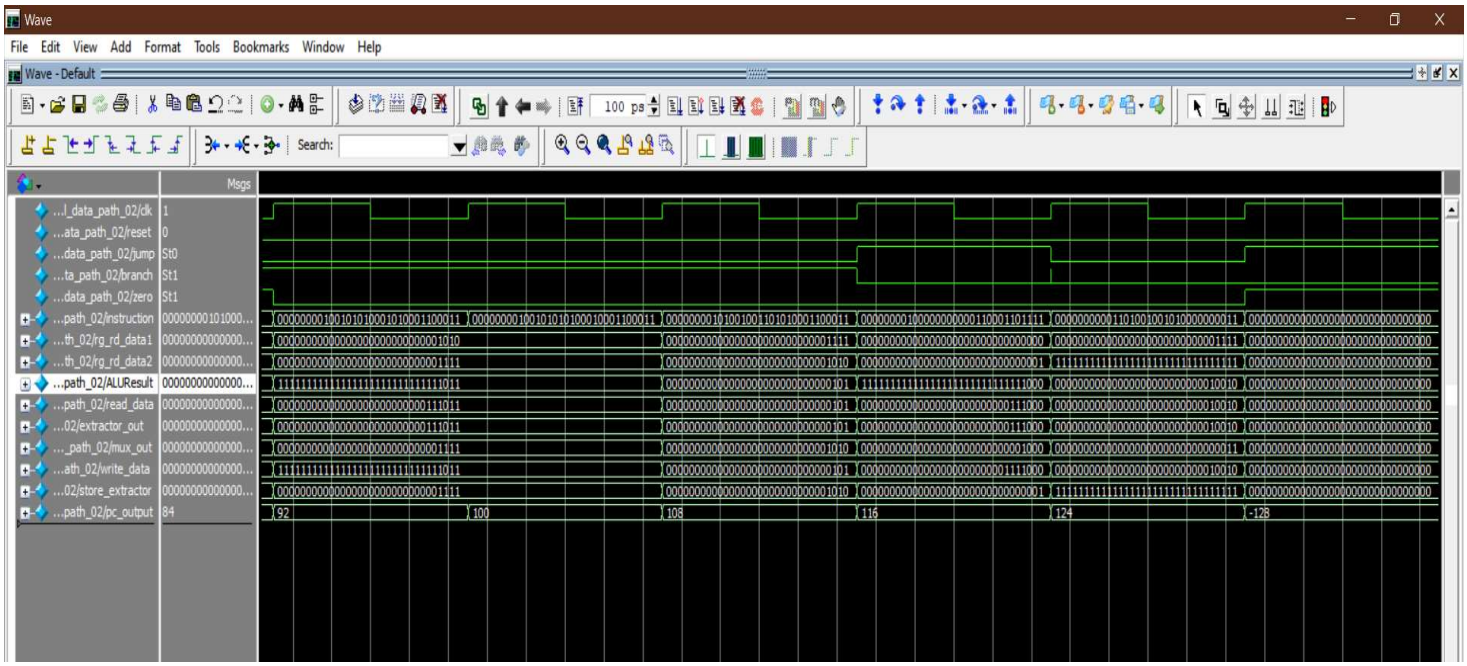
assign ins_mem[72] = 32'b000000010011_00110_111_00100_0010011;//andi



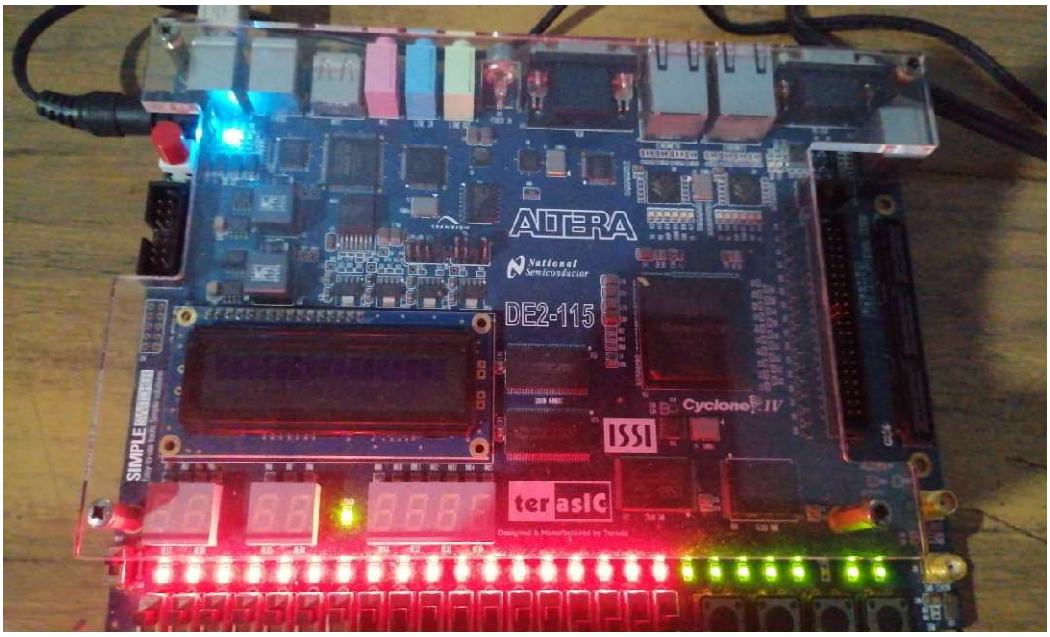
56----64



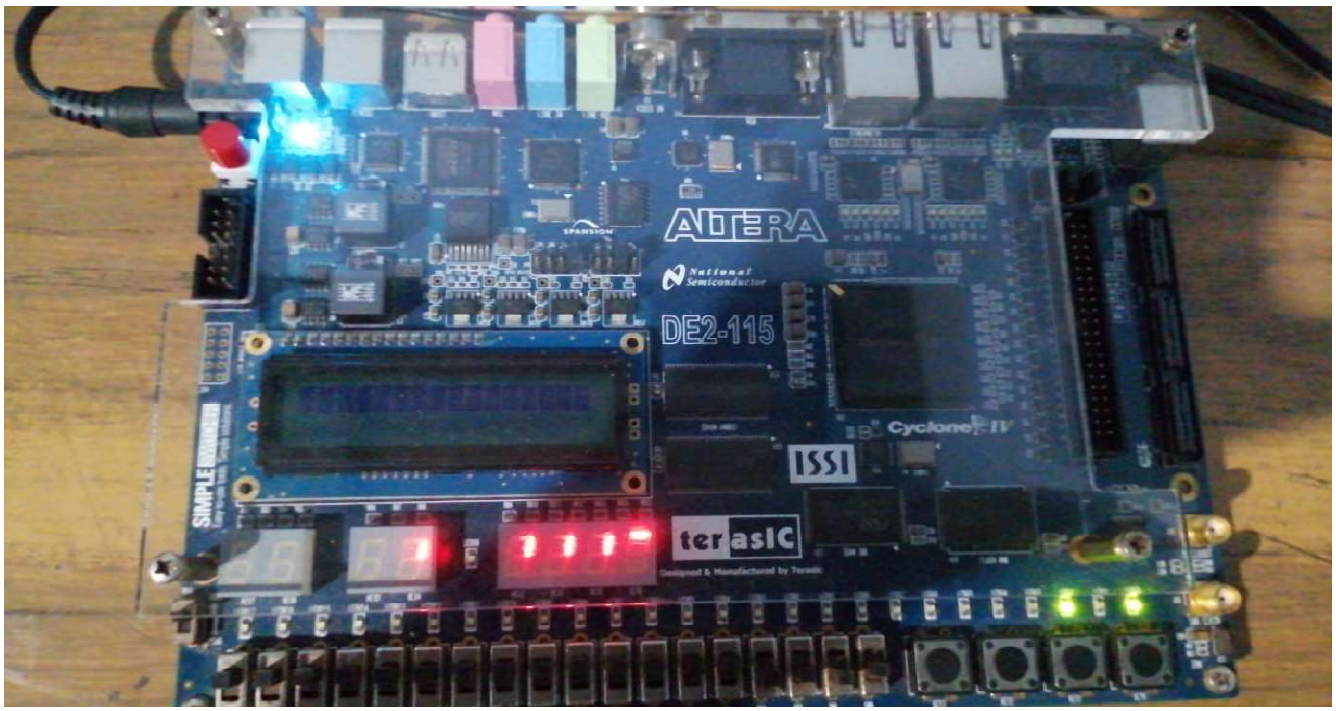
Some other results



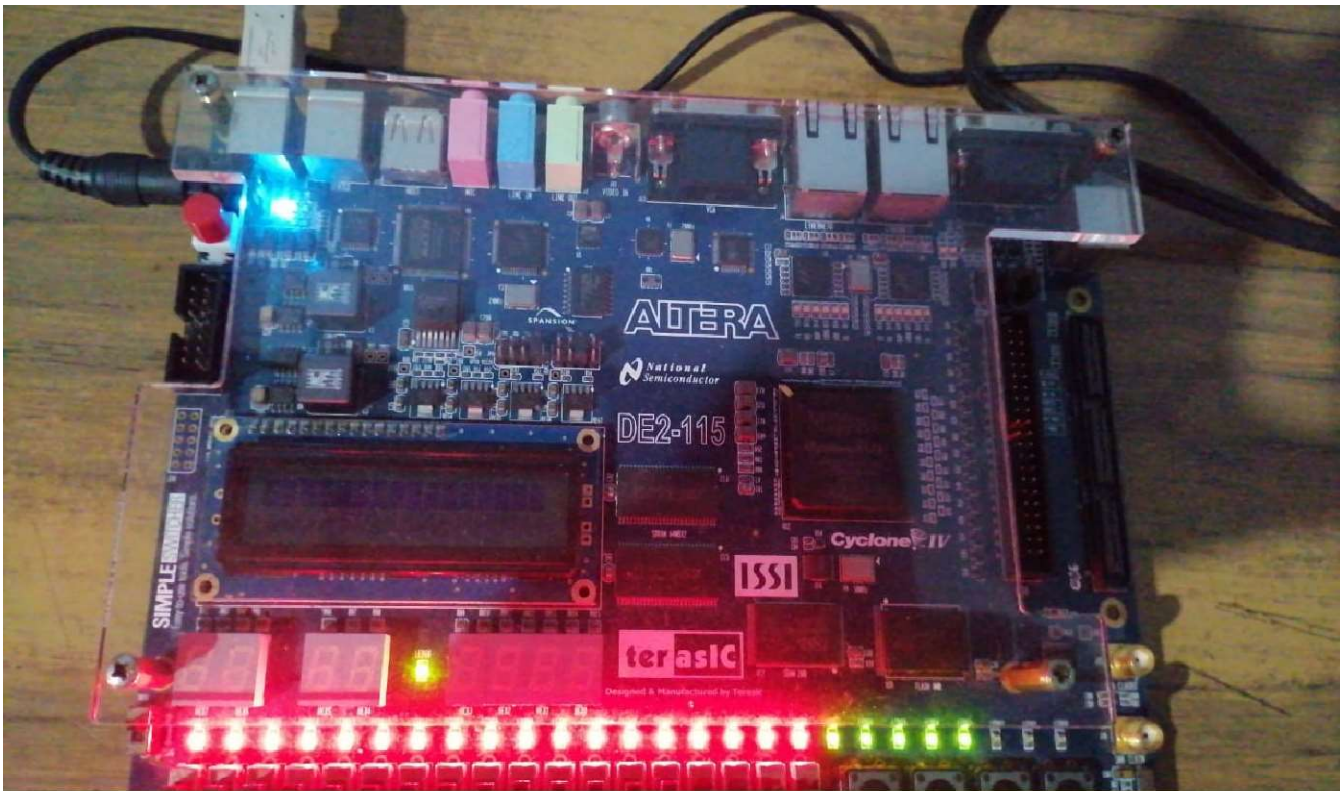
assign ins_mem[92] = 32'b0000000_01001_01010_001_01000_1100011;//bne



assign ins_mem[108] = 32'b0000000_01010_01001_101_01000_1100011;//bgt



assign ins_mem[116] = 32'b0000000_01000_00000_000_11000_1101111; //jal



assign ins_mem[124] = 32'b000000000011_01001_001_01000_0000011;//lh