COMPILER DESIGN

Paper Code: ETCS-302	**L**	**T/P**	**C**
Paper: Compiler Design	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should

Objective: This course aims to teach students the principles involved in compiler design. It will cover all the basic components of a compiler, its optimizations and machine code generation. Students will be able to design different types of compiler tools to meet the requirements of the realistic constraints of compilers.

UNIT- I

Brief overview of the compilation process, structure of compiler & its different phases, lexical analyzer, cross compiler, Bootstrapping, quick & dirty compiler, Shift-reduce parsing, operator- precedence parsing, top-down parsing, predictive parsing ,LL(1) and LL(k) grammar, bottom up parsing, SLR, LR(0), LALR parsing techniques.

[T1][T2][R1][No. of Hrs. 12]

UNIT- II

Design and implementation of a lexical analyzer and parsing using automated compiler construction tools(eg. Lex, YACC, PLY), Syntax-directed translation schemes, implementation of syntax directed translations, intermediate code, postfix notation, three address code, quadruples, and triples, translation of assignment statements, Boolean expressions, control statements, Semantic Analysis, Type Systems, Type Expressions, Type Checker, Type Conversion

[T2][R1][R3][R4][R5][No. of Hrs. 12]

UNIT- III

Symbol table, data structures and implementation of symbol tables, representing scope information.

Run Time Storage Administration, implementation of a simple stack allocation scheme, storage allocation in block structured languages and non block structured languages, Error, Lexical-phase errors, syntactic-phase errors, semantic errors.

[T1][T2]][R2][No. of Hrs. 10]

UNIT-IV

The principle sources of optimization, loop optimization, the DAG representation of basic blocks, value number and algebraic laws, global dataflow analysis, Object programs, problems in code generation, a machine model, a single code generator, register allocation and assignment, code generation from DAGs, peephole optimization.

[T1][T2] [No. of Hrs. 10]

Text Books:

[T1] Alfred V. Aho & J.D. Ullman, “Compiler Principles ,Techniques& Tools”, Pearson

[T2] Kenneth C. Louden, “Compiler Design”,Cengage Publication

Reference Books:

[R1] Kakde O.G., “Complier Design”, Laxmi Publication

[R2] Trembley and Sorenson, “Theory and Practice of Compiler Writing”, McGraw Hill

[R3] Vinu V. DAS, “Compiler Design Using FLEX and YACC , PHI

[R4] Jhon R. Levine, Tony Mason and Doug Brown, “Lex &Yacc”, O’Reilly.pdf

[R5] Andrew W. Appel, Maia Ginsburg, “Modern Compiler Implementation in C”, Cambridge University Press

OPERATING SYSTEMS

Paper Code: ETCS-304	**L**	**T/P**	**C**
Paper: Operating Systems	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should

Objective: *The goal of this course is to provide an introduction to the internal operation of modern operating systems. The course will cover processes and threads, mutual exclusion, CPU scheduling, deadlock, memory management, and file systems.*

UNIT I

Introduction: What is an Operating System, Simple Batch Systems, Multiprogrammed Batches systems, Time-Sharing Systems, Personal-computer systems, Parallel systems, Distributed Systems, Real-Time Systems, OS – A Resource Manager.

Memory Organization & Management: Memory Organization, Memory Hierarchy, Memory Management Strategies, Contiguous versus non- Contiguous memory allocation, Partition Management Techniques, Logical versus Physical Address space, swapping, Paging, Segmentation, Segmentation with Paging

Virtual Memory: Demand Paging, Page Replacement, Page-replacement Algorithms, Performance of Demand Paging, Thrashing, Demand Segmentation, and Overlay Concepts.

[T1] [T2][R2][R3] [No. of hrs. 10]

UNIT II

Processes: Introduction, Process states, process management, Interrupts, Interprocess Communication

Threads: Introduction, Thread states, Thread Operation, Threading Models.

Processor Scheduling: Scheduling levels, pre emptive vs no pre emptive scheduling, priorities, scheduling objective, scheduling criteria, scheduling algorithms, demand scheduling, real time scheduling.

Process Synchronization: Mutual exclusion, software solution to Mutual exclusion problem, hardware solution to Mutual exclusion problem, semaphores, Critical section problems. Case study on Dining philosopher problem, Barber shop problem etc.

[T1][T2][[R3] [No. of hrs. 10]

UNIT III

Deadlocks: examples of deadlock, resource concepts, necessary conditions for deadlock, deadlock solution, deadlock prevention, deadlock avoidance with Bankers algorithms, deadlock detection, deadlock recovery.

Device Management: Disk Scheduling Strategies, Rotational Optimization, System Consideration, Caching and Buffering

[T1][T2][R1] [No. of hrs. 10]

UNIT IV

File System: Introduction, File Organization, Logical File System, Physical File System , File Allocation strategy, Free Space Management, File Access Control, Data Access Techniques, Data Integrity Protection, Case study on file system viz FAT32, NTFS, Ext2/Ext3 etc.

[T1] [T2][R4][R5] [No. of hrs. 10]

Text Books:

[T1] Deitel & Dietel, “Operating System”, Pearson, 3rd Ed., 2011
[T2] Silbersachatz and Galvin, “Operating System Concepts”, Pearson, 5th Ed., 2001
[T3] Madnick & Donovan, “Operating System”, TMH,1st Ed., 2001

Reference Books:

[R1] Tannenbaum, “Operating Systems”, PHI, 4th Edition, 2000
[R2] Godbole, “Operating Systems”, Tata McGraw Hill, 3rd edition, 2014
[R3] Chauhan, “Principles of Operating Systems”, Oxford Uni. Press, 2014
[R4] Dhamdhere, “Operating Systems”, Tata McGraw Hill, 3rd edition, 2012
[R5] Loomis, “Data Management & File Structure”, PHI, 2nd Ed.

DATA COMMUNICATION & NETWORKS

Paper Code: ETEC-310	**L**	**T/P**	**C**
Paper: Data Communication & Networks	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.
2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 12.5 marks.

Objectives: The objective of the paper is to provide an introduction to the fundamental concepts on data communication and the design, deployment, and management of computer networks.

UNIT- I

Data Communications : Components, protocols and standards, Network and Protocol Architecture, Reference Model ISO-OSI, TCP/IP-Overview ,topology, transmission mode, digital signals, digital to digital encoding, digital data transmission, DTE-DCE interface, interface standards, modems, cable modem, transmission media- guided and unguided, transmission impairment, Performance, wavelength and Shannon capacity. Review of Error Detection and Correction codes.

Switching: Circuit switching (space-division, time division and space-time division), packet switching (virtual circuit and Datagram approach), message switching.

[T1, T2, R1, R4] [No. of Hours: 11]

UNIT- II

Data Link Layer: Design issues, Data Link Control and Protocols: Flow and Error Control, Stop-and-wait ARQ. Sliding window protocol, Go-Back-N ARQ, Selective Repeat ARQ, HDLC, Point-to –Point Access: PPP Point –to-Point Protocol, PPP Stack,

Medium Access Sub layer: Channel allocation problem, Controlled Access, Channelization, multiple access protocols, IEEE standard 802.3 & 802.11 for LANS and WLAN, high-speed LANs, Token ring, Token Bus, FDDI based LAN, Network Devices-repeaters, hubs, switches bridges.

[T1, T2,R1][No. of Hours: 11]

UNIT- III

Network Layer: Design issues, Routing algorithms, Congestion control algorithms,
Host to Host Delivery: Internetworking, addressing and routing, IP addressing (class full & Classless), Subnet, Network Layer Protocols: ARP, IPV4, ICMP, IPV6 ad ICMPV6.

[T1, T2,R1][No. of Hours: 11]

UNIT- IV

Transport Layer: Process to Process Delivery: UDP; TCP, congestion control and Quality of service.

Application Layer: Client Server Model, Socket Interface, Domain Name System (DNS): Electronic Mail (SMTP), file transfer (FTP), HTTP and WWW.

[T2, T1, R1, R4][No. of Hours: 11]

Text Books:

[T1] A. S. Tannenbum, D. Wetherall, “Computer Networks”, Prentice Hall, Pearson, 5th Ed

[T2] Behrouz A. Forouzan, “Data Communications and Networking”, Tata McGraw-Hill, 4th Ed

Reference Books:

[R1] Fred Halsall, “Computer Networks”, Addison – Wesley Pub. Co. 1996.

[R2] Larry L, Peterson and Bruce S. Davie, “Computer Networks: A system Approach”, Elsevier, 4th Ed

[R3] Tomasi, “Introduction To Data Communications & Networking”, Pearson 7th impression 2011

[R4] William Stallings, “Data and Computer Communications”, Prentice Hall, Imprint of Pearson, 9th Ed.

[R5] Zheng , “Network for Computer Scientists & Engineers”, Oxford University Press

[R6] Data Communications and Networking: White, Cengage Learning

WEB ENGINEERING

Paper Code: ETCS-308	**L**	**T/P**	**C**
Paper: Web Engineering	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should

Objective: This paper gives understanding of web designing to the students.

UNIT - I

History of the Internet, Basic internet protocols, World Wide Web (W3C), HTTP: Hypertext Transfer Protocol.
Markup languages-XHTML: Introduction to HTML, basics of XTHML, HTML elements, HTML tags, lists, tables, frames, forms, defining XHTML's abstract syntax, defining HTML documents.
CSS style sheets: Introduction, CSS core syntax, text properties, CSS box model, normal flow box layout, other properties like list, tables, DHTML, XML, XML documents & vocabulary, XML versions & declarations, Introduction to WML.

[T1,T2][No. of hrs. 10]

UNIT – II

Client Side Programming: JAVA Scripts, basic syntax, variables & data-types, literals, functions, objects, arrays, built-in objects, JAVA Script form programming, Intrinsic event handling, modifying element style, document trees,

Server side programming – Java Servlets: Servlet architecture, life cycle, parameter data, sessions, cookies, servlets capabilities, servlets & concurrency. Introduction to JSP, JSP Tags, JSP life cycle, custom tags.

[T1,T2][No. of hrs. 12]

UNIT - III

Security Threats, Security risks of a site, Web attacks and their prevention, Web security model, Session management, authentication, HTTPS and certificates, Application vulnerabilities and defenses.
Client-side security, Cookies security policy, HTTP security extensions, Plugins, extensions, and web apps, Web user tracking.
Server-side security tools, Web Application Firewalls (WAFs) and Fuzzers.

[T1,T2][No. of hrs. 10]

UNIT – IV

Introduction to Web 2.0 and Web 3.0, Concepts and Issues, Latest Trends in Web Technologies. Web Security concerns. Applications of Web Engineering Technologies in distributed systems etc. Case studies using different tools.

[T1,T2][No. of hrs. 12]

Text Books:

[T1] Web Technologies: A Computer Science Perspective, Jackson, Pearson Education India, 2007.
[T2] Web Engineering: A Practitioner's Approach by Roger S Pressman, David Lowe, TMH, 2008.

Reference Books:

[R1] Achyut Godbole,Atul Kahate, "Web Technologies", McGraw-Hill Education, Third Edition.
[R2] Uttam K Roy, "Web Technologies", Oxford University Press, 2012.
[R3] Chris Bates, "Web Programming", Wiley
[R4] Web Engineering by Gertel Keppel, Birgit Proll, Siegfried Reich, Werner R., John Wiley.
[R5] Thinking on the Web: Berner's LEE, Godel and Turing, John Wiley & Sons Inc.

ARTIFICIAL INTELLIGENCE

Paper Code: ETCS-310	**L**	**T/P**	**C**
Paper: Artificial Intelligence	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should

Objective: To learn the basics of designing intelligent agents that can solve general purpose problems, represent and process knowledge, plan and act, reason under uncertainty and can learn from experiences

UNIT-I

Introduction: Introduction to intelligent agents

Problem solving: Problem formulation, uninformed search strategies, heuristics, informed search strategies, constraint satisfaction Solving problems by searching, state space formulation, depth first and breadth first search, iterative deepening

[T1,T2][No. of hrs. 12]

UNIT-II

Logical Reasoning : Logical agents , propositional logic, inferences ,first-order logic, inferences in first order logic, forward chaining, backward chaining, unification , resolution

[T1,T2][No. of hrs. 10]

UNIT-III

Game Playing: Scope of AI -Games, theorem proving, natural language processing, vision and speech processing, robotics, expert systems, AI techniques- search knowledge, abstraction

[T1,T2][No. of hrs. 12]

UNIT-IV

Learning from observations: Inductive learning, learning decision trees, computational learning theory, Explanation based learning

Applications: Environmental Science, Robotics, Aerospace, Medical Sciences etc.

[T1,T2][No. of hrs. 10]

Text Book:

[T1] Rich and Knight, “Artificial Intelligence”, Tata McGraw Hill, 1992

[T2] S. Russel and P. Norvig, “Artificial Intelligence – A Modern Approach”, Second Edition, Pearson Edu.

Reference Books:

[R1] KM Fu, "Neural Networks in Computer Intelligence", McGraw Hill

[R2] Russel and Norvig, "Artificial Intelligence: A modern approach", Pearson Education

MICROPROCESSORS AND MICROCONTROLLERS

Paper Code: ETEE-310	**L**	**T/P**	**C**
Paper: Microprocessors and Microcontrollers	**3**	**1**	**4**

INSTRUCTIONS TO PAPER SETTERS: **MAXIMUM MARKS: 75**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 25 marks.
2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be of 12.5 marks

Objective: The objective of the paper is to facilitate the student with the knowledge of microprocessor systems and microcontroller.

UNIT- I

Introduction to Microprocessor Systems: Architecture and PIN diagram of 8085, Timing Diagram, memory organization, Addressing modes, Interrupts. Assembly Language Programming.

[T1][No. of hrs. 10]

UNIT- II

8086 Microprocessor: 8086 Architecture, difference between 8085 and 8086 architecture, generation of physical address, PIN diagram of 8086, Minimum Mode and Maximum mode, Bus cycle, Memory Organization, Memory Interfacing, Addressing Modes, Assembler Directives, Instruction set of 8086, Assembly Language Programming, Hardware and Software Interrupts.

[T2][No. of hrs. :12]

UNIT- III

Interfacing of 8086 with 8255, 8254/ 8253, 8251, 8259: Introduction, Generation of I/O Ports, Programmable Peripheral Interface (PPI)-Intel 8255, Sample-and-Hold Circuit and Multiplexer, Keyboard and Display Interface, Keyboard and Display Controller (8279), Programmable Interval timers (Intel 8253/8254), USART (8251), PIC (8259), DAC, ADC, LCD, Stepper Motor.

[T1][No. of hrs. :12]

UNIT-IV

Overview of Microcontroller 8051: Introduction to 8051 Micro-controller, Architecture, Memory organization, Special function registers, Port Operation, Memory Interfacing, I/O Interfacing, Programming 8051 resources, interrupts, Programmer's model of 8051, Operand types, Operand addressing, Data transfer instructions, Arithmetic instructions, Logic instructions, Control transfer instructions, Timer & Counter Programming, Interrupt Programming.

[T3][No. of hrs. 11]

Text Books:

[T1] Muhammad Ali Mazidi, "Microprocessors and Microcontrollers", Pearson, 2006

[T2] Douglas V Hall, "Microprocessors and Interfacing, Programming and Hardware" Tata McGraw Hill, 2006.

[T3] Ramesh Gaonkar, "MicroProcessor Architecture, Programming and Applications with the 8085", PHI

References Books:

[R1] Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. MCKinlay "The 8051 Microcontroller and Embedded Systems",2nd Edition, Pearson Education 2008.

[R2] Kenneth J. Ayala, "The 8086 Microprocessor: Programming & Interfacing The PC", Delmar Publishers, 2007.

[R3] A K Ray, K M Bhurchandi, "Advanced Microprocessors and Peripherals", Tata McGraw Hill, 2007.

[R4] Vaneet Singh, Gurmeet Singh, "Microprocessor and Interfacing", Satya Prakashan, 2007.

OPERATING SYSTEMS (LINUX PROGRAMMING AND ADMINISTRATION) LAB

Paper Code: ETCS-352	**L**	**T/P**	**C**
Paper: Operating Systems (Linux Programming and Administration) Lab	**0**	**2**	**1**

List of Experiments:

1. Write a program to implement CPU scheduling for first come first serve.
2. Write a program to implement CPU scheduling for shortest job first.
3. Write a program to perform priority scheduling.
4. Write a program to implement CPU scheduling for Round Robin.
5. Write a program for page replacement policy using a) LRU b) FIFO c) Optimal.
6. Write a program to implement first fit, best fit and worst fit algorithm for memory management.
7. Write a program to implement reader/writer problem using semaphore.
8. Write a program to implement Banker's algorithm for deadlock avoidance.

NOTE:- At least 8 Experiments out of the list must be done in the semester.

DATA COMMUNICATION & NETWORKS LAB

Paper Code: ETEC-358	**L**	**T/P**	**C**
Paper: Data Communication & Networks Lab	**0**	**2**	**1**

List of Experiments:

1. PC to PC Communication
2. Parallel Communication using 8 bit parallel cable & Serial communication using RS 232C
3. Ethernet LAN protocol
4. To create scenario and study the performance of CSMA/CD protocol through Simulation
5. To create scenario and study the performance of token bus and token ring protocols through simulation
6. To create scenario and study the performance of network with CSMA / CA protocol and compare with
7. CSMA/CD protocols.
8. Implementation and study of stop and wait protocol
9. Implementation and study of Go back-N and selective repeat protocols
10. Implementation of distance vector routing algorithm
11. Implementation of Link state routing algorithm.

***All Practical can be conducted using C-Language and LAN Emulator.**

NOTE:- At least 8 Experiments out of the list must be done in the semester.

WEB ENGINEERING LAB

Paper Code: ETCS-356	**L**	**T/P**	**C**
Paper: Web Engineering Lab	**0**	**2**	**1**

Web Engineering Lab experiment based on syllabus of (ETCS-308).

NOTE:- At least 8 Experiments from the syllabus must be done in the semester.

MICROPROCESSORS AND MICROCONTROLLERS LAB

	L	T/P	C
Paper Code: ETEE-358			
Paper: Microprocessors and Microcontrollers Lab	**0**	**2**	**1**

List of Experiments:

1. Write a program to add and subtract two 16-bit numbers with/ without carry using 8086.
2. Write a program to multiply two 8 bit numbers by repetitive addition method using 8086.
3. Write a Program to generate Fibonacci series.
4. Write a Program to generate Factorial of a number.
5. Write a Program to read 16 bit Data from a port and display the same in another port.
6. Write a Program to generate a square wave using 8254.
7. Write a Program to generate a square wave of 10 kHz using Timer 1 in mode 1(using 8051).
8. Write a Program to transfer data from external ROM to internal (using 8051).
9. Design a Minor project using 8086 Micro processor (Ex: Traffic light controller/temperature controller etc)
10. Design a Minor project using 8051 Micro controller

NOTE: - At least 8 Experiments out of the list must be done in the semester.