**CSE 3203 CT 4 Assignment**

**Roll No: 1903036**

**Assignment Problem:**

**Build CPU based on following requirements:**

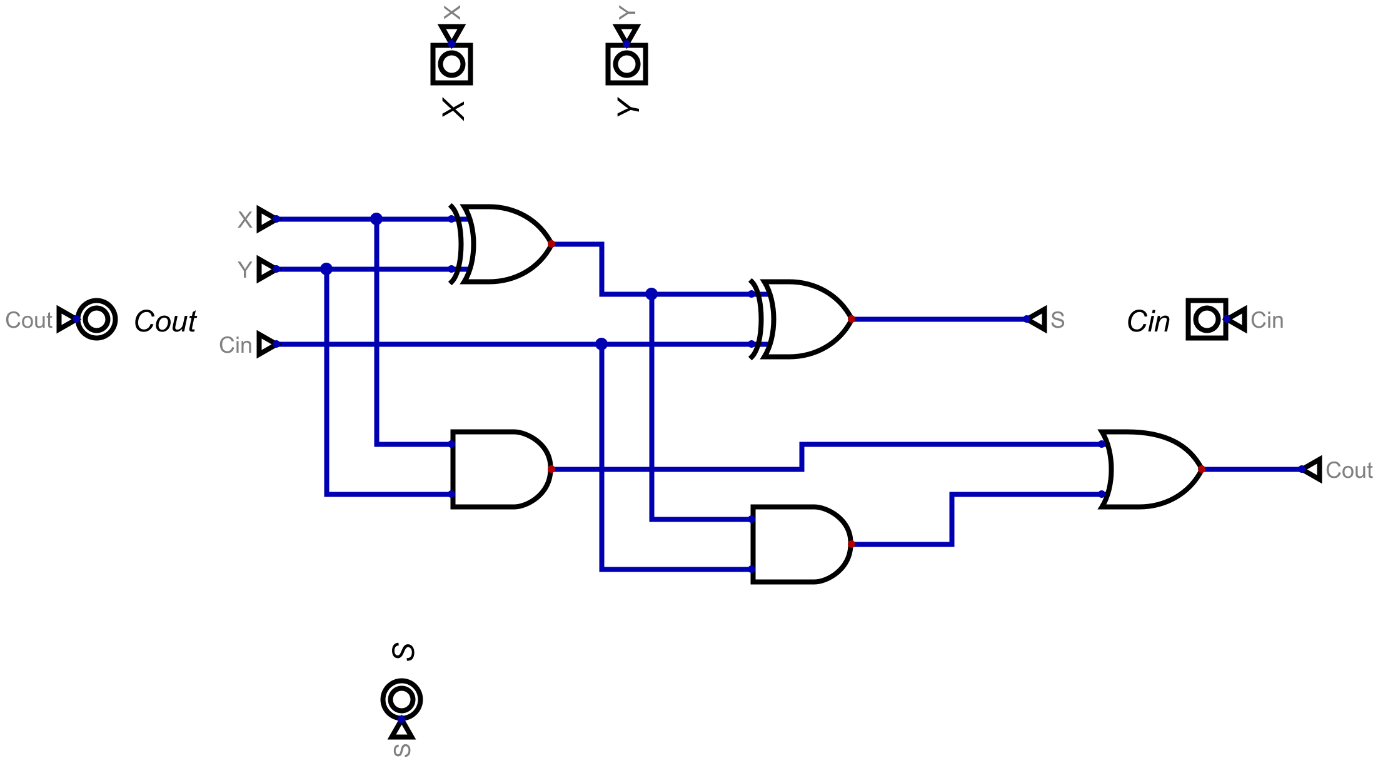
1. **Word Size of CPU = 5**
2. **ALU Operations = XOR, ADD, SHR**
3. **Register Number = 3**
4. **Size of RAM = 9**
5. **Word size of ISA and RAM = 18**
6. **CPU Instructions = Register Mode, Immediate Mode, JMP, JGE**

**Solution:**

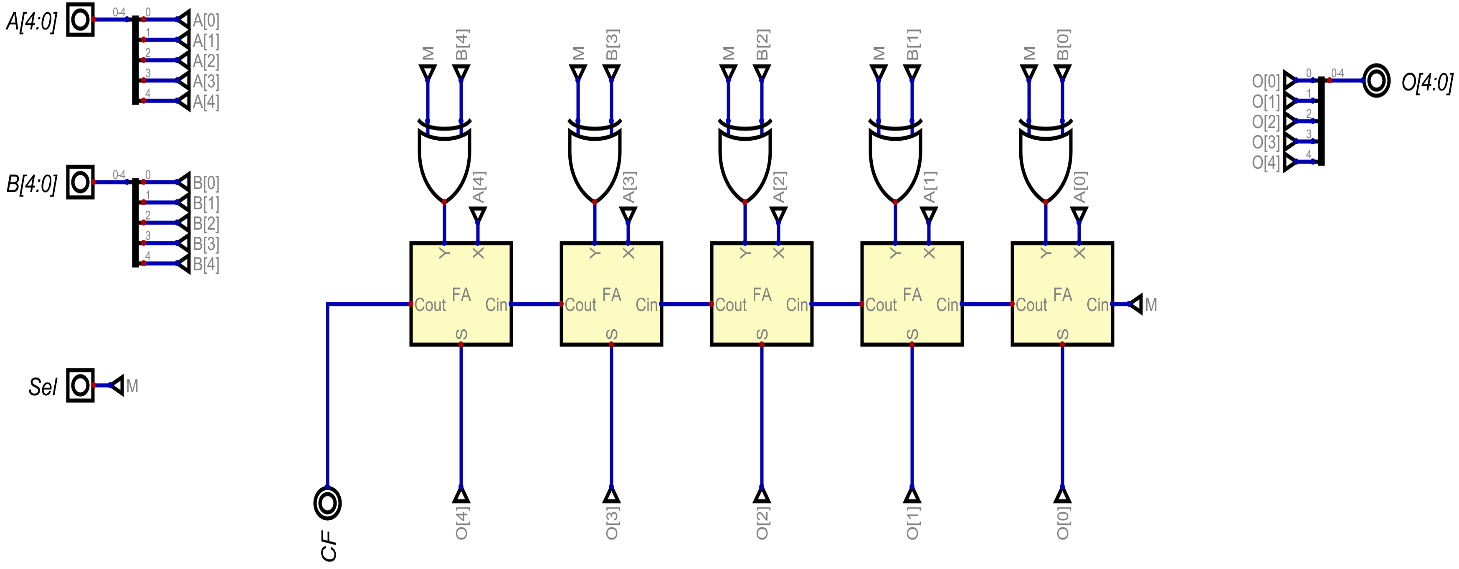
**Simulator Design:**

1. **ALU Circuit (Top to Bottom all circuits):**

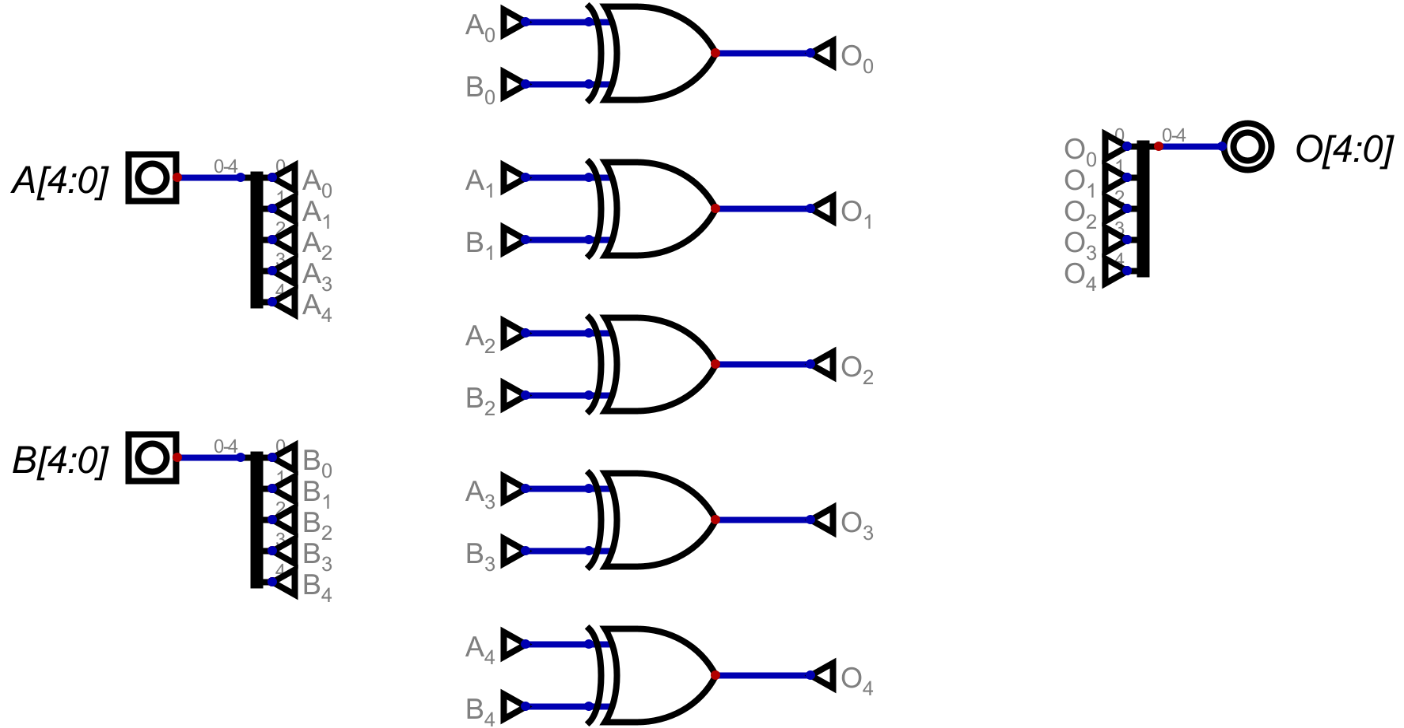
**1 bit Full Adder:**

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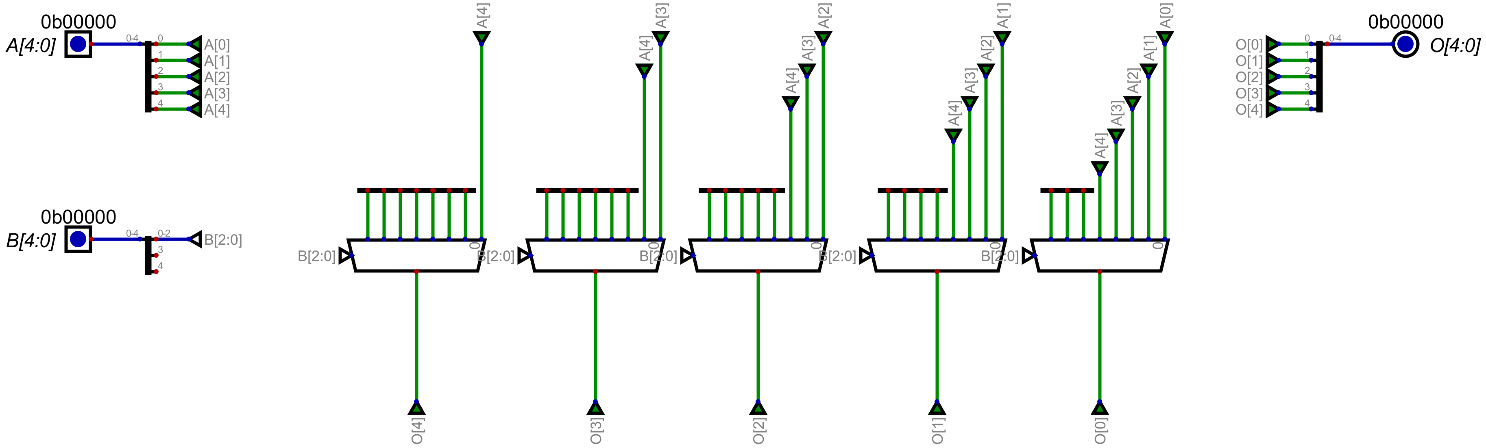
**5 bit Adder & Subtractor:**

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**5 bit XOR:**

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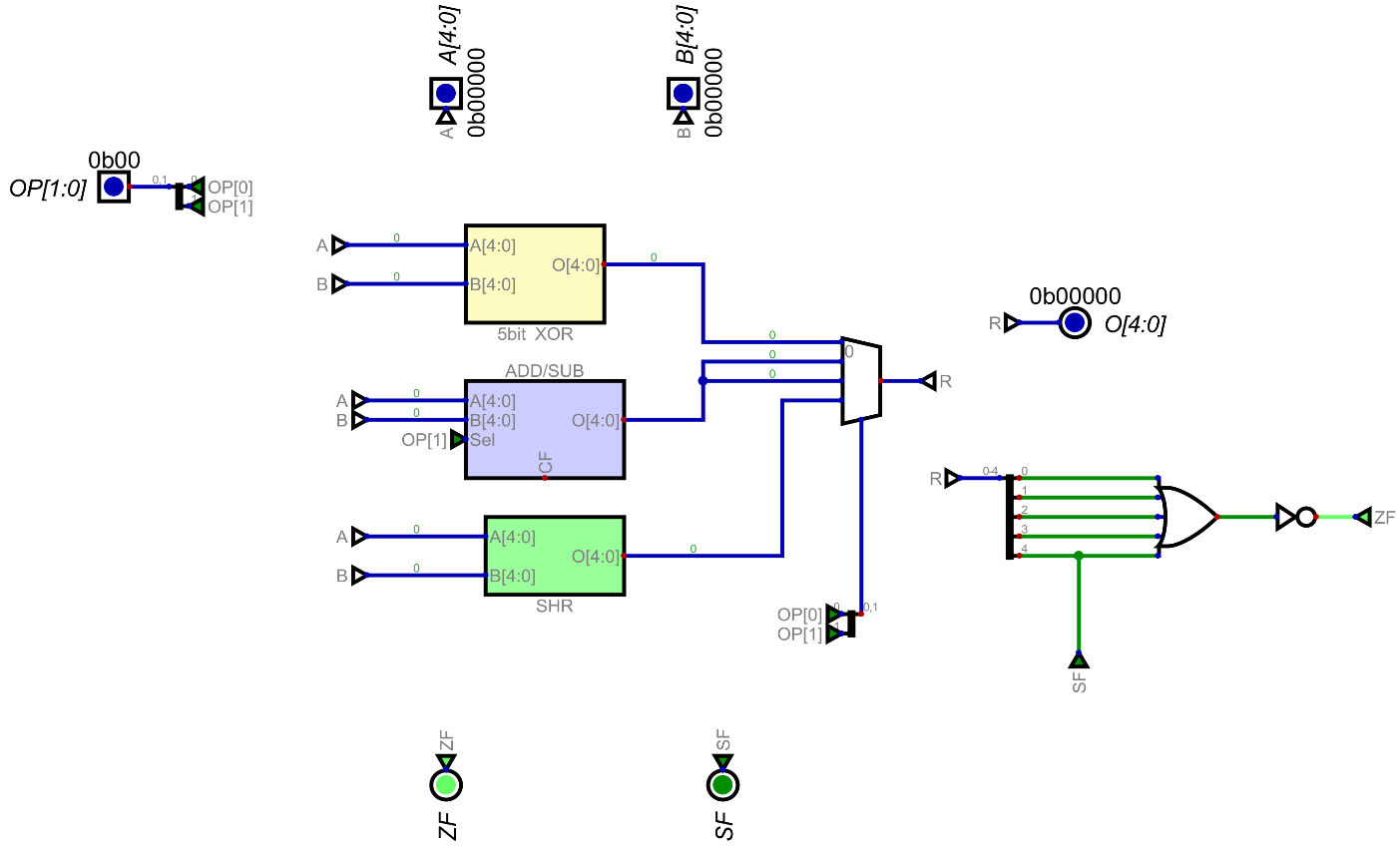
**5 bit Shift Right(SHR):**

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**5 bit ALU:**

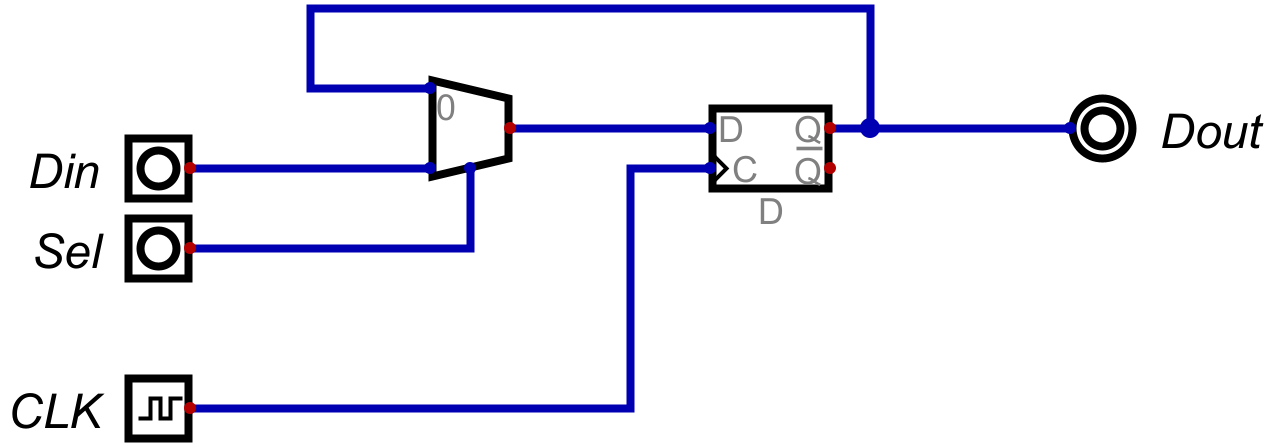
**ALU Operations:**

|  |  |  |
| --- | --- | --- |
| Opcode [1:0] | | operation |
| 0 | 0 | XOR |
| 0 | 1 | ADD |
| 1 | 0 | CMP |
| 1 | 1 | SHR |

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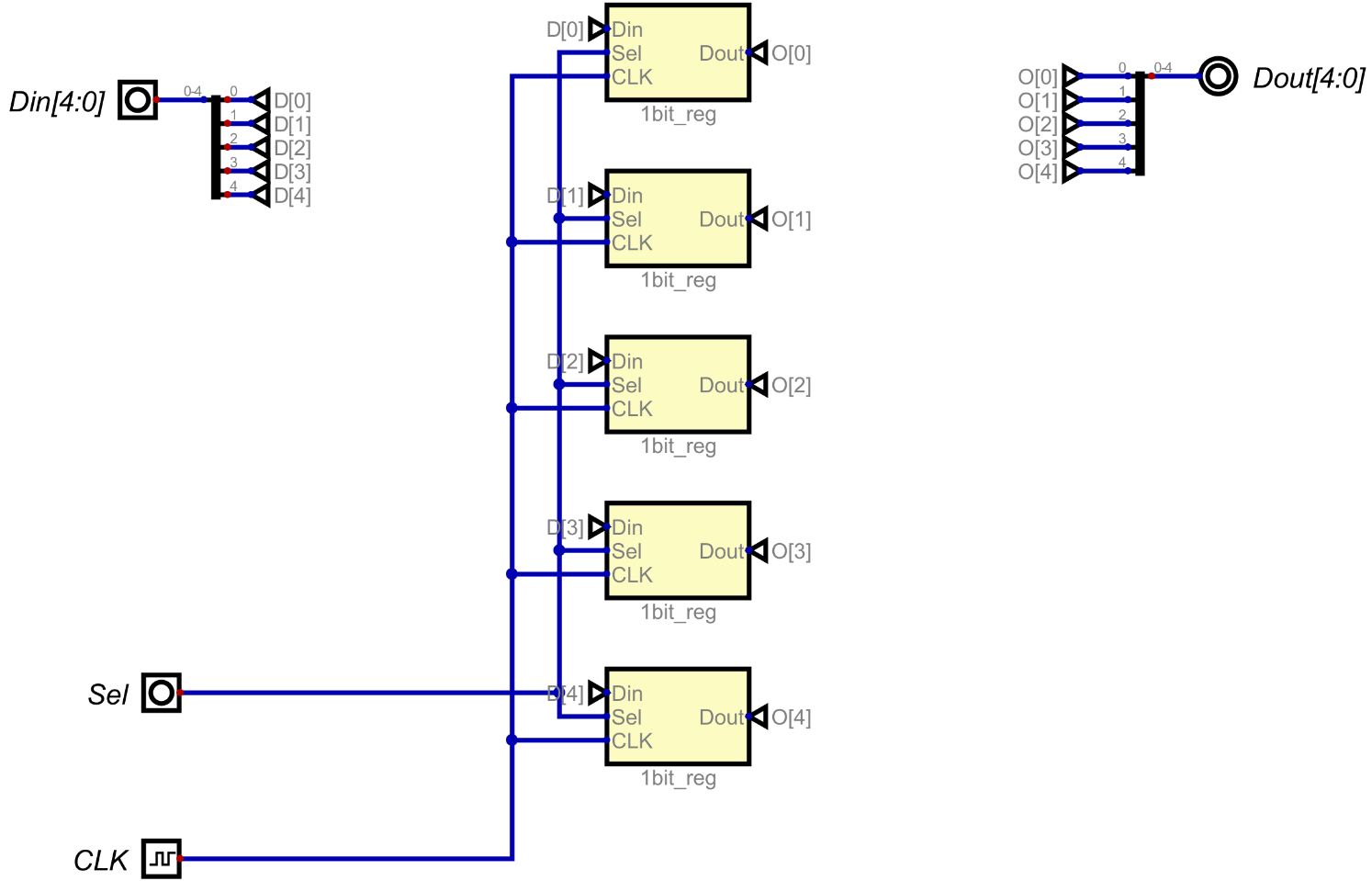
1. **Register Set Circuit (Top to Bottom all circuits):**

**1 bit register:**

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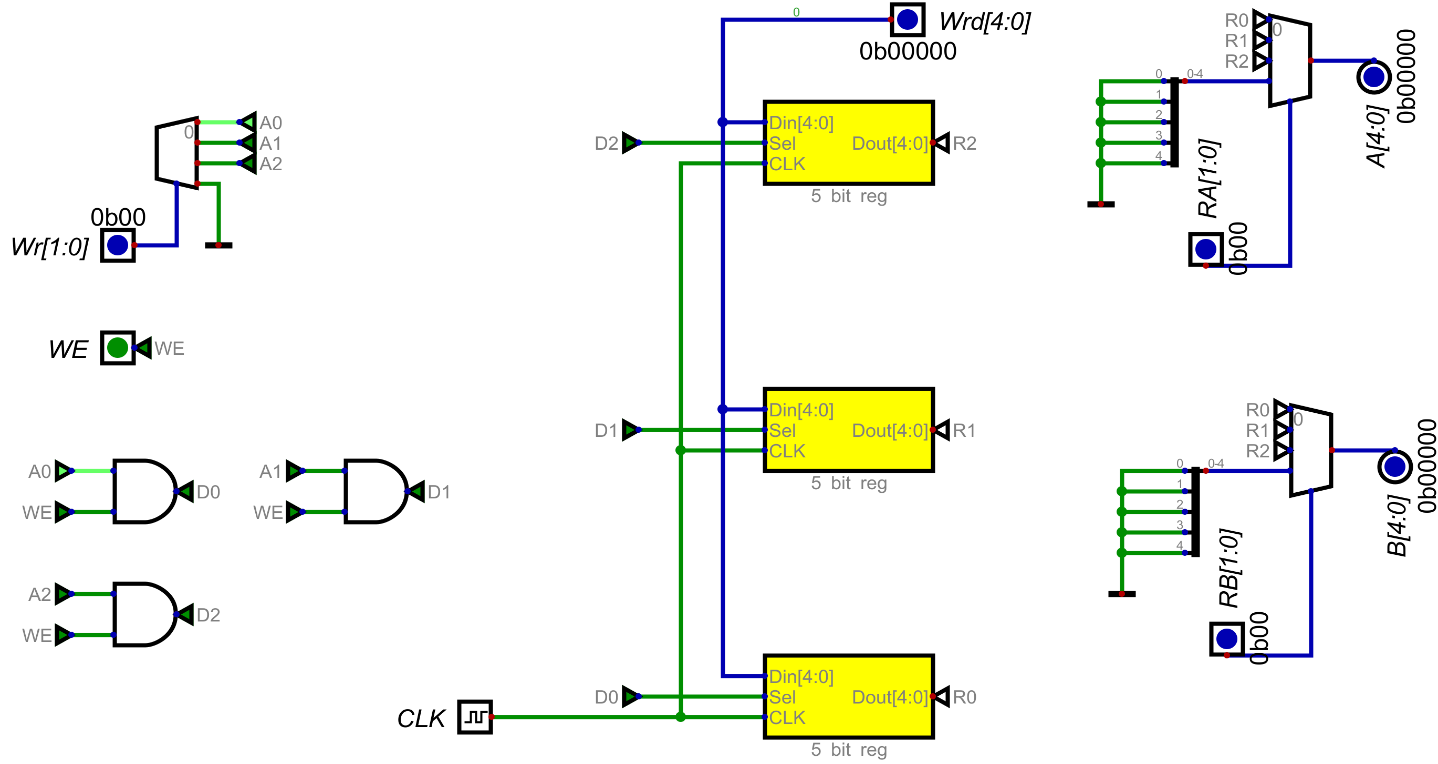
**5 bit register:**

Using 5, 1bit registers:



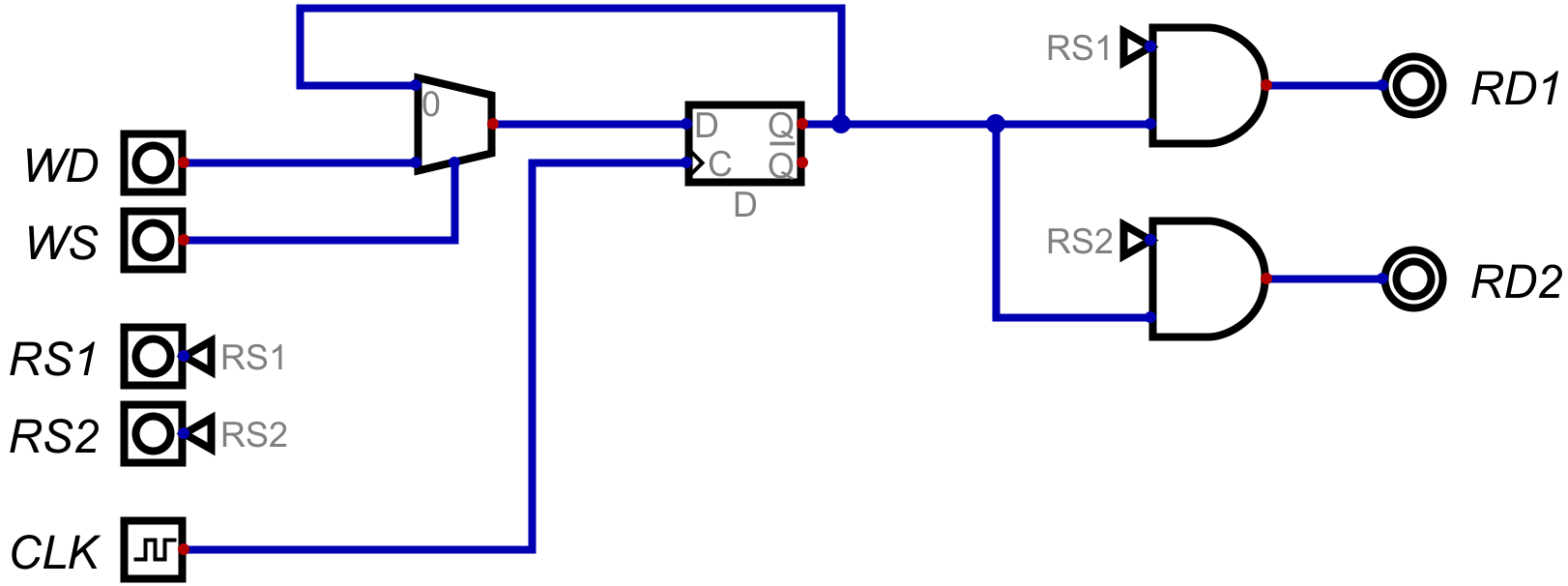
**5 bit register set with 3 register:**

Final register set design:

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1. **RAM Circuit (Top to Bottom all circuits):**

**1x1 SRAM:**

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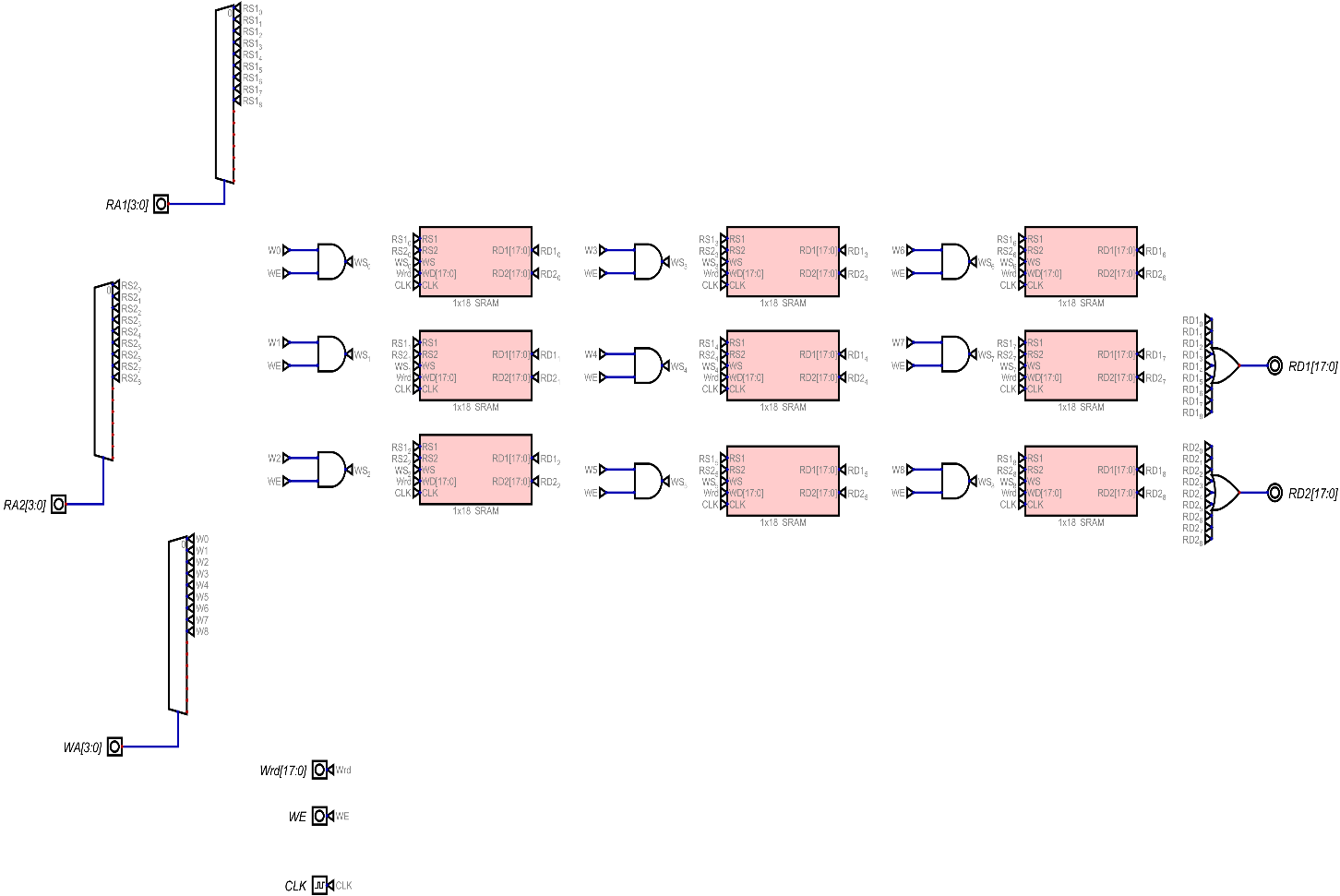
**1x18 SRAM:**

According to ISA and SRAM word size:



**9x18 SRAM:**

According to SRAM size:



1. **ISA:**

**Mode operation:**

|  |  |  |
| --- | --- | --- |
| Opcode [3:2] | | Mode |
| 0 | 0 | Register Mode |
| 0 | 1 | Immediate Mode |
| 1 | 0 | Branching Mode |

**Register Mode:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Opcode (4 bit)** | | **Register 1** | **Register 2** | **Unused** |
| 2 bits | 2 bits | 2 bits | 2 bits | 10 bits |
| Type of instruction  (00) | Selection of ALU operation  (00-11) | RA  (00-10) | RB  (00-10) | x |

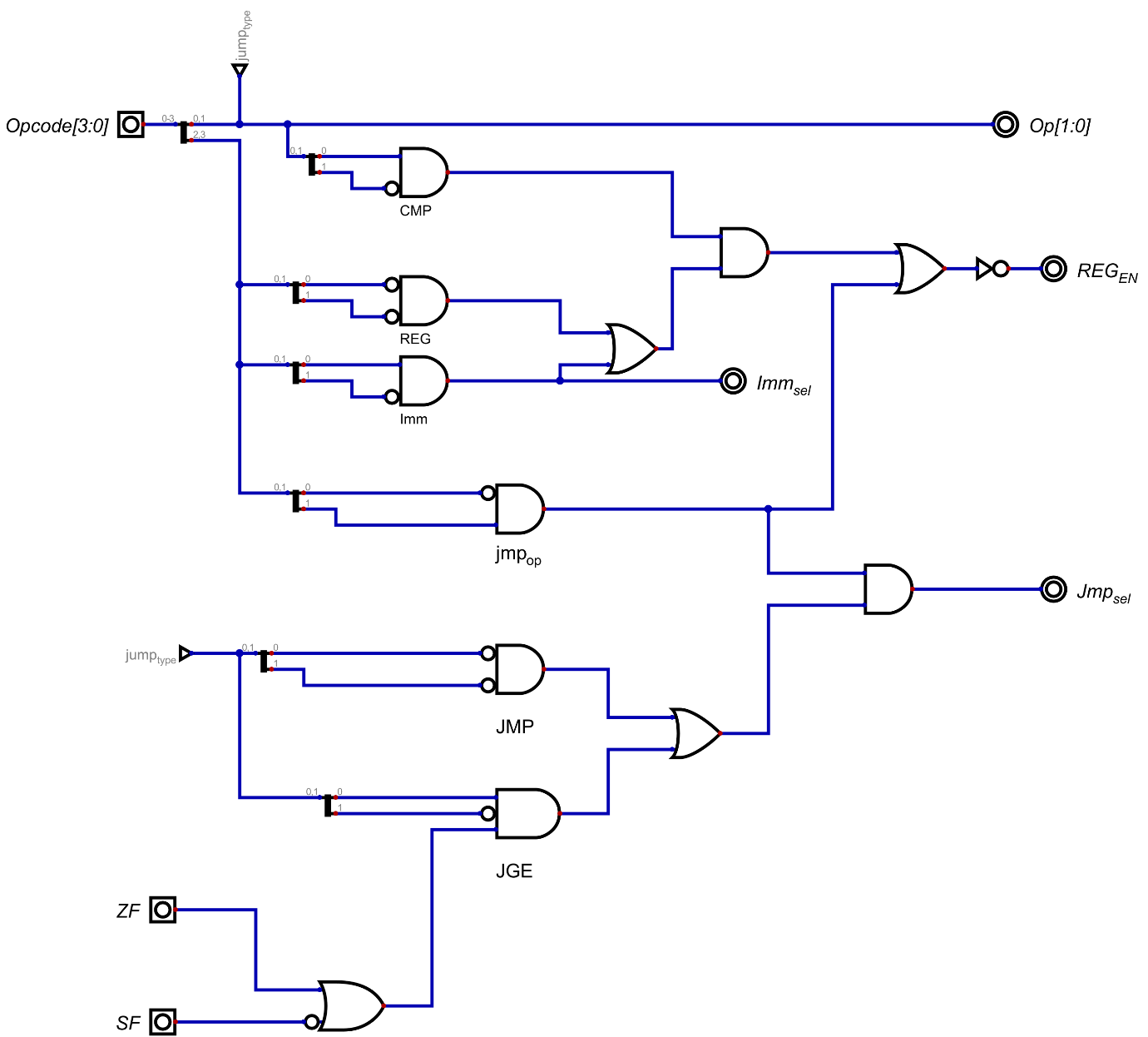
**Immediate Mode:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Opcode (4 bit)** | | **Register 1** | **Value** | **Unused** |
| 2 bits | 2 bits | 2 bits | 5 bits | 7 bits |
| Type of instruction  (01) | Selection of ALU operation  (00-11) | RA  (00-10) | value  (00000-11111) | x |

**Branching Mode:**

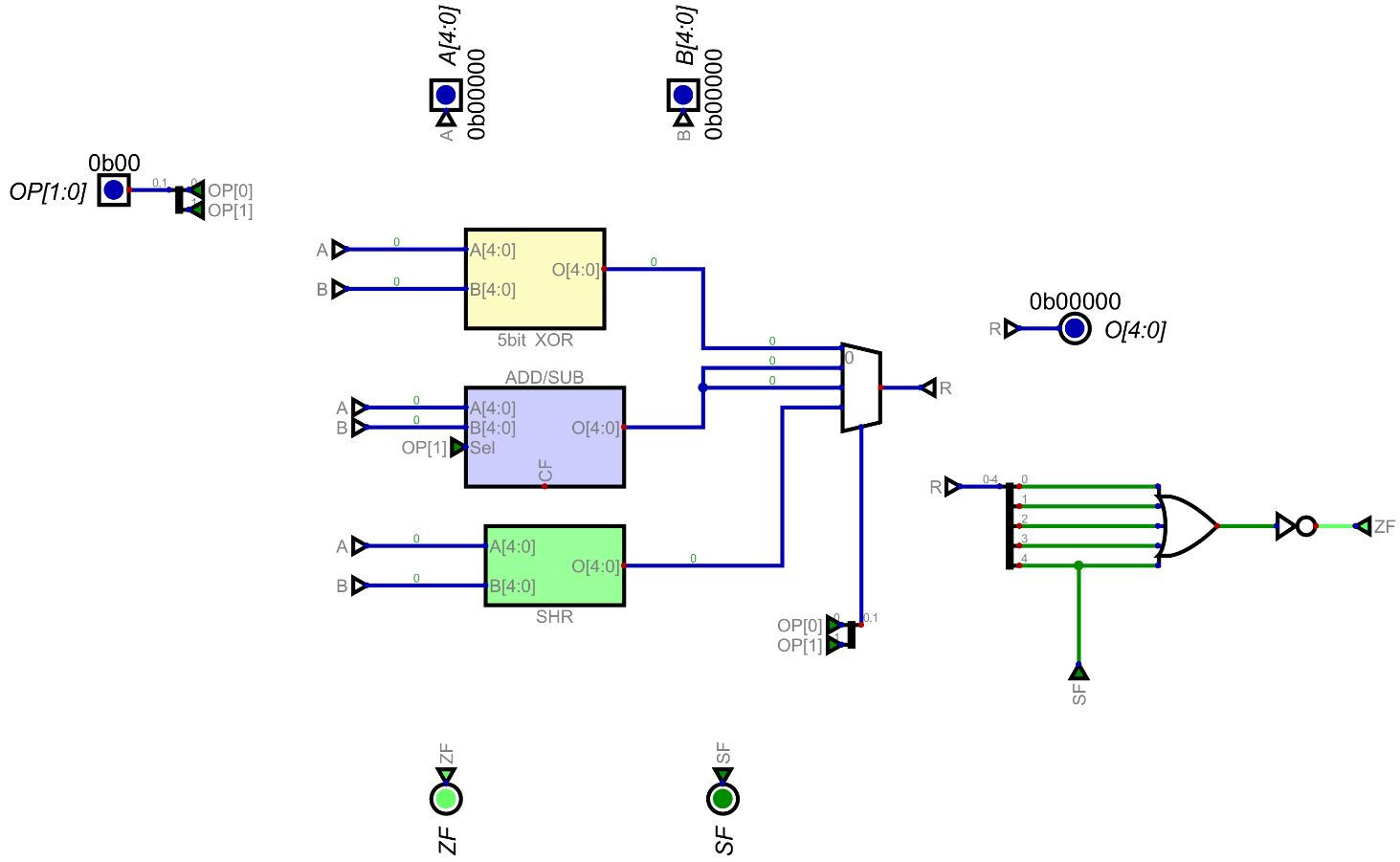
|  |  |  |  |
| --- | --- | --- | --- |
| **Opcode (4 bit)** | | **Jump Address** | **Unused** |
| 2 bits | 2 bits | 4 bits | 10 bits |
| Type of instruction  (10) | Selection of Jump Operation  (00-01) | Address  (0000-1111) | x |

**Control Unit:**

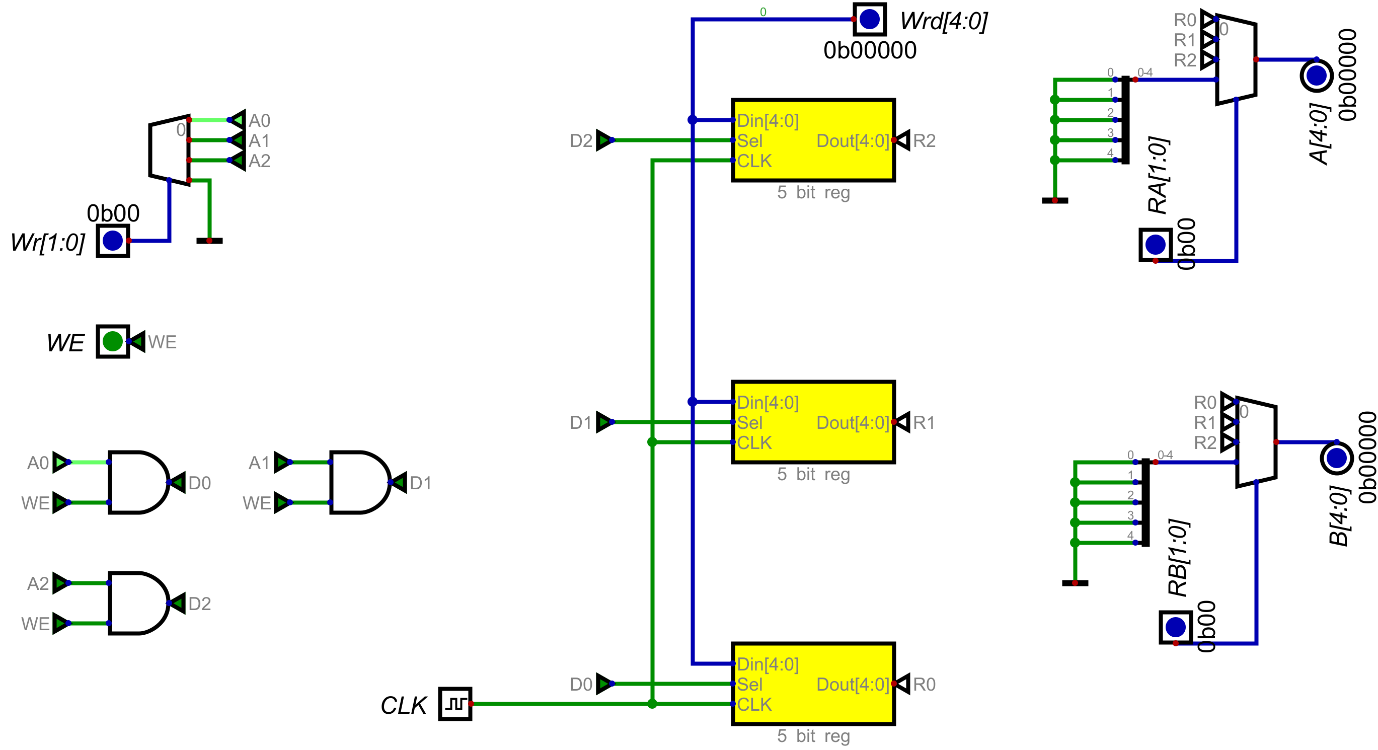
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1. **CPU (Top to Bottom all circuits):**

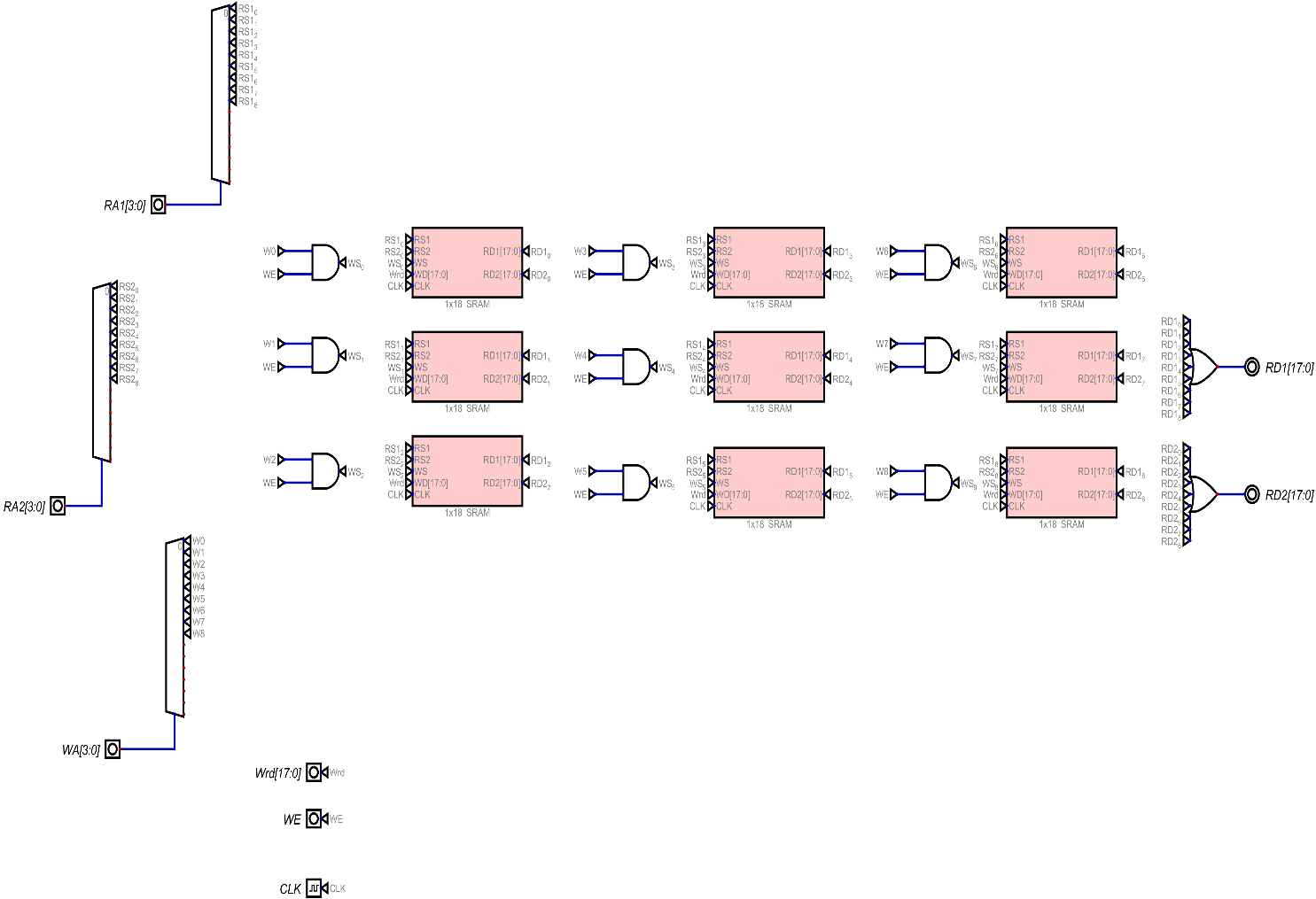
**5 bit ALU:**

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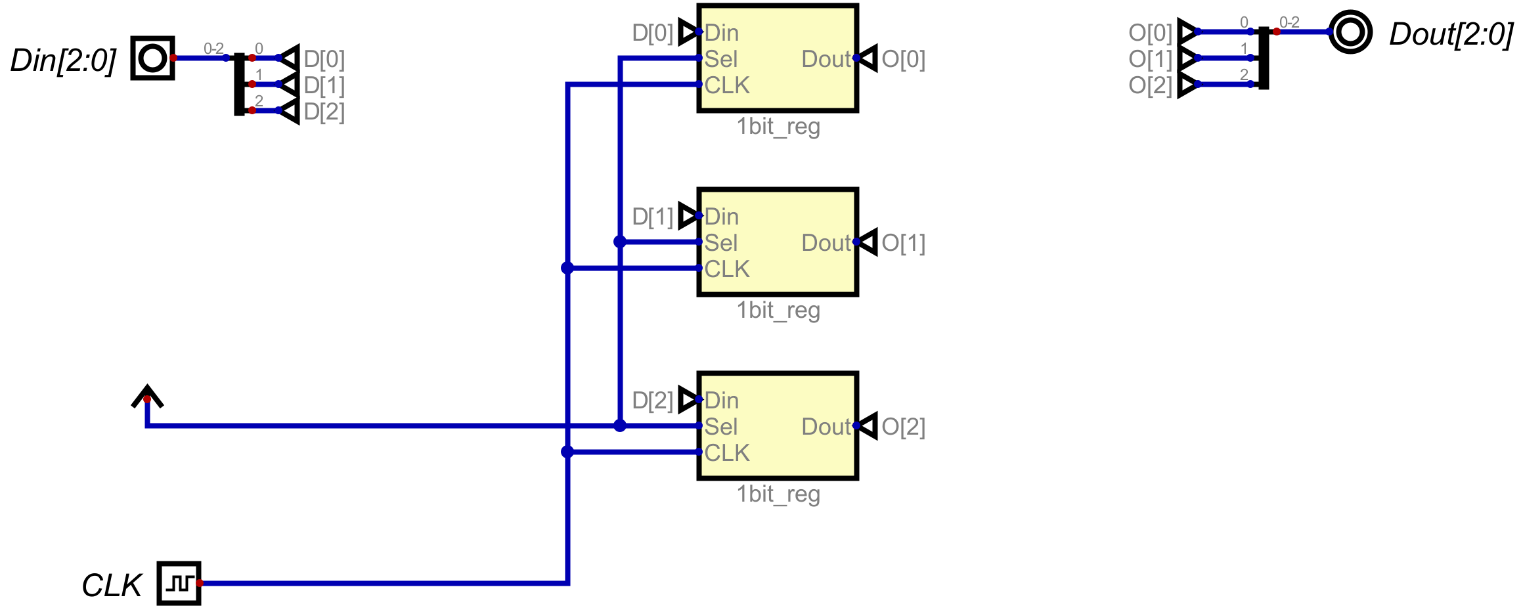
**5 bit Reg Set:**

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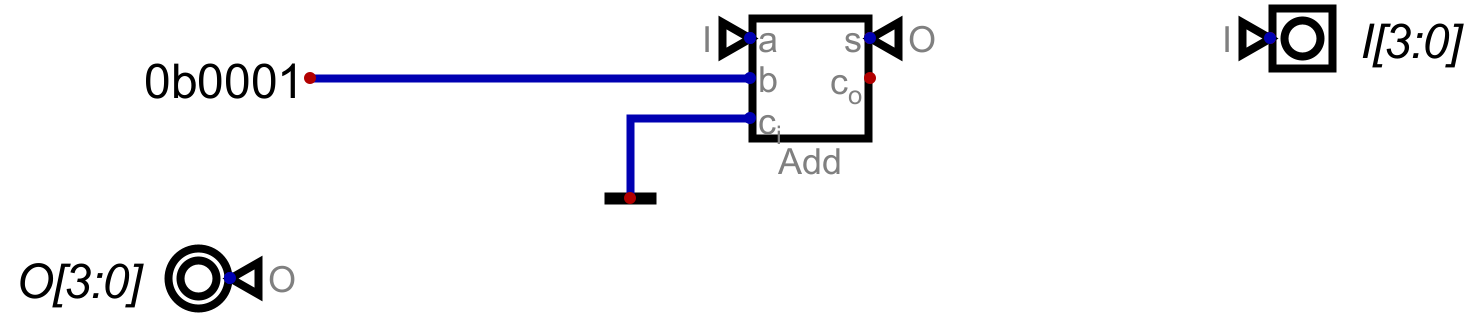
**9x18 SRAM:**



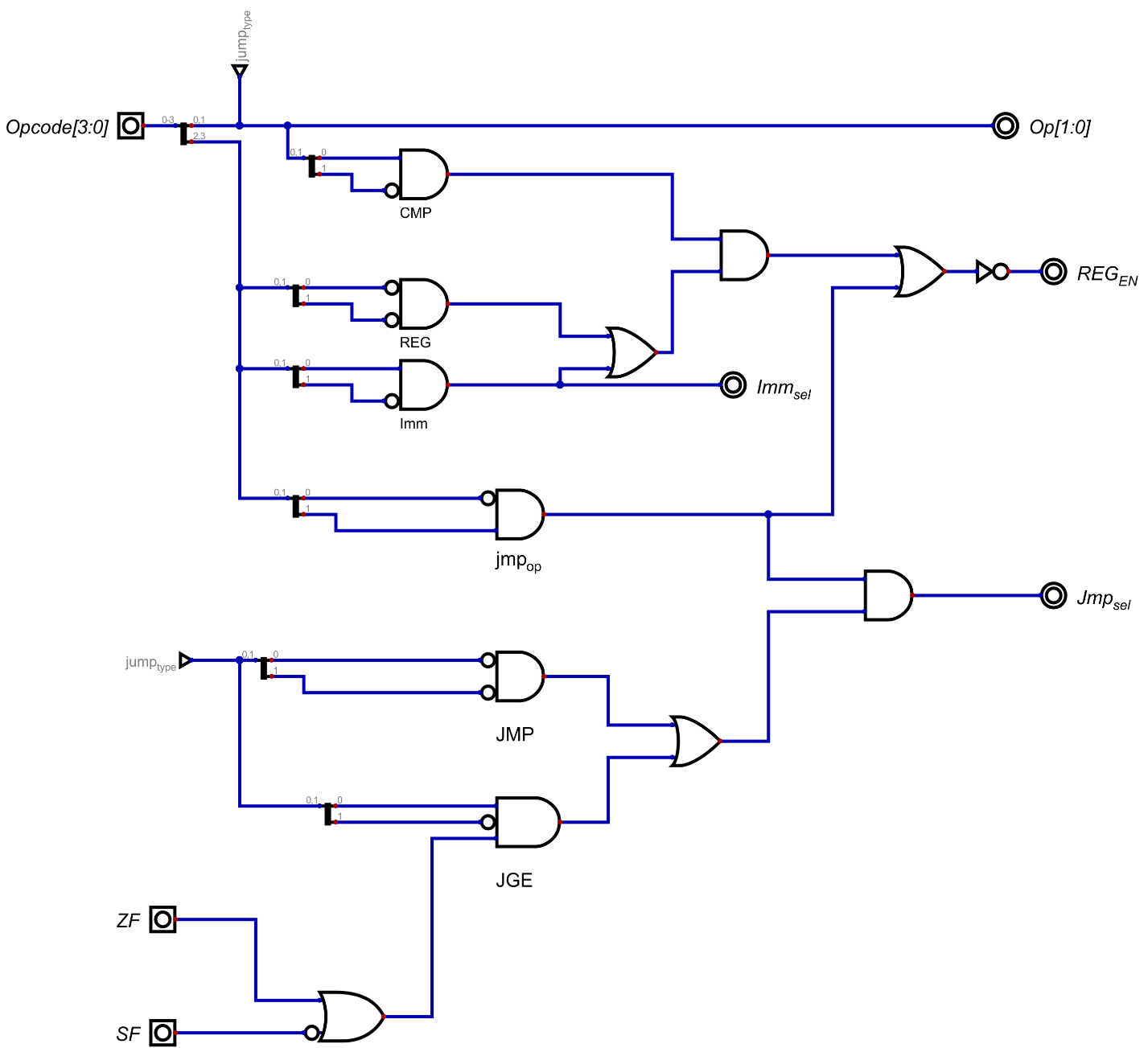
**4 bit program Counter :**

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**4 bit PC Adder:**

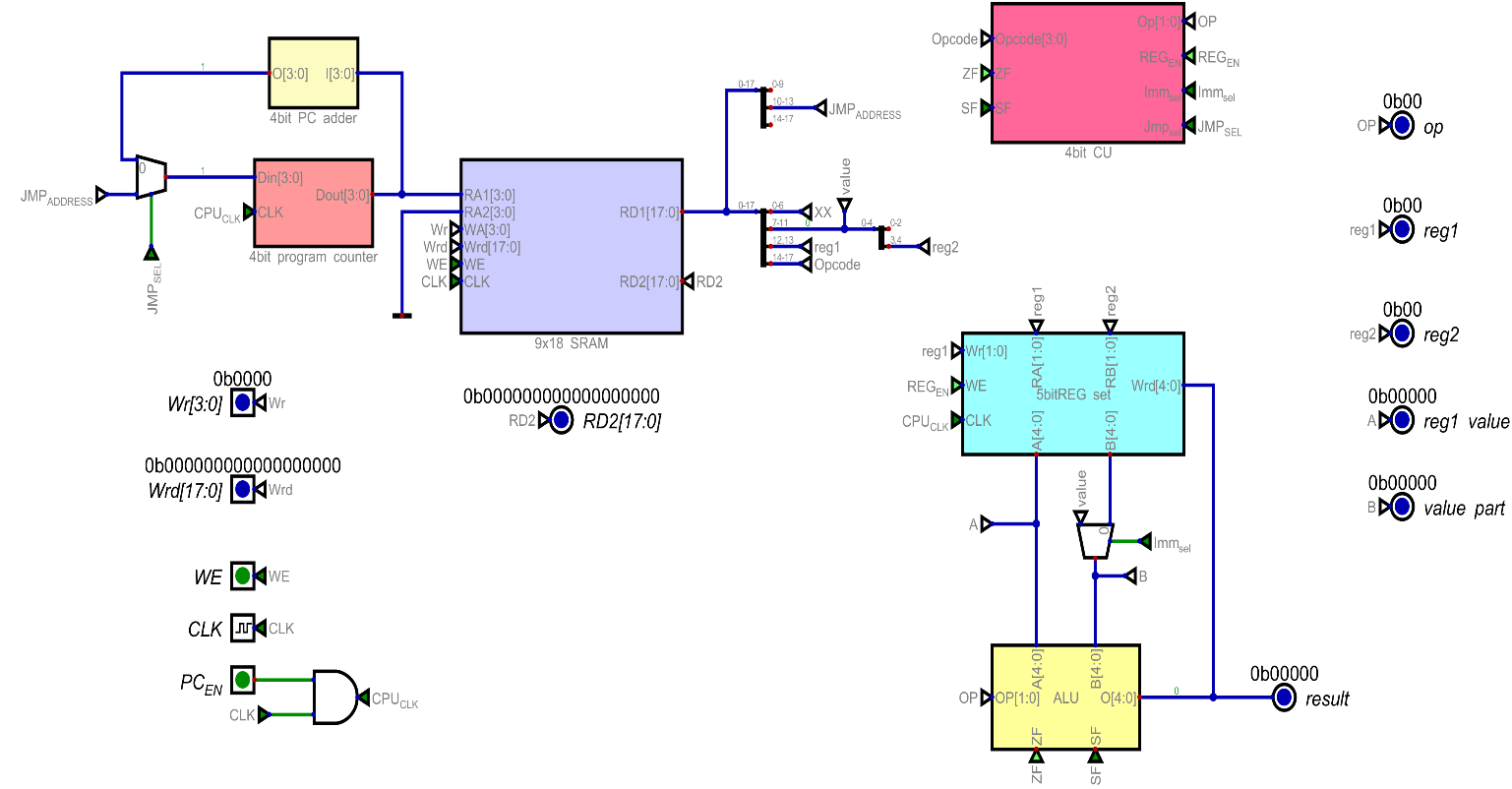
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**Control Unit:**

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**5 bit CPU:**

Final design:

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