# Utilize your CPU power

### Cache optimizations and SIMD instructions

Mario Mulansky

ISC-CNR, Institute for Complex Systems, Florence, Italy



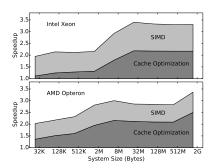


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### Performance

#### **Numerical Simulations:**

- Flops Flops
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#### This talk:

- Bandwidth bottleneck
- Example: Numerical algorithm (ODE solver)
- ullet Bandwidth bound o Flops bound
- More speed: Boost.SIMD

## Data bandwidth and latency limitation

Modern CPUs:  $\sim$  3 GHz, 1 Op/cycle  $\rightarrow$  3 GFlops/s

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Example  $\mathbf{x} = \mathbf{a} + \mathbf{b}$ : 24 Bytes/Operation

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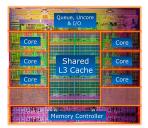
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#### Cache

Intel® Core™ i7-3960X Processor Die Detail

### Intel Sandy Bridge

Cache	Size	GB/s	Cycles	
L1	32K	350	4	
L2	256K	250	12	
L3	3-6M	100	12-30	
RAM	4-32G	16	20-100	



0

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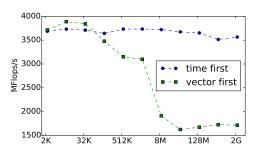
#### Two approaches:

- time first:  $r_1(t) \rightarrow r_1(t + \Delta t) \rightarrow r_1(t + 2\Delta t) \dots$ , then  $r_2 \dots$
- vector first:  $\mathbf{r}(t) \rightarrow \mathbf{r}(t + \Delta t) \rightarrow \mathbf{r}(t + 2\Delta t) \dots$

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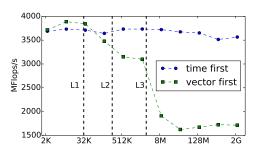
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$$\dot{r}_{i} = f_{i}(\mathbf{r}, t)$$

$$= \underbrace{h_{i}(r_{i}, t)}_{\text{local}} + \underbrace{g_{i}(r_{i}, r_{i-1}, r_{i+1}, t)}_{\text{n. n. coupling}}$$

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Time discretization  $\mathbf{r}_t$  with  $\Delta t$ .

R-K algorithms: 
$$\mathbf{r}_t \to \mathbf{r}_{t+\Delta t}$$
 with  $s$  stages  $j=1\dots s$ .

at each stage:

$$\mathbf{k}^{j} = \mathbf{f}(\mathbf{r}', t')$$
  
$$\mathbf{r}' = \mathbf{r}_{t} + \sum_{n < j} a_{j,n} \mathbf{k}^{n} \Delta t$$

$$\dot{r}_i = f_i(\mathbf{r}, t)$$

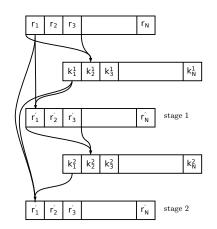
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r <sub>1</sub>	r <sub>2</sub>	r <sub>3</sub>	$r_N$	stage s

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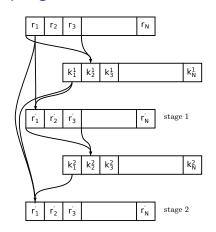
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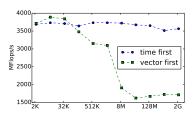
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Problem: Coupling prevents "time first" approach

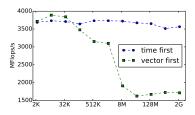




Coupling: only "vector first"?

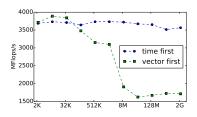


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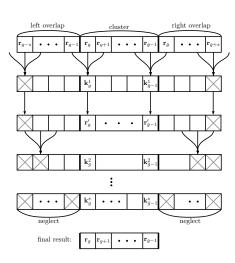


Clustering!

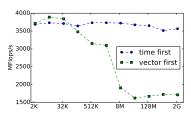
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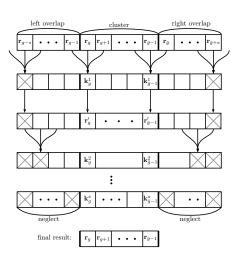
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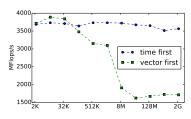
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s iterations for each cluster at once ightarrow better cache usage

Price: additional overlap computations



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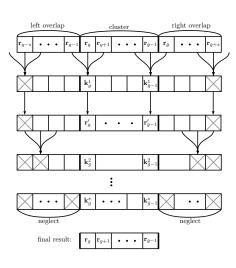


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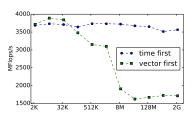
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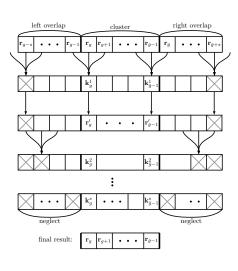


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Optimal granularity?  $\sim$  Cache size... Measure!

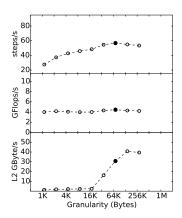


Coupled Rössler systems,  $N=2^{20}\approx 10^6$  (24 MB)

Intel Xeon E5-2690 @ 3.8GHz, Intel Compiler 15.0.0

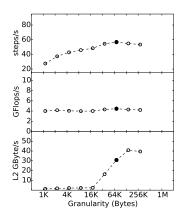
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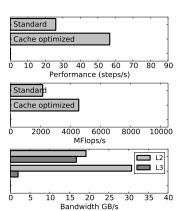
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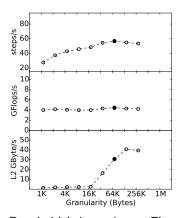
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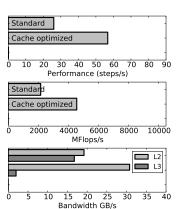




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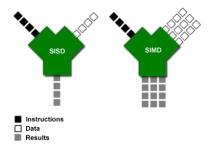




Bandwidth bound → Flops/s bound

# Increase Flops/s: SIMD instructions

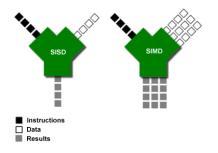
SIMD: Single Instruction Multiple Data



Additional registers and instructions in modern CPUs

## Increase Flops/s: SIMD instructions

SIMD: Single Instruction Multiple Data



Additional registers and instructions in modern CPUs Compilers try to use those automatically Often, explicit SIMD code improve Flops/s significantly Only helpful, if algorithm is Flops bound!

#### Boost.SIMD

### (not yet official Boost library)

- Abstraction of SIMD instructions: (SSE3, SSE4.1, SSE4.2, AVX, FMA4, AltiVec, Intel MIC).
- Fundamental ingredient: SIMD registers  $\rightarrow$  SIMD pack.
- Expression template for optimization possibilities.
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### simd::pack<T>

- pack<T,N> SIMD register with N elements of T.
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- N must be power of 2.
- Operations available +,-,\*,/
- Math functions available: pow,abs,sqrt,log10,...

## Quick Example: vector addition $\mathbf{x} = \alpha \cdot \mathbf{a} + \mathbf{b}$

```
typedef vector < double > vec;

double alpha;
vec x(N), a(N), b(N);

for (int n=0; n < x. size(); ++n)
    x[n] = alpha * a[n] + b[n];</pre>
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```
typedef simd::pack<double> pack; // automatic size
typedef vector<pack, simd::allocator<pack> > vec;
static const size_t pack_size = pack::static_size;
static const int M = N/pack_size;

double alpha;
vec x(M), a(M), b(M);

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## Algorithm does not change

```
for(int n=0; n<x.size(); ++n)
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#### even more clear:

```
transform(a, b, x, [alpha](double a_n, double b_n)
{return alpha * a_n + b_n;}
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With Boost.SIMD: change typdefs, don't touch algorithm.

### SIMD for ODE Simulation

ODE iteration  $\mathbf{r}_t \to \mathbf{r}_{t+\Delta t}$ : some sort of transform

Abstraction Boost.odeint provides:

- generic algorithms
- container independent implementation
- exchangeable backends

```
typedef vector<double> state_type;
state_type x(N);
odeint::runge_kutta4<state_type> rk4;
odeint::integrate_const(rk4, roessler, x, 0.0, T, dt);
```

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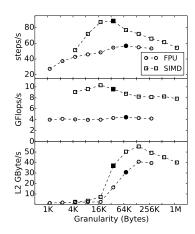
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### SIMD Performance Results

 ${\sf Boost.odeint} + {\sf Boost.SIMD}$ 

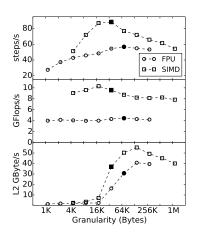
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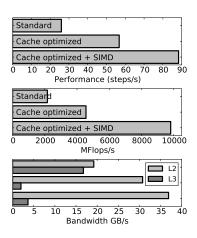
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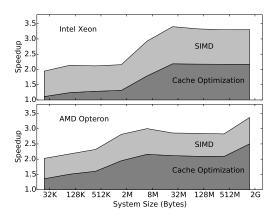
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# Size Dependence



### Summary + Conclusions

- Granularity  $\rightarrow$  data transfer  $\searrow$ , BW bound  $\rightarrow$  Flops/s bound.
- Increase Op/cycle via SIMD  $\rightarrow$  total performance gain 3x.
- Known for stencil computations: space- and time-blocking.

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#### Take-home-message:

- Data size > L2 cache size → introduce granularity.
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- Source code: https://github.com/mariomulansky/olsos
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www.odeint.com