

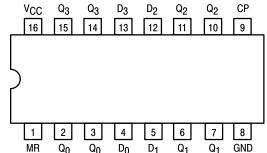
QUAD D FLIP-FLOP

The LSTTL/MSI SN54/74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

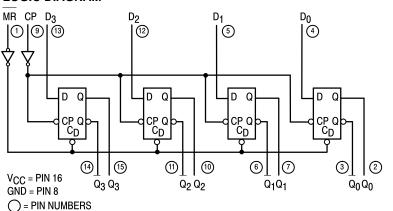
PIN NAMES

		HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5 (2.5) U.L.
Q_0-Q_3	Complemented Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

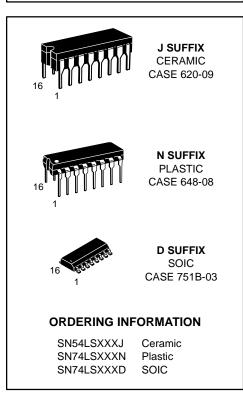
- a. 1 TTL Unit Load (U.L.) = $40 \mu A HIGH/1.6 mA LOW$.
- b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

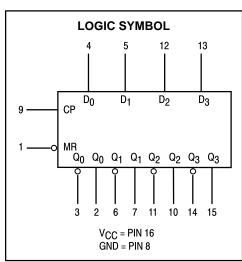
LOGIC DIAGRAM



SN54/74LS175

QUAD D FLIP-FLOP LOW POWER SCHOTTKY





SN54/74LS175

FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and Q outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and Q outputs to follow. A

LOW input on the Master Reset (MR) will force all Q outputs LOW and Q outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, MR = H)	Outputs (t = n+1) Note 1		
D	Q	Q	
L	L	Н	
Н	Н	L	

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
ЮН	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits					
Symbol	Parameter		Min	Тур	Max	Unit	Tes	et Conditions
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Inpu All Inputs	t HIGH Voltage for
\/	January CVV Voltage				0.7	V	Guaranteed Input LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8	V	All Inputs	
VIK	Input Clamp Diode Voltage			-0.65	-1.5	٧	V _{CC} = MIN, I _{IN} = -18 mA	
Maria	Output HICH Make as	54	2.5	3.5		V	V _{CC} = MIN, I _{OH}	= MAX, V _{IN} = V _{IH}
VOH	Output HIGH Voltage	74	2.7	3.5		V	or V _{IL} per Truth	Table Table
V	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$ $V_{IN} = V_{IL} \text{ or } V_{IH}$
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	per Truth Table
1					20	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V	
і ін	Input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
IIL	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
los	Short Circuit Current (Note	1)	-20		-100	mA	V _{CC} = MAX	
lcc	Power Supply Current				18	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS175

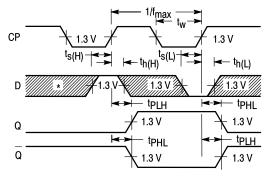
AC CHARACTERISTICS (T_A = 25°C)

		Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
fMAX	Maximum Input Clock Frequency	30	40		MHz	
^t PLH ^t PHL	Propagation Delay, MR to Output		20 20	30 30	ns	V _{CC} = 5.0 V C _L = 15 pF
^t PLH ^t PHL	Propagation Delay, Clock to Output		13 16	25 25	ns	- '

AC SETUP REQUIREMENTS (TA = 25°C)

		Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions	
t₩	Clock or MR Pulse Width	20			ns		
t _S	Data Setup Time	20			ns	V _{CC} = 5.0 V	
th	Data Hold Time	5.0			ns		
t _{rec}	Recovery Time	25			ns		

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

CP Q tpLH 1.3 V 1.3 V 1.3 V 1.3 V 1.3 V 1.3 V 1.3 V

Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

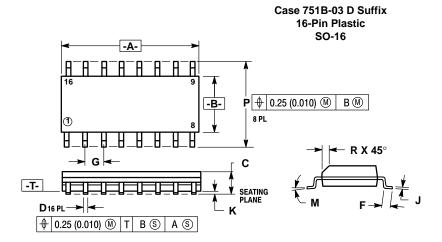
DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

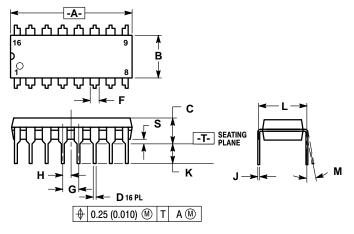
HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recog-

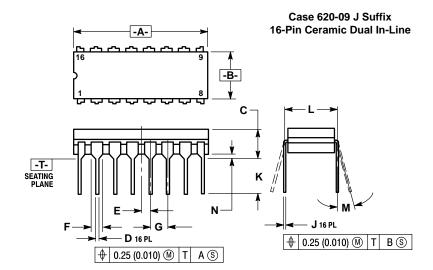
nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.



Case 648-08 N Suffix 16-Pin Plastic





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
 751B-01 IS OBSOLETE, NEW STANDARD
 751B-03.

DIM MIN A 9.80 B 3.80 C 1.35 D 0.35 F 0.40	MAX 10.00 4.00 1.75 0.49 1.25	MIN 0.386 0.150 0.054 0.014 0.016	MAX 0.393 0.157 0.068 0.019 0.049
A 9.80 B 3.80 C 1.35 D 0.35 F 0.40	10.00 4.00 1.75 0.49 1.25	0.386 0.150 0.054 0.014	0.393 0.157 0.068 0.019
B 3.80 C 1.35 D 0.35 F 0.40	4.00 1.75 0.49 1.25	0.150 0.054 0.014	0.157 0.068 0.019
C 1.35 D 0.35 F 0.40	1.75 0.49 1.25	0.054 0.014	0.068 0.019
D 0.35 F 0.40	0.49	0.014	0.019
F 0.40	1.25		
. 0.10	1.20	0.016	0.049
G 1.27			
	BSC	0.050	BSC
J 0.19	0.25	0.008	0.009
K 0.10	0.25	0.004	0.009
M 0°	7°	0°	7°
P 5.80	6.20	0.229	0.244
R 0.25	0.50	0.010	0.019

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- TO THE STATE OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD
- ROUNDED CORNERS OPTIONAL. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	18.80	19.55	0.740	0.770	
В	6.35	6.85	0.250	0.270	
С	3.69	4.44	0.145	0.175	
D	0.39	0.53	0.015	0.021	
F	1.02	1.77	0.040	0.070	
G	2.54	BSC	0.100	BSC	
Н	1.27	BSC	0.050 BSC		
J	0.21	0.38	0.008	0.015	
K	2.80	3.30	0.110	0.130	
L	7.50	7.74	0.295	0.305	
M	0°	10°	0°	10°	
S	0.51	1.01	0.020	0.040	

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L'TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU-08 OBSOLETE, NEW STANDARD 620-09.

	MILLIM	IETERS	INC	HES				
DIM	MIN	MAX	MIN	MAX				
Α	19.05	19.55	0.750	0.770				
В	6.10	7.36	0.240	0.290				
С	_	4.19	_	0.165				
D	0.39	0.53	0.015	0.021				
E	1.27	BSC	0.050 BSC					
F	1.40	1.77	0.055	0.070				
G	2.54	2.54 BSC		0.100 BSC				
J	0.23	0.27	0.009	0.011				
K	_	5.08	_	0.200				
L	7.62 BSC		0.300	BSC				
M	0°	15°	0°	15°				
N	0.39	0.88	0.015	0.035				

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