**Processor Design Project**

**Final Report**

**EE480**

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Table of Contents

[Table of Figures 4](#_Toc352703169)

[1. Introduction 5](#_Toc352703170)

[1.1. Implementation 5](#_Toc352703171)

[1.1.1. Add 5](#_Toc352703172)

[1.1.2. Sub 6](#_Toc352703173)

[1.1.3. Logical OR 6](#_Toc352703174)

[1.1.4. Logical AND 7](#_Toc352703175)

[1.1.5. Logical Complement (COMP) 8](#_Toc352703176)

[1.1.6. Multiply and Divide 8](#_Toc352703177)

[1.1.7. Arithmetic Left/Right Shift 9](#_Toc352703178)

[1.1.8. Conditional Branch 10](#_Toc352703179)

[1.1.9. Unconditional Jump 11](#_Toc352703180)

[1.1.10. Branch to a Subroutine 11](#_Toc352703181)

[1.1.11. Return from a Subroutine 12](#_Toc352703182)

[1.1.12. Return from Interrupt Service Routine 12](#_Toc352703183)

[1.1.13. LOAD Accumulator 13](#_Toc352703184)

[1.1.14. STORE Accumulator to RAM 14](#_Toc352703185)

[1.1.15. LOAD A Register from RAM 14](#_Toc352703186)

[1.1.16. STORE A Register to RAM 15](#_Toc352703187)

[1.1.17. LOAD B Register from RAM 16](#_Toc352703188)

[1.1.18. STORE B Register to RAM 17](#_Toc352703189)

[1.1.19. INPUT Data Word to RAM 17](#_Toc352703190)

[1.1.20. OUTPUT Data Word from RAM 18](#_Toc352703191)

[1.1.21. LOAD Mask Register of HVPI 19](#_Toc352703192)

[1.1.22. NOP 19](#_Toc352703193)

[2. Accumulator Architecture Development 20](#_Toc352703194)

[2.1. Architecture Overview 20](#_Toc352703195)

[2.2. Instruction Implementation 22](#_Toc352703196)

[2.2.1. Add 24](#_Toc352703197)

[2.2.2. Sub 25](#_Toc352703198)

[2.2.3. Logical OR 26](#_Toc352703199)

[2.2.4. Logical AND 27](#_Toc352703200)

[2.2.5. Logical Complement (COMP) 27](#_Toc352703201)

[2.2.6. Multiply and Divide 28](#_Toc352703202)

[2.2.7. Arithmetic Left/Right Shift 30](#_Toc352703203)

[2.2.8. Conditional Branch 31](#_Toc352703204)

[2.2.9. Unconditional Jump 31](#_Toc352703205)

[2.2.10. Branch to a Subroutine 32](#_Toc352703206)

[2.2.11. Return from a Subroutine 32](#_Toc352703207)

[2.2.12. LOAD Accumulator from RAM 33](#_Toc352703208)

[2.2.13. STORE Accumulator to RAM 35](#_Toc352703209)

[2.2.14. LOAD A Register from RAM 36](#_Toc352703210)

[2.2.15. STORE A Register to RAM 37](#_Toc352703211)

[2.2.16. LOAD B Register from RAM 38](#_Toc352703212)

[2.2.17. STORE B Register to RAM 39](#_Toc352703213)

[2.2.18. INPUT Data Word to RAM 40](#_Toc352703214)

[2.2.19. OUTPUT Data Word from RAM 41](#_Toc352703215)

[2.2.20. LOAD Mask Register of HVPI 42](#_Toc352703216)

[2.2.21. NOP 42](#_Toc352703217)

[2.3. Direct Mapped Cache 43](#_Toc352703218)

[3. Conclusion 43](#_Toc352703219)

[4. References 44](#_Toc352703220)

Table of Figures

[Figure 1 - ACC Processor Single Cycle Diagram 21](#_Toc352704788)

[Figure 2 - Start of Single Cycle Instruction Cycle 23](#_Toc352704789)

[Figure 3 - ADD Flow Diagram 24](#_Toc352704790)

[Figure 4 - SUB Flow Diagram 25](#_Toc352704791)

[Figure 5 - OR Flow Diagram 26](#_Toc352704792)

[Figure 6 - AND Flow Diagram 27](#_Toc352704793)

[Figure 7 - COMP Flow Diagram 27](#_Toc352704794)

[Figure 8 - MULT Flow Diagram 28](#_Toc352704795)

[Figure 9 - DIV Flow Diagram 29](#_Toc352704796)

[Figure 10 - SHFT Flow Diagram 30](#_Toc352704797)

[Figure 11 - BRA Flow Diagram 31](#_Toc352704798)

[Figure 12 - JMP Flow Diagram 31](#_Toc352704799)

[Figure 13 - BSR Flow Diagram 32](#_Toc352704800)

[Figure 14 - RTS Flow Diagram 32](#_Toc352704801)

[Figure 15 - LOAD Flow Diagram 34](#_Toc352704802)

[Figure 16 - STORE Flow Diagram 35](#_Toc352704803)

[Figure 17 - LDA Flow Diagram 36](#_Toc352704804)

[Figure 18 - STA Flow Diagram 37](#_Toc352704805)

[Figure 19 - LDB Flow Diagram 38](#_Toc352704806)

[Figure 20 - STB Flow Diagram 39](#_Toc352704807)

[Figure 21 - INPUT Flow Diagram 40](#_Toc352704808)

[Figure 22 - OUTPUT Flow Diagram 41](#_Toc352704809)

[Figure 23 - LMSK Flow Diagram 42](#_Toc352704810)

[Figure 24 - NOP Flow Diagram 42](#_Toc352704811)

[Figure 25 - Direct Mapped Cache Flow Diagram 43](#_Toc352704812)

# Introduction

The purpose of this project is to design, develop, test, and validate a high performing accumulator based processor capable of efficiently implementing an Instruction Set Architecture (ISA) that we specifically designed for it. By definition, the accumulator based architecture has only one register, called the accumulator, in the data path and for all ALU operations. For every ALU instruction, one operand will always be in the ACC register and the other operand comes from RAM. The process of developing the accumulator processor begins with defining the ISA and designing the physical layout of the architecture. After the architecture is designed, each clock cycle operation of the processor is defined as to show the processors operation and functionality as a system. From this, the steps of each instruction are diagramed on a cycle by cycle basis to define their exact operation by the system on the architecture.

# Overview and Objective

Beyond simply implementing an accumulator processor, the team wishes to build a robust and efficient processing unit. Operations will focus around the ALU to perform arithmetic, but additional features will be made available to do this more elaborately. The following features should be implemented within the hybrid accumulator processor:

* 2-Stage Pipelined Design
  + Stage 1 – Fetch Instructions
  + Stage 2 – Execute Instructions
* Separate Instruction and Data Memory Systems
* Fully Associative Cache for improving memory access time.
  + Least Recently Used (LRU) replacement algorithm
  + 8x faster access than memory
* Multiple Addressing Modes
  + Direct, Indirect, and Immediate
* Hardware Vectored Priority Interrupt System
  + ALU Zero Output
  + ALU Overflow
  + Invalid OPcode
  + Input/Output Ready
* Data Lines
  + 8 Bits Wide

Building a high performance hybrid accumulator processor to satisfy the outlined specifications will require the development of a custom Instruction Set Architecture (ISA). Section 4 describes the implementation of the Instruction Set Architecture. The ISA should implement control of the accumulator processor. Below specifies the required OPcode instructions to be implemented:

* ADD
* SUB
* Logical OR
* Logical AND
* Logical Compliment (COMP)
* MULT/DIV of a single operand by 2\*\*m for m, an integer, in addition to “Zeroing-Out” or “Passing-Through” the single operand.
* Arithmetic Right/Left SHIFT (by any number less than 7)
* Conditional Branch
* Unconditional Branch (JMP)
* Jump to Subroutine
* Return from Subroutine
* Return from Interrupt Subroutine
* LOAD a data path register from Random Access Memory (RAM).
* STORE a data path register to RAM
* INPUT a data word to RAM from an 8-bit INPUT Bus
  + 2 – Way handshaking protocol should be utilized.
* OUTPUT a data word from RAM to an 8-bit OUTPUT bus
  + 2 – Way handshaking protocol should be utilized.
* LOAD Mask Register of HVPI system.
* NOP (NO Operation)

Correct operation of the hybrid accumulator processor should be tested and verified. The following will be implemented to fully test the accumulator processor:

* Assembly Program Assembler
  + Input: Assembly Language Program
  + Output: Machine Code
* Write four assembly programs to test functionality
  + Straight line control flow
  + Straight line control flow with loops
  + Subroutine Execution
  + HVPI system testing
* Implement to the post place and route level.
* Test program execution using Behavioral simulation.
* Test program execution using post place and route simulation.

# Objective Summary

# Instruction Set Architecture Development

The instruction set architecture defines the computer architecture and capabilities by detailing the data types, possible instructions, registers, memory addressing modes, interrupt control, and data input/output control. Defining the instruction set architecture enables programming the computer architecture, assembly instructions and associated parameters are translated to machine code.

## Implementation

This accumulator computer architecture includes 22 OPcodes with multiple flags, which describe addressing modes and specific opcode operation. Each instruction is implemented as 16-bits wide (one word) for this accumulator processor, which features an 8-bit data bus. 5-bits are reserved for the opcode, 3-bits are reserved for the opcode flag, and 8-bits are allocated for the operand. Table 1 provides an overview of the instruction structure. The size of the operand is limited by the width of the data bus (5-bits).

Table 1 - Instruction Structure

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | 15:11 | 10:8 | 7:0 |
| Field | OPCODE | FLAG | OPERAND |

Each of the 22 opcodes are detailed in the following sections by OPCode, flags, assembly format, machine code format, description of operation, architecture level operation, and memory addressing.

### Add

|  |  |
| --- | --- |
| Instruction | Add |
| OPCode | 00000 |
| Flags | 000: Direct 001: Indirect 010: Immediate |
| Format | ADD FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00000 | xxx | RAM ADDR / INTEGER | |
| Description | Adds the specified operand to the current contents of the ACC register. The Output from the ALU will be returned to the ACC register. |
| Operation | ACC ← ACC + OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Sub

|  |  |
| --- | --- |
| Instruction | SUB |
| OPCode | 00001 |
| Flags | 000: Direct 001: Indirect 010: Immediate |
| Format | SUB FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00001 | xxx | RAM ADDR / INTEGER | |
| Description | Subtracts the specified operand from the current contents of the ACC register. The Output from the ALU will be returned to the ACC register. |
| Operation | ACC ← ACC - OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical OR

|  |  |
| --- | --- |
| Instruction | OR |
| OPCode | 00011 |
| Flags | 000: Direct 001: Indirect 010: Immediate |
| Format | OR FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00011 | xxx | RAM ADDR / INTEGER | |
| Description | Perform a LOGICAL OR operation of contents in Accumulator and OPERAND. The result of the operation will be stored in the accumulator. |
| Operation | ACC ← ACC | OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical AND

|  |  |
| --- | --- |
| Instruction | AND |
| OPCode | 00100 |
| Flags | 000: Direct 001: Indirect 010: Immediate |
| Format | AND FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00100 | xxx | RAM ADDR / INTEGER | |
| Description | Perform a LOGICAL AND operation of contents in Accumulator and OPERAND. The result of the operation will be stored in the accumulator. |
| Operation | ACC ← ACC & OPERAND |
| Memory Addressing | Immediate, Direct, and Indirect |

### Logical Complement (COMP)

|  |  |
| --- | --- |
| Instruction | COMP |
| OPCode | 10000 |
| Flags | 000 |
| Format | COMP FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10000 | 000 | 00000000 | |
| Description | Perform LOGICAL complement/Negation on the contents of the accumulator register. The complement will be stored in the accumulator register. |
| Operation | ACC ← NOT ACC |
| Memory Addressing | N/A |

### Multiply and Divide

|  |  |
| --- | --- |
| Instruction | MUL |
| OPCode | 00010 |
| Flags | 000: Direct 001: Indirect |
| Format | MUL FLAG OPERAND [Lower 4 bits] |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00010 | 000 001 | RAM ADDR | |
| Description | Performs multiplication on lower 4-bits of Accumulator and lower 4-bits of the operand. |
| Operation | ACC ← ACC \* OPERAND |
| Memory Addressing | Direct and Indirect |

|  |  |
| --- | --- |
| Instruction | DIV |
| OPCode | 00010 |
| Flags | 010: Direct 011: Indirect |
| Format | DIV FLAG OPERAND [Lower 4 bits] |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00010 | 010 011 | RAM ADDR | |
| Description | Performs division on lower 4-bits of Accumulator and lower 4-bits of the operand. |
| Operation | ACC ← ACC / OPERAND |
| Memory Addressing | Direct and Indirect |

### Arithmetic Left/Right Shift

|  |  |
| --- | --- |
| Instruction | SHFT |
| OPCode | 00101 |
| Flags | 000: Left Shift in 0 001: Left Shift in 1 |
| Format | SHFT FLAG OPPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00101 | 000 001 | INTEGER < 7 | |
| Description | Performs a LEFT SHIFT operation on the contents of the accumulator register. The value of the bit shifted in is dependent upon the provided flag. Any number of bits less than 7. |
| Operation | ACC ← ACC [N-2:0 + (FLAG BIT)\*OPERAND] |
| Memory Addressing | N/A |

|  |  |
| --- | --- |
| Instruction | SHFT |
| OPCode | 00101 |
| Flags | 010: Right Shift in 0 011: Right Shift in 1 |
| Format | SHFT FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00101 | 010 011 | INTEGER < 7 | |
| Description | Performs a RIGHT SHIFT operation on the contents of the accumulator register. The value of the bit shifted in is dependent upon the provided flag. Shift by any number of bits less than 7. |
| Operation | ACC ← ACC [OPERAND\*(FLAG BIT) + N-1:1] |
| Memory Addressing | N/A |

### Conditional Branch

|  |  |
| --- | --- |
| Instruction | BRA |
| OPCode | 00110 |
| Flags | 000: Branch if Equal 001: Branch if Not Equal |
| Format | BRA FLAG OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00110 | 000 001 | MEM ADDR | |
| Description | Performs a comparison between the Accumulator and A register. If true, jump to instruction pointed to by OPERAND.  The comparison is performed on the ACC and A registers. |
| Operation | PC ←OPERAND |
| Memory Addressing | Direct |

### Unconditional Jump

|  |  |
| --- | --- |
| Instruction | JMP |
| OPCode | 00111 |
| Flags | NULL |
| Format | JUMP OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 00111 | 000 | MEM ADDR | |
| Description | Executes an unconditional branch. When encountered the instruction pointer is adjusted to the operand target memory address. |
| Operation | IP ←IP + OPERAND |
| Memory Addressing | N/A |

### Branch to a Subroutine

|  |  |
| --- | --- |
| Instruction | BSR |
| OPCode | 10101 |
| Flags | NULL |
| Format | BSR OPERAND |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10101 | 000 | MEM ADDR | |
| Description | Transfer program control to the address specified by the operand. Before loading the program counter with the operand, the current contents of the ACC and PC should be saved to their respective stacks. |
| Operation | ACC\_STACK[0] ← ACC  PC\_STACK[0] ← PC  PC ← OPERAND |
| Memory Addressing | NULL |

### Return from a Subroutine

|  |  |
| --- | --- |
| Instruction | RTS |
| OPCode | 01000 |
| Flags | NULL |
| Format | RTS |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01000 | 000 | 00000000 | |
| Description | Transfer program control to the address located in the implied return address. Return is made to the top element in the PC stack. Should also pop the ACC value from the ACC stack. |
| Operation | PC ← PC\_STACK[0] ACC ← ACC\_STACK[0] |
| Memory Addressing | NULL |

### Return from Interrupt Service Routine

|  |  |
| --- | --- |
| Instruction | RTI |
| OPCode | 01001 |
| Flags | NULL |
| Format | RTI |
| Machine Format | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01001 | 000 | 00000000 | |
| Description | Return from an Interrupt Subroutine to the position the PC was at before the interrupt. The PC location to return to will be the top element in the PC stack. |
| Operation | PC ← Return Address (From Stack) |
| Memory Addressing | NULL |

### LOAD Accumulator

|  |  |
| --- | --- |
| Instruction | LOAD |
| OPCode | 01010 |
| Flags | 000: Direct 001: Indirect  010: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01010 | 000 001 010 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the accumulator.  **Indirect Mode:** Copy the accumulator to the destination memory address found at the memory address of the operand  **Immediate Mode:** Copy the 8-bit immediate source operand to the accumulator. |
| Operation | **Direct Mode** ACC ← memory (OPERAND)  **Indirect Mode:**  ACC ← Memory{ memory( OPERAND) }   **Immediate Mode:** ACC ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE Accumulator to RAM

|  |  |
| --- | --- |
| Instruction | STOR |
| OPCode | 01011 |
| Flags | 000: Direct 001: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01011 | 000 001 | MEM ADDR | |
| Description | **Direct Mode** Copy the accumulator to the destination memory address specified by the operand **Indirect Mode:** Copy the accumulator to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← ACC **Indirect Mode:** Memory{ memory( OPERAND) } ← ACC |
| Memory Addressing | Direct, Indirect |

### LOAD A Register from RAM

|  |  |
| --- | --- |
| Instruction | LDA |
| OPCode | 10001 |
| Flags | 000: Direct 001: Indirect  010: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10001 | 000 001 010 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the A register.  **Indirect Mode:** Copy the memory data found at the memory address of the operand into the A register.   **Immediate Mode:** Copy the 8-bit immediate source operand to the A register. |
| Operation | **Direct Mode** A ← memory (OPERAND)  **Indirect Mode:**  A ← Memory{ memory( OPERAND) }   **Immediate Mode:** A ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE A Register to RAM

|  |  |
| --- | --- |
| Instruction | STA |
| OPCode | 10010 |
| Flags | 000: Direct 001: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10010 | 000 001 | MEM ADDR | |
| Description | **Direct Mode** Copy the A register contents to the destination memory address specified by the operand **Indirect Mode:** Copy the A register contents to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← A **Indirect Mode:** Memory{ memory( OPERAND) } ← A |
| Memory Addressing | Direct, Indirect |

### LOAD B Register from RAM

|  |  |
| --- | --- |
| Instruction | LDB |
| OPCode | 10011 |
| Flags | 000: Direct 001: Indirect  010: Immediate |
| Format | LOAD FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10011 | 000 001 010 | MEM ADDR MEM ADDR Integer | |
| Description | **Direct Mode** Copy the contents of the address in RAM specified by the source operand to the B register.  **Indirect Mode:** Copy the memory data found at the memory address of the operand into the B register.   **Immediate Mode:** Copy the 8-bit immediate source operand to the B register. |
| Operation | **Direct Mode** B ← memory (OPERAND)  **Indirect Mode:**  B ← Memory{ memory( OPERAND) }   **Immediate Mode:** B ← IMMED OPERAND |
| Memory Addressing | Direct, Immediate |

### STORE B Register to RAM

|  |  |
| --- | --- |
| Instruction | STB |
| OPCode | 10100 |
| Flags | 000: Direct 001: Indirect |
| Format | STORE FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 10100 | 000 001 | MEM ADDR | |
| Description | **Direct Mode** Copy the B register contents to the destination memory address specified by the operand **Indirect Mode:** Copy the B register contents to the destination memory address found at the memory address of the operand |
| Operation | **Direct Mode** memory(OPERAND) ← B **Indirect Mode:** Memory{ memory( OPERAND) } ← B |
| Memory Addressing | Direct, Indirect |

### INPUT Data Word to RAM

|  |  |
| --- | --- |
| Instruction | INPUT |
| OPCode | 01100 |
| Flags | 000: Direct 001: Indirect |
| Format | INPUT FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01100 | 000 001 | MEM ADDR | |
| Description | Input a data word to RAM |
| Operation | **Direct Mode** memory(OPERAND) ← I/O Port  **Indirect Mode:** Memory{ memory( OPERAND) } ← I/O Port  **Flow Control**   * Wait until processor is ready to receive INPUT data. * Wait for INPUT data to become ready from connected device. * Read in INPUT data. * Notify that INPUT data has been read. |
| Memory Addressing | Direct, Indirect |

### OUTPUT Data Word from RAM

|  |  |
| --- | --- |
| Instruction | OUTPUT |
| OPCode | 01101 |
| Flags | 000: Direct 001: Indirect |
| Format | OUTPUT FLAG OPERAND |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01101 | 000 001 | MEM ADDR | |
| Description | Output data word from RAM |
| Operation | **Direct Mode** memory(OPERAND) → I/O Port  **Indirect Mode:** Memory{ memory( OPERAND) } → I/O Port  **Flow Control**   * Wait until processor data is ready to OUTPUT. * Wait until connected device is ready to receive. * Output OUTPUT data. * Output data until connected device says the data has been received. |
| Memory Addressing | Direct, Indirect |

### LOAD Mask Register of HVPI

|  |  |  |
| --- | --- | --- |
| Instruction | LMSK | |
| OPCode | 01110 | |
| Flags | | NULL |
| Format | LMSK VALUE | |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01110 | 00 | 00001000 00000100 00000010 00000001 00000000 | | |
| Description | Loads the mask register of the Maskable Hardware Vectorized Priority Interrupt System. The lower 4 bits of the operand will load into the 4 bit mask register within the MHVPIS.  Value: 1 – 1000 – ALU Output Zero Value: 2 – 0100 – ALU Overflow Value: 3 – 0010 – Illegal Opcode Value: 4 – 0001 – INPUT/OUTPUT Interrupt Value: 0 – 0000 – CLEAR mask register (disables interrupts) | |
| Operation | MASK REGISTER ← VALUE[3:0] | |
| Memory  Addressing | NULL | |

### NOP

|  |  |
| --- | --- |
| Instruction | NOP |
| OPCode | 01111 |
| Flags | NULL |
| Format | NOP |
| Format Machine | |  |  |  |  | | --- | --- | --- | --- | | Bits | 15:11 | 10:8 | 7:0 | | Field | OPCODE | FLAG | OPERAND | | Values | 01111 | 000 | 00000000 | |
| Description | Performs no operation. |
| Operation | NULL |
| Memory Addressing | NULL |

# Accumulator Architecture Development

## Architecture Overview

Figure 1 provides a single cycle diagram highlighting the accumulator processor. The hardware architecture has been designed to support the operations available in the instruction set architecture. Each of the data paths (wires) in Figure 1 are 8-bits wide. Control point and select lines are not drawn out in Figure 1 in interest of preserving space. Two memories (RAM) are used to store program data and the instruction data (programs to be executed).

Multiplexers are used to select what data exists on varying data busses at a given time. It is not desirable to have multiple data trying to output onto one bus at the same time, the current value would be unknown. Each of the multiplexer’s select lines are attached to the controller via control point lines (CP). Depending upon the opcode interpreted by the controller, the control points are set to enable the correct data to be passed to the desired function units.

It is preferred for each instruction to have a minimal cycle time, enabling the processor to execute each instruction more quickly. Every use of the ALU function unit leaves the new result stored in the accumulator register, ACC. Operations to use, load, and store the ACC register contents should be easily accessible, meaning available in very few clock cycles. The layout of the single cycle processor enables very short paths to the next functional unit. Memory access is an expensive operation, to simulate this – memory operations loop 8 clock cycles before returning results. To avoid constantly running realizing the burden of memory accesses, a direct-mapped cache is implemented. The 4 word cache mimics the L1 or L2 cache on a modern system. If the target memory address exists in the cache, the data can be returned without experiencing the 8 clock cycle delay.

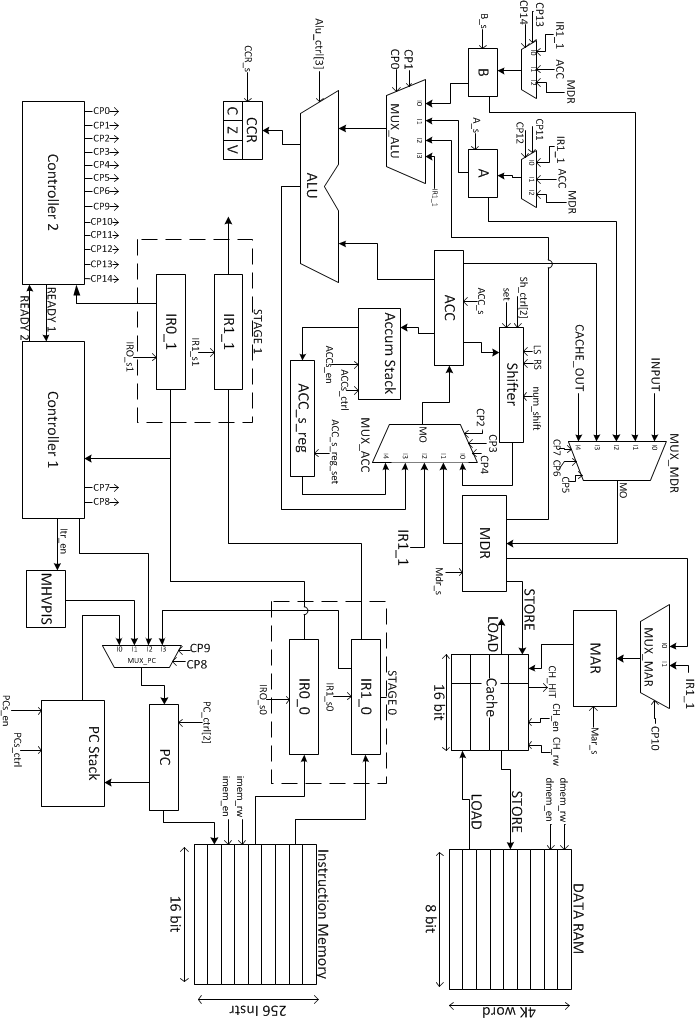


Figure 1 - ACC Processor Single Cycle Diagram

One ALU exists in the single cycle accumulator processor design. ALU operations must always include the ACC register as an input, and results are stored back into the ACC register. Operations enabling two inputs (Add, Subtract, etc.) allow input from the A, B, and MDR registers. A, B, and ACC may be loaded three different ways – direct memory addressing, indirect memory addressing, and using immediate addressing. A shifter is connected to the ACC register and enables the CPU to be programmed to shift the contents of the ACC register to the left or right by bits. Current contents of the A, B, and ACC registers may be saved into the processor’s data RAM using direct and indirect addressing schemes.

Interrupts are emitted and handled using a Masked Hardware Vectored Priority Interrupt System (MHVPIS). Divide by zero, overflow, input/output, and illegal Op-code instructions are all occurrences handled by the MHVPIS. When an interrupt is encountered, the MHVPIS points the program counter to the memory address for the interrupt service routine (ISR) to handle the interrupt.

Entering subroutines and interrupt service routines requires that the current value of the ACC register and PC be saved. Two stacks are introduced PC Stack and Accumulator Stack, to handle pushing the current register contents before entering the subroutine. When an instruction to return from subroutine is encountered the top of the stack is popped off and placed into the respective register.

## Instruction Implementation

Figure 2 highlights the initial operations performed at the beginning of every instruction execution. When control returns to the beginning of the loop, the controller must determine what the next instruction is highlighting by evaluating the Opcode and flags. Before the next instruction is read from the instruction memory, the MHVIPS is evaluated to check if an interrupt is pending. If there is an interrupt to be processed, the current contents of the PC and ACC are stored on their respective stacks and the interrupt service routine address is loaded into the program counter. Otherwise, the OPcode and instruction flag(s) into IR0 and the operand is loaded into IR1. Finally the PC is incremented to point to the next instruction in the instruction memory.



Figure 2 - Start of Single Cycle Instruction Cycle

After the initial operations have been completed, the instruction operations can be executed. The operation to be executed is determined within the controller by evaluating the contents of IR0 (OPcode + Flags). The following sections detail the processor cycles entailed for implementing each instruction. It is most desirable to have instructions complete using the minimal number of clock cycles to satisfy the instruction operation.

After each of the operations finish their loop, flow of control is directed to the pipeline handshake state. Figure 3 illustrates the logic state where the pipeline stage 1 handshaking occurs. In this state the controller communicates with the stage 0 controller to notify it that it is ready to receive an instruction. Stage 0 will notify stage 1 when it has an instruction ready to be executed. Once stage 1 begins executing the instruction, stage 1 notifies stage 0 that it has received the instruction and operand. This notification allows stage 0 to continue to its next cycle and begin fetching the next instruction. Stage 0 should generally finish always before stage 1, thus minimizing the amount of time stage 1 should have to ever wait for its next instruction to execute.



Figure 3 - Stage 1 Pipeline Handshake

### Add



Figure 4 - ADD Flow Diagram

### Sub



Figure 5 - SUB Flow Diagram

### Logical OR



Figure 6 - OR Flow Diagram

### Logical AND



Figure 7 - AND Flow Diagram

### Logical Complement (COMP)



Figure 8 - COMP Flow Diagram

### Multiply and Divide



Figure 9 - MULT Flow Diagram



Figure 10 - DIV Flow Diagram

### Arithmetic Left/Right Shift



Figure 11 - SHFT Flow Diagram

### Conditional Branch



Figure 12 - BRA Flow Diagram

### Unconditional Jump



Figure 13 - JMP Flow Diagram

### Branch to a Subroutine



Figure 14 - BSR Flow Diagram

### Return from a Subroutine



Figure 15 - RTS Flow Diagram

### Return from Interrupt Service Routine



Figure 16 - RTI State Flow

### LOAD Accumulator from RAM



Figure 17 - LOAD Flow Diagram

### STORE Accumulator to RAM



Figure 18 - STORE Flow Diagram

### LOAD A Register from RAM



Figure 19 - LDA Flow Diagram

### STORE A Register to RAM



Figure 20 - STA Flow Diagram

### LOAD B Register from RAM



Figure 21 - LDB Flow Diagram

### STORE B Register to RAM



Figure 22 - STB Flow Diagram

### INPUT Data Word to RAM



Figure 23 - INPUT Flow Diagram

### OUTPUT Data Word from RAM



Figure 24 - OUTPUT Flow Diagram

### LOAD Mask Register of HVPI



Figure 25 - LMSK Flow Diagram

### NOP



Figure 26 - NOP Flow Diagram

## Fully Associative Cache



Figure 27 – Fully Associative Cache Flow Diagram

# State Control

# Hierarchal Description of Processor



Figure 28 - ACC Processor Top Level Schematic

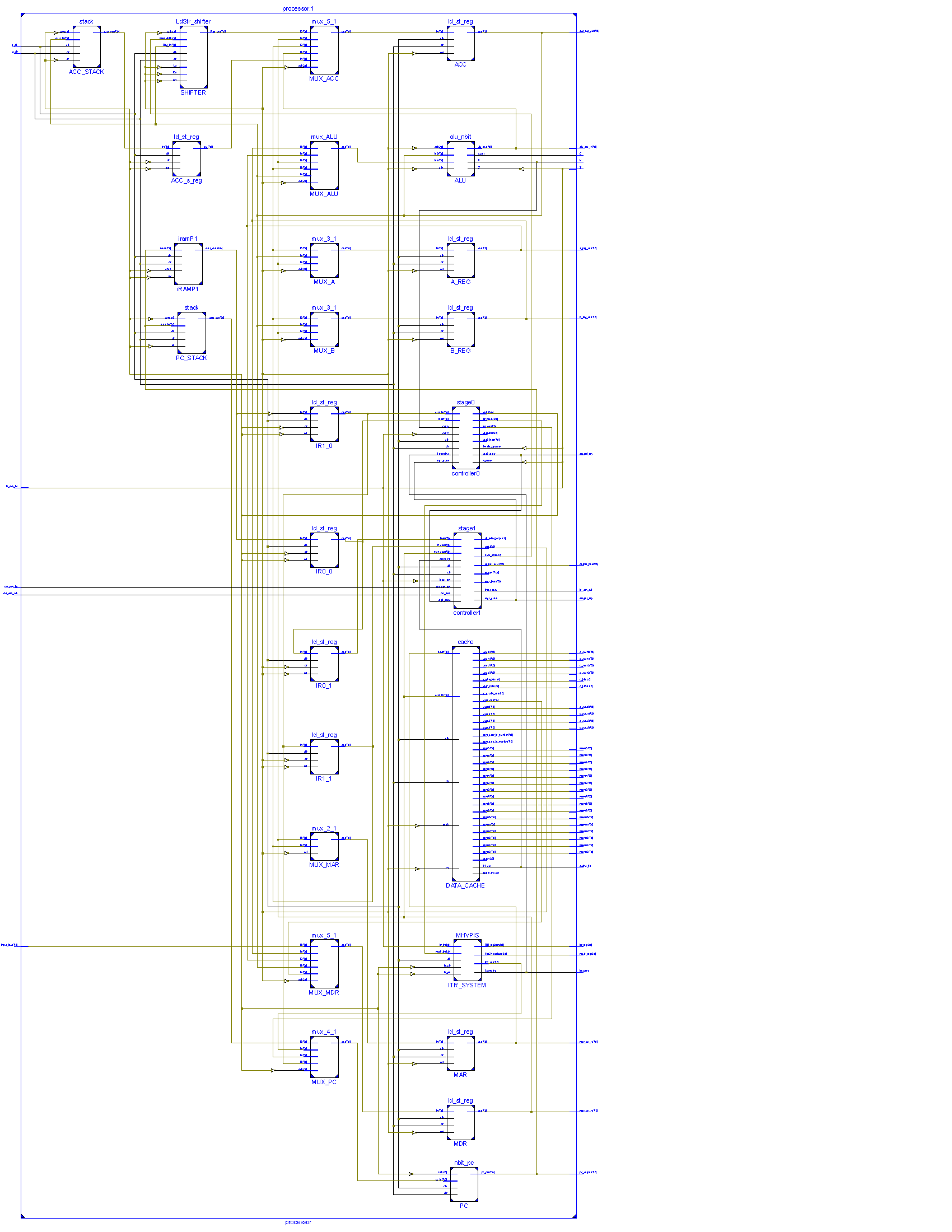


Figure 29 - ACC Processor Bottom Level Schematic (Functional Unit Level)

# Verilog Description of Processor

## Processor.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Proccessor

//

//

//////////////////////////////////////////////////////////////////////////////////

/\* DEBUG IO Port Mapping

module processor(g\_clk, g\_clr, in\_dev\_hs, out\_dev\_hs, out\_dev\_ack, in\_dev\_ack,

input\_bus, output\_bus, mem0, mem1, mem2, mem3, mem4, mem5, mem6,

mem7, mem8, mem9, mem10, mem11, mem12, mem13, mem14, mem15,

c\_data0, c\_data1, c\_data2, c\_data3, c\_addr0, c\_addr1, c\_addr2,

c\_addr3, c\_hit, c\_LRU, cache\_hit, C, V, Z, stage0, stage1,

stage0\_rdy, stage1\_rdy, stg1\_instr, stg0\_instr, pc\_output, acc\_reg\_out, alu\_out\_w,

a\_reg\_out, b\_reg\_out, mar\_out\_w, mdr\_out\_w, num\_shift\_out, shifter\_out, ch\_output ,

ch\_target\_rw, ch\_target\_data, ch\_state, ram\_data\_in, ram\_addr\_in, ch\_miss\_loop,

itr\_pend, itr\_reg, mask\_reg, pc\_s\_out, acc\_s\_out);

\*/

**module** processor**(**g\_clk**,** g\_clr**,** in\_dev\_hs**,** out\_dev\_hs**,** out\_dev\_ack**,** in\_dev\_ack**,** input\_bus**,** output\_bus**,** mem0**,** mem1**,** mem2**,** mem3**,** mem4**,** mem5**,** mem6**,** mem7**,** mem8**,** mem9**,** mem10**,** mem11**,** mem12**,** mem13**,** mem14**,** mem15**,** c\_data0**,** c\_data1**,** c\_data2**,** c\_data3**,** c\_addr0**,** c\_addr1**,** c\_addr2**,**c\_addr3**,** c\_hit**,** c\_LRU**,** cache\_hit**,** C**,** V**,** Z**,** stage0\_rdy**,** stage1\_rdy**,** pc\_output**,** acc\_reg\_out**,** alu\_out\_w**,** a\_reg\_out**,** b\_reg\_out**,** mar\_out\_w**,** mdr\_out\_w**,** itr\_pend**,** itr\_reg**,** mask\_reg**);**

//Define Inputs

**input** g\_clk**;** //Global Clock

**input** g\_clr**;** //Global g\_clr

**input** in\_dev\_hs**;** //INPUT Device Handshake - Data Ready

**input** out\_dev\_hs**;** //OUTPUT Device Handhsake - Device Ready to Receive

**input** out\_dev\_ack**;** //OUTPUT Device Handshake - Data received

**input** **[**7**:**0**]** input\_bus**;** //INPUT data bus

//Define Outputs

**output** in\_dev\_ack**;** //INPUT Device Handshake - Data Received by proc

**output** **[**7**:**0**]** output\_bus**;** //OUTPUT data bus

**output** **[**7**:**0**]** pc\_output**;**

// output [71:0] stage1;

// output [15:0] stage0;

**output** stage0\_rdy**,** stage1\_rdy**;**

**output** **[**7**:**0**]** acc\_reg\_out**;**

**output** **[**7**:**0**]** alu\_out\_w**;**

**output** **[**7**:**0**]** a\_reg\_out**;**

**output** **[**7**:**0**]** b\_reg\_out**;**

**output** **[**7**:**0**]** mdr\_out\_w**;**

**output** **[**7**:**0**]** mar\_out\_w**;**

**output** C**,** V**,** Z**;**

// output [2:0] num\_shift\_out;

// output [7:0] shifter\_out;

// output [7:0] ch\_output;

// output [7:0] ch\_target\_data;

// output ch\_target\_rw;

// output [3:0] ch\_state;

// output [7:0] ram\_data\_in;

// output [7:0] ram\_addr\_in;

// output [4:0] ch\_miss\_loop;

**output** itr\_pend**;**

**output** **[**3**:**0**]** mask\_reg**,** itr\_reg**;**

// output [7:0] pc\_s\_out, acc\_s\_out;

//Cache Outputs

**output** **[**7**:**0**]** mem0**,** mem1**,** mem2**,** mem3**,** mem4**,** mem5**,** mem6**,** mem7**;**

**output** **[**7**:**0**]** mem8**,** mem9**,** mem10**,** mem11**,** mem12**,** mem13**,** mem14**,** mem15**;**

**output** **[**7**:**0**]** c\_data0**,** c\_data1**,** c\_data2**,** c\_data3**;**

**output** **[**7**:**0**]** c\_addr0**,** c\_addr1**,** c\_addr2**,** c\_addr3**;**

**output** **[**1**:**0**]** c\_hit**,** c\_LRU**;**

**output** cache\_hit**;**

// output [7:0] stg0\_instr, stg1\_instr; //DEBUG OUTPUT

**wire** **[**7**:**0**]** stg0\_instr\_w**,** stg1\_instr\_w**;**

// assign stg0\_instr = stg0\_instr\_w; //DEBUG OUTPUT

// assign stg1\_instr = stg1\_instr\_w; //DEBUG OUTPUT

//////////////////////////////////////////////////////////////////////////////////

//////////////////////// Wire Definitions //////////////////////////////////////

//////////////////////////////////////////////////////////////////////////////////

//State Control Lines

**wire** **[**20**:**0**]** ctrl0**;**

**wire** **[**35**:**0**]** ctrl1**;**

**wire** **[**71**:**0**]** state1\_w**;**

**wire** **[**15**:**0**]** state0\_w**;**

//assign stage1 = state1\_w; //DEBUG OUTPUT

//assign stage0 = state0\_w; //DEBUG OUTPUT

//Controller Wires

**wire** stg1\_state**,** stg0\_state**,** stg1\_state2**;**

**wire** **[**7**:**0**]** stg0\_pc**;**

**wire** **[**4**:**0**]** ch\_miss\_loop\_wire**;**

**assign** ch\_miss\_loop **=** ch\_miss\_loop\_wire**;**

**wire** **[**7**:**0**]** output\_bus\_w**;**

**assign** output\_bus **=** output\_bus\_w**;**

//Instruction Memory Wire

**wire** imem\_rw**,** imem\_en**;**

**assign** imem\_rw **=** ctrl0**[**11**];**

**assign** imem\_en **=** ctrl0**[**10**];**

**wire** **[**15**:**0**]** imem\_out**;**

//Condition Code Registers

**wire** ccr\_V**,** ccr\_Z**,** ccr\_C**;**

//MHVPIS Wire

**wire** **[**3**:**0**]** itr\_in**,** itr\_mask**,** itr\_out**,** itr\_mask\_out**;**

**wire** itr\_en**,** i\_pending**,** itr\_clr**,** invalid\_opcode**;**

**wire** **[**7**:**0**]** itr\_pc\_addr**;**

**wire** v\_state**;**

**assign** itr\_clr **=** ctrl0**[**9**];**

**assign** itr\_en **=** ctrl0**[**8**];**

**assign** itr\_in**[**0**]** **=** ccr\_Z**;**

**assign** itr\_in**[**1**]** **=** v\_state**;**

**assign** itr\_in**[**2**]** **=** invalid\_opcode**;**

**assign** itr\_in**[**3**]** **=** in\_dev\_hs**;**

**assign** itr\_pend **=** i\_pending**;**

**assign** itr\_reg **=** itr\_out**;**

**assign** mask\_reg **=** itr\_mask\_out**;**

//Instruction Registers

**wire** **[**7**:**0**]** ir1\_0\_in**,** ir1\_0\_out**,** ir0\_0\_in**,** ir0\_0\_out**;**

**wire** **[**7**:**0**]** ir1\_1\_out**,** ir0\_1\_out**;**

**wire** ir1\_0\_s**,** ir0\_0\_s**,** ir1\_1\_s**,** ir0\_1\_s**;**

**wire** ir1\_0\_c**,** ir0\_0\_c**,** ir1\_1\_c**,** ir0\_1\_c**;**

**assign** ir0\_0\_s **=** ctrl0**[**14**];**

**assign** ir0\_0\_c **=** ctrl0**[**15**];**

**assign** ir1\_0\_s **=** ctrl0**[**16**];**

**assign** ir1\_0\_c **=** ctrl0**[**17**];**

**assign** ir0\_1\_s **=** ctrl1**[**19**];**

**assign** ir0\_1\_c **=** ctrl1**[**20**];**

**assign** ir1\_1\_s **=** ctrl1**[**17**];**

**assign** ir1\_1\_c **=** ctrl1**[**18**];**

**assign** ir1\_0\_in **=** imem\_out**[**7**:**0**];**

**assign** ir0\_0\_in **=** imem\_out**[**15**:**8**];**

//Shifter Wires

**wire** **[**7**:**0**]** shft\_out**;**

**wire** **[**1**:**0**]** sh\_ctrl**;**

**wire** **[**2**:**0**]** num\_shift**;**

**wire** sh\_set**,** LS**,** RS**;**

**assign** sh\_ctrl **=** ctrl1**[**4**:**3**];**

**assign** LS **=** ctrl1**[**2**];**

**assign** RS **=** ctrl1**[**1**];**

**assign** sh\_set **=** ctrl1**[**0**];**

//assign num\_shift\_out = num\_shift; //DEBUG OUTPUT

//assign shifter\_out = shft\_out; //DEBUG OUTPUT

//Cache Wires

**wire** **[**7**:**0**]** cache\_out**,** ch\_addr0**,** ch\_addr1**,** ch\_addr2**,** ch\_addr3**;**

**wire** **[**7**:**0**]** ch\_data0**,** ch\_data1**,** ch\_data2**,** ch\_data3**;**

**wire** ch\_en**,** ch\_rw**,** ch\_hit**;**

**wire** **[**1**:**0**]** curr\_hit**,** ch\_LRU**;**

**wire** **[**7**:**0**]** ram0**,** ram1**,** ram2**,** ram3**,** ram4**,** ram5**,** ram6**,** ram7**;**

**wire** **[**7**:**0**]** ram8**,** ram9**,** ram10**,** ram11**,** ram12**,** ram13**,** ram14**,** ram15**;**

**wire** cache\_target\_rw**;**

**wire** **[**7**:**0**]** ch\_target\_data\_wire**,** ch\_ram\_data**,** ch\_ram\_addr**;**

**wire** **[**3**:**0**]** ch\_state\_w**;**

**assign** ch\_en **=** ctrl1**[**23**];**

**assign** ch\_rw **=** ctrl1**[**22**];**

// assign ch\_output = cache\_out; //DEBUG OUTPUT

// assign ch\_target\_rw = cache\_target\_rw; //DEBUG OUTPUT

// assign ch\_target\_data = ch\_target\_data\_wire; //DEBUG OUTPUT

// assign ch\_state = ch\_state\_w; //DEBUG OUTPUT

// assign ram\_data\_in = ch\_ram\_data; //DEBUG OUTPUT

// assign ram\_addr\_in = ch\_ram\_addr; //DEBUG OUTPUT

//Program Counter Wire

**wire** **[**1**:**0**]** pc\_ctrl**;**

**assign** pc\_ctrl **=** ctrl0**[**19**:**18**];**

**wire** **[**7**:**0**]** pc\_in**,** pc\_out**;**

**assign** pc\_output **=** pc\_out**;**

//Stack Wire

**wire** **[**1**:**0**]** PCs\_ctrl**,** ACCs\_ctrl**;**

**wire** PCs\_en**,** ACCs\_en**;**

**wire** **[**7**:**0**]** pc\_stack\_out**,** acc\_stack\_out**;**

**assign** PCs\_ctrl **=** ctrl0**[**4**:**3**];**

**assign** PCs\_en **=** ctrl0**[**5**];**

**assign** ACCs\_ctrl **=** ctrl0**[**1**:**0**];**

**assign** ACCs\_en **=** ctrl0**[**2**];**

// assign pc\_s\_out = pc\_stack\_out; //DEBUG OUTPUT

// assign acc\_s\_out = acc\_stack\_out; //DEBUG OUTPUT

//ALU Wires

**wire** **[**2**:**0**]** alu\_ctrl**;**

**assign** alu\_ctrl **=** ctrl1**[**32**:**30**];**

**wire** alu\_cin**;**

**assign** alu\_cin **=** ctrl1**[**29**];**

**wire** **[**7**:**0**]** ALU\_in1**,** alu\_out**;**

**assign** alu\_out\_w **=** alu\_out**;**

//Data Register Wires

**wire** **[**7**:**0**]** mdr\_in**,** mdr\_out**,** mar\_in**,** mar\_out**,** acc\_s\_reg\_out**;**

**wire** **[**7**:**0**]** b\_reg\_in**,** b\_out**,** a\_reg\_in**,** a\_out**,** acc\_in**,** acc\_out**;**

**wire** mar\_s**,** mdr\_s**,** a\_s**,** b\_s**,** acc\_s**,** acc\_s\_reg\_g\_clr**,** acc\_s\_reg\_set**;**

**assign** mar\_s **=** ctrl1**[**16**];**

**assign** mdr\_s **=** ctrl1**[**15**];**

**assign** a\_s **=** ctrl1**[**34**];**

**assign** b\_s **=** ctrl1**[**26**];**

**assign** acc\_s **=** ctrl1**[**33**];**

**assign** acc\_s\_reg\_g\_clr **=** ctrl0**[**13**];**

**assign** acc\_s\_reg\_set **=** ctrl0**[**12**];**

**assign** acc\_reg\_out **=** acc\_out**;**

**assign** a\_reg\_out **=** a\_out**;**

**assign** b\_reg\_out **=** b\_out**;**

**assign** mdr\_out\_w **=** mdr\_out**;**

**assign** mar\_out\_w **=** mar\_out**;**

//////////////////////////////////////////////////////////////////////////////////

//////////////////////// Controller Units //////////////////////////////////////

//////////////////////////////////////////////////////////////////////////////////

//Controllers

**wire** **[**7**:**0**]** ctrl0\_pc**;**

//stage0(clk, clr, instr, data\_in, i\_pending, ccr\_z, ccr\_v, stg1\_state,

// stg0\_state, ctrl, pc\_out, itr\_mask, stage0, stg0\_instr, v\_state,

// invalid\_opcode);

stage0 controller0**(**g\_clk**,**g\_clr**,**ir0\_0\_out**,**ir1\_0\_out**,**i\_pending**,**ccr\_Z**,**

ccr\_V**,** stg1\_state**,** stg0\_state**,** ctrl0**,** stg0\_pc**,**

itr\_mask**,** state0\_w**,** stg0\_instr\_w**,** v\_state**,**

invalid\_opcode**);**

//stage1(clk, clr, instr, ir\_data, mdr\_data, stg0\_state, input\_rdy, out\_recv,

// out\_dev\_rdy, cache\_hit, stg1\_state, ctrl, num\_shift, input\_recv, stage1,

// output\_data, stg1\_instr, ch\_miss\_loop);

stage1 controller1**(**g\_clk **,**g\_clr**,** ir0\_1\_out**,** ir1\_1\_out**,** mdr\_out**,** stg0\_state**,**

in\_dev\_hs**,** out\_dev\_ack**,** out\_dev\_hs**,** ch\_hit**,** stg1\_state**,**

ctrl1**,** num\_shift**,** in\_dev\_ack**,** state1\_w**,**

output\_bus\_w**,** stg1\_instr\_w**,** ch\_miss\_loop\_wire**);**

**assign** stage1\_rdy **=** stg1\_state**;**

**assign** stage0\_rdy **=** stg0\_state**;**

//MHVPIS

//MHVPIS(g\_clk, itr\_g\_clr, itr\_in, mask\_in, itr\_en, i\_pending, PC\_out);

MHVPIS ITR\_SYSTEM**(**g\_clk**,** itr\_clr**,** itr\_in**,** itr\_mask**,** itr\_en**,** i\_pending**,** itr\_pc\_addr**,** itr\_out**,** itr\_mask\_out**);**

//////////////////////////////////////////////////////////////////////////////////

//////////////////////// Functional Units //////////////////////////////////////

//////////////////////////////////////////////////////////////////////////////////

//ALU

//module alu\_nbit(in0,in1,c\_in,ctrl,c\_out,alu\_out,V, Z);

alu\_nbit ALU**(**acc\_out**,** ALU\_in1**,** alu\_cin**,** alu\_ctrl**,** ccr\_C**,** alu\_out**,** ccr\_V**,** ccr\_Z**);**

//Program Counter

//module nbit\_pc(g\_clk,g\_clr, ctrl, pc\_in, pc\_out);

nbit\_pc PC**(**g\_clk**,** g\_clr**,** pc\_ctrl**,** pc\_in**,** pc\_out**);**

//Data Cache + Data RAM

cache DATA\_CACHE**(**g\_clk**,** g\_clr**,** ch\_en**,** ch\_rw**,** mar\_out**,** mdr\_out**,** cache\_out**,** ch\_hit**,**

ch\_addr0**,** ch\_addr1**,** ch\_addr2**,** ch\_addr3**,**

ch\_data0**,** ch\_data1**,** ch\_data2**,** ch\_data3**,**

ram0**,** ram1**,** ram2**,** ram3**,** ram4**,** ram5**,** ram6**,** ram7**,** ram8**,** ram9**,** ram10**,** ram11**,** ram12**,** ram13**,** ram14**,** ram15**,**

ch\_LRU**,** curr\_hit**,** cache\_target\_rw**,** ch\_target\_data\_wire**,** ch\_state\_w**,** ch\_ram\_data**,** ch\_ram\_addr**);**

//Assign Outputs to wires

**assign** mem0 **=** ram0**;**

**assign** mem1 **=** ram1**;**

**assign** mem2 **=** ram2**;**

**assign** mem3 **=** ram3**;**

**assign** mem4 **=** ram4**;**

**assign** mem5 **=** ram5**;**

**assign** mem6 **=** ram6**;**

**assign** mem7 **=** ram7**;**

**assign** mem8 **=** ram8**;**

**assign** mem9 **=** ram9**;**

**assign** mem10 **=** ram10**;**

**assign** mem11 **=** ram11**;**

**assign** mem12 **=** ram12**;**

**assign** mem13 **=** ram13**;**

**assign** mem14 **=** ram14**;**

**assign** mem15 **=** ram15**;**

**assign** c\_data0 **=** ch\_data0**;**

**assign** c\_data1 **=** ch\_data1**;**

**assign** c\_data2 **=** ch\_data2**;**

**assign** c\_data3 **=** ch\_data3**;**

**assign** c\_addr0 **=** ch\_addr0**;**

**assign** c\_addr1 **=** ch\_addr1**;**

**assign** c\_addr2 **=** ch\_addr2**;**

**assign** c\_addr3 **=** ch\_addr3**;**

**assign** c\_hit **=** curr\_hit**;**

**assign** c\_LRU **=** ch\_LRU**;**

**assign** cache\_hit **=** ch\_hit**;**

**assign** C **=** ccr\_C**;**

**assign** V **=** ccr\_V**;**

**assign** Z **=** ccr\_Z**;**

//Stacks

//module stack(en, g\_clr, g\_clk, con, data\_in, data\_out);

stack PC\_STACK**(**PCs\_en**,** g\_clr**,** g\_clk**,** PCs\_ctrl**,** pc\_out**,** pc\_stack\_out**);**

stack ACC\_STACK**(**ACCs\_en**,** g\_clr**,** g\_clk**,** ACCs\_ctrl**,** acc\_out**,** acc\_stack\_out**);**

//Shifter

//LdStr\_shifter(Reg\_in,g\_clr,set,g\_clk,Ls,Rs,ctrl,num\_shift,Reg\_out);

LdStr\_shifter SHIFTER**(**acc\_out**,** g\_clr**,** sh\_set**,** g\_clk**,** LS**,** RS**,** sh\_ctrl**,** num\_shift**,** shft\_out**);**

//Load Store Registers

//module ld\_st\_reg(g\_clk, g\_clr, set, in, out);

//Instruction Registers

ld\_st\_reg IR1\_0**(**g\_clk**,** ir1\_0\_c**,** ir1\_0\_s**,** ir1\_0\_in**,** ir1\_0\_out**);** //Stage 0 OPERAND REG

ld\_st\_reg IR0\_0**(**g\_clk**,** ir0\_0\_c**,** ir0\_0\_s**,** ir0\_0\_in**,** ir0\_0\_out**);** //Stage 0 INSTR REG

ld\_st\_reg IR1\_1**(**g\_clk**,** ir1\_1\_c**,** ir1\_1\_s**,** ir1\_0\_out**,** ir1\_1\_out**);** //Stage 1 OPERAND REG

ld\_st\_reg IR0\_1**(**g\_clk**,** ir0\_1\_c**,** ir0\_1\_s**,** ir0\_0\_out**,** ir0\_1\_out**);** //Stage 1 INSTR REG

//Data Registers

ld\_st\_reg MDR**(**g\_clk**,** g\_clr**,** mdr\_s**,** mdr\_in**,** mdr\_out**);** //Stage 1 - MDR REG

ld\_st\_reg MAR**(**g\_clk**,** g\_clr**,** mar\_s**,** mar\_in**,** mar\_out**);** //Stage 1 - MAR REG

ld\_st\_reg A\_REG**(**g\_clk**,** g\_clr**,** a\_s**,** a\_reg\_in**,** a\_out**);**

ld\_st\_reg B\_REG**(**g\_clk**,** g\_clr**,** b\_s**,** b\_reg\_in**,** b\_out**);**

ld\_st\_reg ACC**(**g\_clk**,** g\_clr**,** acc\_s**,** acc\_in**,** acc\_out**);** //ACCUMULATOR REG

ld\_st\_reg ACC\_s\_reg**(**g\_clk**,** acc\_s\_reg\_g\_clr**,** acc\_s\_reg\_set**,** acc\_stack\_out**,** acc\_s\_reg\_out**);**

//////////////////////////////////////////////////////////////////////////////////

//////////////////////// Instruction Memory ////////////////////////////////////

//////////////////////////////////////////////////////////////////////////////////

//module ram(g\_clk, g\_clr, enab, rw, Addr, data\_out);

//iram iRAM(g\_clk, g\_clr, imem\_en, imem\_rw, pc\_out, imem\_out);

iramP1 iRAMP1**(**g\_clk**,** g\_clr**,** imem\_en**,** imem\_rw**,** pc\_out**,** imem\_out**);**

//iramFib iRAMFib(g\_clk, g\_clr, imem\_en, imem\_rw, pc\_out, imem\_out);

//iramITR iRAM\_ITR(g\_clk, g\_clr, imem\_en, imem\_rw, pc\_out, imem\_out);

//iramSUB iRAM\_ITR(g\_clk, g\_clr, imem\_en, imem\_rw, pc\_out, imem\_out);

//////////////////////////////////////////////////////////////////////////////////

//////////////////////// Multiplexers //////////////////////////////////////////

//////////////////////////////////////////////////////////////////////////////////

//MUX Select Lines

**wire** CP10**;**

**wire** **[**1**:**0**]** CP8\_9**,** CP12\_11**,** CP14\_13**;**

**wire** **[**2**:**0**]** CP1\_0**,** CP4\_3\_2**,** CP7\_6\_5**;**

**assign** CP1\_0 **=** ctrl1**[**11**:**9**];**

**assign** CP4\_3\_2 **=** ctrl1**[**14**:**12**];**

**assign** CP7\_6\_5 **=** ctrl1**[**7**:**5**];**

**assign** CP8\_9 **=** ctrl0**[**7**:**6**];**

**assign** CP10 **=** ctrl1**[**8**];**

**assign** CP12\_11 **=** ctrl1**[**28**:**27**];**

**assign** CP14\_13 **=** ctrl1**[**25**:**24**];**

//MUX Units

//module mux\_2\_1(i0, i1, sel, out);

mux\_2\_1 MUX\_MAR**(**mdr\_out**,** ir1\_1\_out**,** CP10**,** mar\_in**);**

//mux\_4\_1(i0, i1, i2, i3, sel, out);

mux\_4\_1 MUX\_PC**(**pc\_stack\_out**,** itr\_pc\_addr**,** stg0\_pc**,** ir1\_0\_out**,** CP8\_9**,** pc\_in**);**

mux\_3\_1 MUX\_A**(**ir1\_1\_out**,** acc\_out**,** mdr\_out**,** CP12\_11**,** a\_reg\_in**);**

mux\_3\_1 MUX\_B**(**ir1\_1\_out**,** acc\_out**,** mdr\_out**,** CP14\_13**,** b\_reg\_in**);**

//module mux\_5\_1(i0, i1, i2, i3, i4, sel, out);

mux\_5\_1 MUX\_ACC**(**shft\_out**,** mdr\_out**,** ir1\_1\_out**,** alu\_out**,** acc\_s\_reg\_out**,**

CP4\_3\_2**,** acc\_in**);**

mux\_5\_1 MUX\_MDR**(**input\_bus**,** b\_out**,** a\_out**,** acc\_out**,** cache\_out**,**

CP7\_6\_5**,** mdr\_in**);**

mux\_ALU MUX\_ALU**(**b\_out**,** a\_out**,** mdr\_out**,** ir1\_1\_out**,** acc\_out**,** CP1\_0**,** ALU\_in1**);**

**endmodule**

## stage0.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Controller Unit 0

//

// Moore Model Finite State Machine (FSM) implements control of stage 0 of the

// accumulator processor.

//

//////////////////////////////////////////////////////////////////////////////////

**module** stage0**(**clk**,** clr**,** instr**,** data\_in**,** i\_pending**,** ccr\_z**,** ccr\_v**,** stg1\_state**,**

stg0\_state**,** ctrl**,** pc\_out**,** itr\_mask**,** stage0**,** stg0\_instr**,** v\_state**,**

invalid\_opcode**);**

//Inputs

**input** clk**,** clr**;**

**input** ccr\_z**;** //Condition Code Register Z - Zero Flag (For Branch)

**input** ccr\_v**;** //Identify overflow and hold value while spinning

**input** i\_pending**;** //Pending interrupt signal sent from MHVPIS

//input [7:0] data; //Contents of IR0\_0 - Data Register

**input** **[**7**:**0**]** instr**;** //Contents of IR0\_0 - Instruction Register

**input** stg1\_state**;** //Handshake control line - Stage 1 interface

**input** **[**7**:**0**]** data\_in**;** //Contents of IR1\_0 - Operand Register

//Outputs

**output** **reg** stg0\_state**;** //Handshake control line - Stage 0 (this unit) status

**output** **reg** **[**7**:**0**]** pc\_out**;** //Used to set PC address

**output** **reg** **[**20**:**0**]** ctrl**;** //21 bit control line - control and select points

**output** **reg** **[**15**:**0**]** stage0**;** //Current Controller state

**output** **[**7**:**0**]** stg0\_instr**;**

**output** **reg** **[**3**:**0**]** itr\_mask**;** //Output ITR mask

**output** **reg** v\_state**;**

**output** **reg** invalid\_opcode**;** //Flag for bad opcode discovered in valid block (T5)

**wire** **[**7**:**0**]** stg0\_instr\_w**;**

**assign** stg0\_instr\_w **=** instr**;**

**assign** stg0\_instr **=** stg0\_instr\_w**;**

//Define Stage 0 state parameters

**parameter** T0 **=** 16'b0000000000000001**;**

**parameter** T1 **=** 16'b0000000000000010**;** //Logic States

**parameter** T2 **=** 16'b0000000000000100**;**

**parameter** T3 **=** 16'b0000000000001000**;**

**parameter** T4 **=** 16'b0000000000010000**;**

**parameter** T5 **=** 16'b0000000000100000**;** //Logic States

**parameter** T6 **=** 16'b0000000001000000**;**

**parameter** T7 **=** 16'b0000000010000000**;** //Logic States

**parameter** T8 **=** 16'b0000000100000000**;** //Logic States

**parameter** T9 **=** 16'b0000001000000000**;** //Logic States

**parameter** T10 **=** 16'b0000010000000000**;**

**parameter** T11 **=** 16'b0000100000000000**;** //Logic States

**parameter** T12 **=** 16'b0001000000000000**;**

**parameter** T13 **=** 16'b0010000000000000**;**

**parameter** T14 **=** 16'b0100000000000000**;**

**parameter** T15 **=** 16'b1000000000000000**;**

//Define Stage 0 control points

**parameter** CP0**=**21'b101101010010010110110**;**

**parameter** CP1**=**21'b100101010011100110110**;**

**parameter** CP2**=**21'b100101010011100100100**;**

**parameter** CP3**=**21'b101101010011101110110**;**

**parameter** CP4**=**21'b100111110011100110110**;**

**parameter** CP5**=**21'b100101010011100110110**;**

**parameter** CP6**=**21'b110101010011100110110**;**

**parameter** CP7**=**21'b100101010011100110110**;**

**parameter** CP8**=**21'b100101010011100110110**;**

**parameter** CP9**=**21'b100101010011100110110**;**

**parameter** CP10**=**21'b101101010011111110110**;**

**parameter** CP11**=**21'b100101010011100110110**;**

**parameter** CP12**=**21'b100101010011100100100**;**

**parameter** CP13**=**21'b100101010010100101101**;**

**parameter** CP14**=**21'b100101010011100110110**;**

**parameter** CP15**=**21'b101101011010100111111**;**

//Define OPcodes that will be executed by this controller

**parameter** BRA **=** 5'b00110**;**

**parameter** JMP **=** 5'b00111**;**

**parameter** BSR **=** 5'b10101**;**

**parameter** RTS **=** 5'b01000**;**

**parameter** RTI **=** 5'b01001**;**

**parameter** LMSK **=** 5'b01110**;**

//Define all other opcodes

**parameter** opADD **=** 5'b00000**;**

**parameter** opSUB **=** 5'b00001**;**

**parameter** opOR **=** 5'b00011**;**

**parameter** opAND **=** 5'b00100**;**

**parameter** opCOMP **=** 5'b10000**;**

**parameter** opMULDIV **=** 5'b00010**;**

**parameter** opSHFT **=** 5'b00101**;**

**parameter** opLOAD **=** 5'b01010**;**

**parameter** opSTOR **=** 5'b01011**;**

**parameter** opLDA **=** 5'b10001**;**

**parameter** opSTA **=** 5'b10010**;**

**parameter** opLDB **=** 5'b10011**;**

**parameter** opSTB **=** 5'b10100**;**

**parameter** opINPUT **=** 5'b01100**;**

**parameter** opOUTPUT **=** 5'b01101**;**

**parameter** opNOP **=** 5'b01111**;**

//Define flags

**parameter** BEQ **=** 3'b000**;** //BRA - If Equal

**parameter** BNE **=** 3'b001**;** //BRA - If Not Equal

//Control Flags

**reg** **[**2**:**0**]** bra\_loop**;** //Branch Wait Flag

**reg** itr\_state**;** //1: Handling Interrupt 0: No ITR

**reg** itr\_pc\_loop**;**

**initial** **begin**

pc\_out **<=** 8'b00000000**;**

bra\_loop **<=** 3'b000**;**

itr\_state **<=** 1'b0**;**

itr\_pc\_loop **<=** 1'b0**;**

v\_state **<=** 1'b0**;**

invalid\_opcode **<=** 1'b0**;**

**end**

**always** **@** **(posedge** clk**)** **begin**

**if(**clr**==**1'b0**)** **begin**

stage0 **<=** T0**;**

**end**

**else** **begin**

**case(**stage0**)**

T0**:** stage0 **<=** T4**;**

T1**:** **if((**i\_pending**==**1'b1**)&&(**itr\_state**==**1'b0**))** **begin** stage0 **<=** T2**;** **end**

**else** **begin** stage0 **<=** T4**;** **end**

T2**:** **begin**

stage0 **<=** T3**;**

itr\_state **<=** 1'b1**;**

**end**

T3**:** **if(**itr\_pc\_loop**==**1'b1**)** **begin**

stage0 **<=** T4**;**

itr\_pc\_loop **<=** 1'b0**;**

**end**

**else** **begin**

itr\_pc\_loop **<=** **(**itr\_pc\_loop **+** 1**);**

stage0 **<=** T3**;**

**end**

T4**:** stage0 **<=** T5**;**

T5**:** **case(**instr**[**7**:**3**])** //Determine next state

BRA**:** stage0 **<=** T8**;**

JMP**:** stage0 **<=** T10**;**

BSR**:** stage0 **<=** T12**;**

RTS**:** stage0 **<=** T13**;**

RTI**:** stage0 **<=** T13**;**

LMSK**:** stage0 **<=** T14**;**

opADD**:** stage0 **<=** T7**;**

opSUB**:** stage0 **<=** T7**;**

opOR**:** stage0 **<=** T7**;**

opAND**:** stage0 **<=** T7**;**

opCOMP**:** stage0 **<=** T7**;**

opMULDIV**:** stage0 **<=** T7**;**

opSHFT**:** stage0 **<=** T7**;**

opLOAD**:** stage0 **<=** T7**;**

opSTOR**:** stage0 **<=** T7**;**

opLDA**:** stage0 **<=** T7**;**

opSTA**:** stage0 **<=** T7**;**

opLDB**:** stage0 **<=** T7**;**

opSTB**:** stage0 **<=** T7**;**

opINPUT**:** stage0 **<=** T7**;**

opOUTPUT**:** stage0 **<=** T7**;**

opNOP**:** stage0 **<=** T7**;**

**default:** **begin**

stage0 **<=** T6**;**

invalid\_opcode **<=** 1'b1**;**

**end**

**endcase**

T6**:** stage0 **<=** T1**;**

T7**:** **begin**

**if(**stg1\_state**==**1'b1**)** **begin** //Stage1 Handshake

stage0 **<=** T6**;** //Restart Fetch Cycle

**end** **else** **begin** stage0 **<=** T7**;** **end** //Wait for Stage1 Handshake

**if(**ccr\_v**==**1'b1**)** **begin** v\_state **<=** 1'b1**;** **end**

**end**

T8**:** **begin**

//stg0\_state <= 1'b1; //Start Stage1

**if(**stg1\_state**==**1'b1**)** **begin** //Continue Branch

**if(**instr**[**2**:**0**]==**BEQ**)** **begin** stage0 **<=** T9**;** **end**

**else** **if** **(**instr**[**2**:**0**]==**BNE**)** **begin** stage0 **<=** T11**;** **end**

**else** **begin** stage0 **<=** T6**;** **end**

**end** **else** **begin**

stage0 **<=** T8**;** //Wait for stage1 Handshake

**end**

**end**

T9**:** **if(**bra\_loop**==**3'b001**)** **begin**

**if(**ccr\_z**==**1'b1**)** **begin** stage0 **<=** T10**;** **end** //Branch

**else** **begin** stage0 **<=** T6**;** **end**

bra\_loop **<=** 3'b000**;**

**end** **else** **begin**

**if(**ccr\_z**==**1'b1**)** **begin** stage0 **<=** T10**;** **end** //Branch

**else** **begin** stage0 **<=** T9**;** **end**

bra\_loop **<=** **(**bra\_loop **+** 1**);**

**end**

T10**:** stage0 **<=** T1**;**

T11**:if(**bra\_loop**==**3'b001**)** **begin**

**if(**ccr\_z**==**1'b0**)** **begin** stage0 **<=** T10**;** **end** //Branch

**else** **begin** stage0 **<=** T6**;** **end**

bra\_loop **<=** 3'b000**;**

**end** **else** **begin**

**if(**ccr\_z**==**1'b1**)** **begin** stage0 **<=** T6**;** **end** //Branch

**else** **begin** stage0 **<=** T11**;** **end**

bra\_loop **<=** **(**bra\_loop **+** 1**);**

**end**

T12**:** stage0 **<=** T10**;**

T13**:** **if(**instr**[**7**:**3**]==**RTI**)** **begin**

itr\_state **<=** 1'b0**;**

v\_state **<=** 1'b0**;**

invalid\_opcode **<=** 1'b0**;**

stage0 **<=** T15**;**

**end** **else** **begin**

stage0 **<=** T15**;**

**end**

T14**:** **begin**

stage0 **<=** T6**;**

**if(**instr**[**7**:**3**]==**LMSK**)** **begin** itr\_mask **<=** data\_in**[**3**:**0**];** **end**

**end**

T15**:** stage0 **<=** T7**;**

**default:** stage0 **<=** T6**;**

**endcase**

**end**

**end**

**always** **@** **(**stage0**)** **begin**

**case(**stage0**)**

T0**:** ctrl **<=** CP0**;**

T1**:** ctrl **<=** CP1**;**

T2**:** ctrl **<=** CP2**;**

T3**:** ctrl **<=** CP3**;**

T4**:** ctrl **<=** CP4**;**

T5**:** ctrl **<=** CP5**;**

T6**:** **begin**

ctrl **<=** CP6**;**

stg0\_state **<=** 1'b0**;**

**end**

T7**:** **begin**

ctrl **<=** CP7**;**

stg0\_state **<=** 1'b1**;** //Stage0 Finished

**end**

T8**:** **begin**

ctrl **<=** CP8**;**

stg0\_state **<=** 1'b1**;** //Stage0 Finished

**end**

T9**:** **begin**

ctrl **<=** CP9**;**

stg0\_state **<=** 1'b0**;**

**end**

T10**:** ctrl **<=** CP10**;**

T11**:** **begin**

ctrl **<=** CP11**;**

stg0\_state **<=** 1'b0**;**

**end**

T12**:** ctrl **<=** CP12**;**

T13**:** ctrl **<=** CP13**;**

T14**:** ctrl **<=** CP14**;**

T15**:** ctrl **<=** CP15**;**

**default:** ctrl **<=** CP1**;**

**endcase**

**end**

**endmodule**

## stage1.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Controller Unit 1

//

// Moore Model Finite State Machine (FSM) implements control of stage 1 of the

// accumulator processor.

//

//////////////////////////////////////////////////////////////////////////////////

**module** stage1**(**clk**,** clr**,** instr**,** ir\_data**,** mdr\_data**,** stg0\_state**,** input\_rdy**,** out\_recv**,**

out\_dev\_rdy**,** cache\_hit**,** stg1\_state**,** ctrl**,** num\_shift**,** input\_recv**,** stage1**,**

output\_data**,** stg1\_instr**,** ch\_miss\_loop**);**

//Inputs

**input** clk**,** clr**;**

**input** **[**7**:**0**]** ir\_data**;** //Contents of IR1\_0 - Data Register

**input** **[**7**:**0**]** mdr\_data**;** //Contents of IR1\_0 - Data Register

**input** **[**7**:**0**]** instr**;** //Contents of IR0\_0 - Instruction Register

**input** stg0\_state**;** //Handshake control line - Stage 1 interface

**input** cache\_hit**;** //Hit signal from the cache

**input** input\_rdy**;** //Handhsake control line - Input device

**input** out\_dev\_rdy**;** //Handshake control line - Output Device Ready

**input** out\_recv**;** //Handshake Control Line - Out Dev Received Data

//Outputs

**output** **reg** stg1\_state**;** //Handshake control line - Stage 0 status

**output** **reg** **[**35**:**0**]** ctrl**;** //21 bit control line - control and sel points

**output** **reg** **[**2**:**0**]** num\_shift**;** //Control Shifter - Number to shift by

**output** **reg** input\_recv**;** //Handhsake Control Line - Input Received

**output** **reg** **[**7**:**0**]** output\_data**;** //Control Output data bus

**output** **reg** **[**71**:**0**]** stage1**;** //Current Controller state

//INPUT/OUTPUT Handshake registers

**reg** rdy\_recv**;** //Ready to Receive Flag

**reg** rdy\_out**;** //Ready to OUTPUT Flag

//Stage1 Pipeline Ready

**reg** stg1\_rdy**;**

//Cache Miss Loop

**output** **reg** **[**4**:**0**]** ch\_miss\_loop**;**

**reg** ch\_hit\_loop**;**

//Stage 1 Instruciton IN - Output

**output** **[**7**:**0**]** stg1\_instr**;**

**wire** **[**7**:**0**]** stg1\_instr\_w**;**

**assign** stg1\_instr\_w **=** instr**;**

**assign** stg1\_instr **=** stg1\_instr\_w**;**

//Define Stage 1 state encoding

**parameter** T0 **=** 72'b000000000000000000000000000000000000000000000000000000000000000000000001**;**

**parameter** T1 **=** 72'b000000000000000000000000000000000000000000000000000000000000000000000010**;**

**parameter** T2 **=** 72'b000000000000000000000000000000000000000000000000000000000000000000000100**;**

**parameter** T3 **=** 72'b000000000000000000000000000000000000000000000000000000000000000000001000**;**

**parameter** T4 **=** 72'b000000000000000000000000000000000000000000000000000000000000000000010000**;**

**parameter** T5 **=** 72'b000000000000000000000000000000000000000000000000000000000000000000100000**;**

**parameter** T6 **=** 72'b000000000000000000000000000000000000000000000000000000000000000001000000**;**

**parameter** T7 **=** 72'b000000000000000000000000000000000000000000000000000000000000000010000000**;**

**parameter** T8 **=** 72'b000000000000000000000000000000000000000000000000000000000000000100000000**;**

**parameter** T9 **=** 72'b000000000000000000000000000000000000000000000000000000000000001000000000**;**

**parameter** T10 **=** 72'b000000000000000000000000000000000000000000000000000000000000010000000000**;**

**parameter** T11 **=** 72'b000000000000000000000000000000000000000000000000000000000000100000000000**;**

**parameter** T12 **=** 72'b000000000000000000000000000000000000000000000000000000000001000000000000**;**

**parameter** T13 **=** 72'b000000000000000000000000000000000000000000000000000000000010000000000000**;**

**parameter** T14 **=** 72'b000000000000000000000000000000000000000000000000000000000100000000000000**;**

**parameter** T15 **=** 72'b000000000000000000000000000000000000000000000000000000001000000000000000**;**

**parameter** T16 **=** 72'b000000000000000000000000000000000000000000000000000000010000000000000000**;**

**parameter** T17 **=** 72'b000000000000000000000000000000000000000000000000000000100000000000000000**;**

**parameter** T18 **=** 72'b000000000000000000000000000000000000000000000000000001000000000000000000**;**

**parameter** T19 **=** 72'b000000000000000000000000000000000000000000000000000010000000000000000000**;**

**parameter** T20 **=** 72'b000000000000000000000000000000000000000000000000000100000000000000000000**;**

**parameter** T21 **=** 72'b000000000000000000000000000000000000000000000000001000000000000000000000**;**

**parameter** T22 **=** 72'b000000000000000000000000000000000000000000000000010000000000000000000000**;**

**parameter** T23 **=** 72'b000000000000000000000000000000000000000000000000100000000000000000000000**;**

**parameter** T24 **=** 72'b000000000000000000000000000000000000000000000001000000000000000000000000**;**

**parameter** T25 **=** 72'b000000000000000000000000000000000000000000000010000000000000000000000000**;**

**parameter** T26 **=** 72'b000000000000000000000000000000000000000000000100000000000000000000000000**;**

**parameter** T27 **=** 72'b000000000000000000000000000000000000000000001000000000000000000000000000**;**

**parameter** T28 **=** 72'b000000000000000000000000000000000000000000010000000000000000000000000000**;**

**parameter** T29 **=** 72'b000000000000000000000000000000000000000000100000000000000000000000000000**;**

**parameter** T30 **=** 72'b000000000000000000000000000000000000000001000000000000000000000000000000**;**

**parameter** T31 **=** 72'b000000000000000000000000000000000000000010000000000000000000000000000000**;**

**parameter** T32 **=** 72'b000000000000000000000000000000000000000100000000000000000000000000000000**;**

**parameter** T33 **=** 72'b000000000000000000000000000000000000001000000000000000000000000000000000**;**

**parameter** T34 **=** 72'b000000000000000000000000000000000000010000000000000000000000000000000000**;**

**parameter** T35 **=** 72'b000000000000000000000000000000000000100000000000000000000000000000000000**;**

**parameter** T36 **=** 72'b000000000000000000000000000000000001000000000000000000000000000000000000**;**

**parameter** T37 **=** 72'b000000000000000000000000000000000010000000000000000000000000000000000000**;**

**parameter** T38 **=** 72'b000000000000000000000000000000000100000000000000000000000000000000000000**;**

**parameter** T39 **=** 72'b000000000000000000000000000000001000000000000000000000000000000000000000**;**

**parameter** T40 **=** 72'b000000000000000000000000000000010000000000000000000000000000000000000000**;**

**parameter** T41 **=** 72'b000000000000000000000000000000100000000000000000000000000000000000000000**;**

**parameter** T42 **=** 72'b000000000000000000000000000001000000000000000000000000000000000000000000**;**

**parameter** T43 **=** 72'b000000000000000000000000000010000000000000000000000000000000000000000000**;**

**parameter** T44 **=** 72'b000000000000000000000000000100000000000000000000000000000000000000000000**;**

**parameter** T45 **=** 72'b000000000000000000000000001000000000000000000000000000000000000000000000**;**

**parameter** T46 **=** 72'b000000000000000000000000010000000000000000000000000000000000000000000000**;**

**parameter** T47 **=** 72'b000000000000000000000000100000000000000000000000000000000000000000000000**;**

**parameter** T48 **=** 72'b000000000000000000000001000000000000000000000000000000000000000000000000**;**

**parameter** T49 **=** 72'b000000000000000000000010000000000000000000000000000000000000000000000000**;**

**parameter** T50 **=** 72'b000000000000000000000100000000000000000000000000000000000000000000000000**;**

**parameter** T51 **=** 72'b000000000000000000001000000000000000000000000000000000000000000000000000**;**

**parameter** T52 **=** 72'b000000000000000000010000000000000000000000000000000000000000000000000000**;**

**parameter** T53 **=** 72'b000000000000000000100000000000000000000000000000000000000000000000000000**;**

**parameter** T54 **=** 72'b000000000000000001000000000000000000000000000000000000000000000000000000**;**

**parameter** T55 **=** 72'b000000000000000010000000000000000000000000000000000000000000000000000000**;**

**parameter** T56 **=** 72'b000000000000000100000000000000000000000000000000000000000000000000000000**;**

**parameter** T57 **=** 72'b000000000000001000000000000000000000000000000000000000000000000000000000**;**

**parameter** T58 **=** 72'b000000000000010000000000000000000000000000000000000000000000000000000000**;**

**parameter** T59 **=** 72'b000000000000100000000000000000000000000000000000000000000000000000000000**;**

**parameter** T60 **=** 72'b000000000001000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T61 **=** 72'b000000000010000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T62 **=** 72'b000000000100000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T63 **=** 72'b000000001000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T64 **=** 72'b000000010000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T65 **=** 72'b000000100000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T66 **=** 72'b000001000000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T67 **=** 72'b000010000000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T68 **=** 72'b000100000000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T69 **=** 72'b001000000000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T70 **=** 72'b010000000000000000000000000000000000000000000000000000000000000000000000**;**

**parameter** T71 **=** 72'b100000000000000000000000000000000000000000000000000000000000000000000000**;**

//Define Stage 1 control points

**parameter** CP0**=**36'b100000000000000111100011110110000001**;**

**parameter** CP1**=**36'b100000000000000101010011110110000001**;**

**parameter** CP2**=**36'b100000000000100101000011110110000001**;**

**parameter** CP3**=**36'b100000000000100101001011110110000001**;**

**parameter** CP4**=**36'b100000000000000111100011110110000001**;**

**parameter** CP5**=**36'b100000000000000101010011110110000001**;**

**parameter** CP6**=**36'b100000000000100101000011110110000001**;**

**parameter** CP7**=**36'b100000000000000101001011110110000001**;**

**parameter** CP8**=**36'b100000000000000101010011110010000001**;**

**parameter** CP9**=**36'b100000000000000111100011110110000001**;**

**parameter** CP10**=**36'b101000000000000101000011010110000001**;**

**parameter** CP11**=**36'b101000000000000101000011011110000001**;**

**parameter** CP12**=**36'b101001100000000101000011010110000001**;**

**parameter** CP13**=**36'b101001100000000101000011011110000001**;**

**parameter** CP14**=**36'b101010000000000101000011010110000001**;**

**parameter** CP15**=**36'b101010000000000101000011011110000001**;**

**parameter** CP16**=**36'b101100000000000101000011010110000001**;**

**parameter** CP17**=**36'b101100000000000101000011011110000001**;**

**parameter** CP18**=**36'b101110000000000101000011010110000001**;**

**parameter** CP19**=**36'b100000000000000101000011100110001001**;**

**parameter** CP20**=**36'b101000000000000101000000100110000001**;**

**parameter** CP21**=**36'b100000000101000101000011100110000001**;**

**parameter** CP22**=**36'b101000000000000101000000100110000001**;**

**parameter** CP23**=**36'b101000000000000101000011000110000001**;**

**parameter** CP24**=**36'b101000000000000101000000100110000001**;**

**parameter** CP25**=**36'b100000000110000101000011100110000001**;**

**parameter** CP26**=**36'b101000000000000101000000100110000001**;**

**parameter** CP27**=**36'b101000000000000101000011000110000001**;**

**parameter** CP28**=**36'b101000000000000101000000100110000001**;**

**parameter** CP29**=**36'b101000000000000101000000100110000001**;**

**parameter** CP30**=**36'b101000000000000101000000100110000001**;**

**parameter** CP31**=**36'b101000000000000101000000100110000001**;**

**parameter** CP32**=**36'b101000000000000101000001100110000001**;**

**parameter** CP33**=**36'b101000000000000101000010100110000001**;**

**parameter** CP34**=**36'b100000000000110101001011100101100001**;**

**parameter** CP35**=**36'b100000000000110101000011100110000001**;**

**parameter** CP36**=**36'b110000010000000101000011100110000001**;**

**parameter** CP37**=**36'b110000000000000101000011100110000001**;**

**parameter** CP38**=**36'b100000000000110101001011100101000001**;**

**parameter** CP39**=**36'b100000000110000101000011100110000001**;**

**parameter** CP40**=**36'b100000000100000101000011100110000001**;**

**parameter** CP41**=**36'b100000000000110101001011100100100001**;**

**parameter** CP42**=**36'b100000000000000101000011100110000001**;**

**parameter** CP43**=**36'b100000000000000101000011100110000001**;**

**parameter** CP44**=**36'b100000000000000101001011100100000001**;**

**parameter** CP45**=**36'b100000000000000101000011100110000001**;**

**parameter** CP46**=**36'b100000000000000101000011100110000001**;**

**parameter** CP47**=**36'b100000000000000101000011100110000001**;**

**parameter** CP48**=**36'b100000000000000101000011100110000001**;**

**parameter** CP49**=**36'b100000000000000101000011100110000001**;**

**parameter** CP50**=**36'b100000000000000101000011100110000001**;**

**parameter** CP51**=**36'b100000000000000111100011100110000001**;**

**parameter** CP52**=**36'b101001100000000101000011001110000001**;**

**parameter** CP53**=**36'b101000000000000101000100100110000001**;**

**parameter** CP54**=**36'b100000000000000101000011100110001001**;**

**parameter** CP55**=**36'b100000000000000111000011100110000001**;**

**parameter** CP56**=**36'b100000000000000111000011100110000001**;**

**parameter** CP57**=**36'b100000000000000101000000100110010001**;**

**parameter** CP58**=**36'b101000000000000101000000100110010101**;**

**parameter** CP59**=**36'b101000000000000101000000100110011001**;**

**parameter** CP60**=**36'b101000000000000101000000100110011011**;**

**parameter** CP61**=**36'b100000000000000101000000100110010001**;**

**parameter** CP62**=**36'b100000000000000101000000100110010001**;**

**parameter** CP63**=**36'b100000000000000101000000100110011001**;**

**parameter** CP64**=**36'b100000000000000101000000100110011001**;**

**parameter** CP65**=**36'b100000000000110101000011100101100001**;**

**parameter** CP66**=**36'b100000000000100101000011100001100001**;**

**parameter** CP67**=**36'b100000000000110101000011100001100001**;**

**parameter** CP68**=**36'b100000000000100101000011100001100001**;**

**parameter** CP69**=**36'b100000000000100101000011100001100001**;**

**parameter** CP70**=**36'b100000000000100101000011100001100001**;**

**parameter** CP71**=**36'b100000000000110101000011100110000001**;**

//Parameterize Instruction OPcodes

**parameter** opADD **=** 5'b00000**;**

**parameter** opSUB **=** 5'b00001**;**

**parameter** opOR **=** 5'b00011**;**

**parameter** opAND **=** 5'b00100**;**

**parameter** opCOMP **=** 5'b10000**;**

**parameter** opMULDIV **=** 5'b00010**;**

**parameter** opSHFT **=** 5'b00101**;**

**parameter** opBRA **=** 5'b00110**;**

**parameter** opRTS **=** 5'b01000**;**

**parameter** opRTI **=** 5'b01001**;**

**parameter** opLOAD **=** 5'b01010**;**

**parameter** opSTOR **=** 5'b01011**;**

**parameter** opLDA **=** 5'b10001**;**

**parameter** opSTA **=** 5'b10010**;**

**parameter** opLDB **=** 5'b10011**;**

**parameter** opSTB **=** 5'b10100**;**

**parameter** opINPUT **=** 5'b01100**;**

**parameter** opOUTPUT **=** 5'b01101**;**

**parameter** opLMSK **=** 5'b01110**;**

**parameter** opNOP **=** 5'b01111**;**

//Parameterize Instruction Flags

**parameter** flDIR **=** 3'b000**;** //Direct

**parameter** flIND **=** 3'b001**;** //Indirect

**parameter** flIMM **=** 3'b010**;** //Immediate

**parameter** flMUL\_DIR **=** 3'b000**;** //Multiply Direct

**parameter** flMUL\_IND **=** 3'b001**;** //Multiply Indirect

**parameter** flDIV\_DIR **=** 3'b010**;** //Multiply Direct

**parameter** flDIV\_IND **=** 3'b011**;** //Multiply Indirect

**parameter** flMUL **=** 1'b0**;** //MULDIV Multiply

**parameter** flDIV **=** 1'b1**;** //MULDIV Division

**parameter** flLS0 **=** 3'b000**;** //Left Shift 0

**parameter** flLS1 **=** 3'b001**;** //Left Shift 1

**parameter** flRS0 **=** 3'b010**;** //Right Shift 0

**parameter** flRS1 **=** 3'b011**;** //Right Shift 1

**initial** **begin**

rdy\_recv **<=** 1'b1**;**

rdy\_out **<=** 1'b1**;**

stg1\_rdy **<=** 1'b0**;**

stg1\_state **<=** 1'b0**;**

ch\_miss\_loop **<=** 5'b00000**;**

ch\_hit\_loop **<=** 1'b0**;**

**end**

**always** **@** **(posedge** clk**)** **begin**

**if(**clr**==**1'b0**)** **begin**

stage1 **<=** T55**;**

**end**

**else** **begin**

**case(**stage1**)**

T0**:** **if(**instr**[**7**:**3**]==**opSHFT**)** **begin** stage1 **<=** T54**;** **end**

**else** **begin** stage1 **<=** T1**;** **end**

T1**:** **case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T65**;**

opSTA**:** stage1 **<=** T65**;**

opSTB**:** stage1 **<=** T65**;**

opINPUT**:** stage1 **<=** T65**;**

**default:** stage1 **<=** T68**;**

**endcase**

T2**:if(**ch\_hit\_loop**==**1'b1**)** **begin**

**if(**cache\_hit**==**1'b1**)** **begin** //Handle cache hit

**case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T55**;**

opSTA**:** stage1 **<=** T55**;**

opSTB**:** stage1 **<=** T55**;**

opINPUT**:** stage1 **<=** T55**;**

**default:** stage1 **<=** T3**;**

**endcase**

ch\_hit\_loop **<=** 1'b0**;**

ch\_miss\_loop **<=** 5'b00000**;**

**end** **else** **begin** //HANDLE MISS

**if(**ch\_miss\_loop**==**5'b01011**)** **begin**

**case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T55**;**

opSTA**:** stage1 **<=** T55**;**

opSTB**:** stage1 **<=** T55**;**

opINPUT**:** stage1 **<=** T55**;**

**default:** stage1 **<=** T3**;**

**endcase**

ch\_miss\_loop **<=** 5'b00000**;**

ch\_hit\_loop **<=** 1'b0**;**

**end**

**else** **begin**

ch\_miss\_loop **<=** **(**ch\_miss\_loop **+** 1**);**

stage1 **<=** T2**;**

**end**

**end**

**end** **else** **begin**

ch\_hit\_loop **<=** **(**ch\_hit\_loop **+** 1**);**

stage1 **<=** T2**;**

**end**

T3**:** **case(**instr**[**7**:**3**])**

opADD**:** stage1 **<=** T10**;**

opSUB**:** stage1 **<=** T12**;**

opOR**:** stage1 **<=** T14**;**

opAND**:** stage1 **<=** T16**;**

opMULDIV**:** stage1 **<=** T54**;**

opLOAD**:** stage1 **<=** T32**;**

opLDA**:** stage1 **<=** T36**;**

opLDB**:** stage1 **<=** T39**;**

opOUTPUT**:** stage1 **<=** T48**;**

**endcase**

T4**:** stage1 **<=** T5**;**

T5**:** **case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T66**;**

opSTA**:** stage1 **<=** T66**;**

opSTB**:** stage1 **<=** T66**;**

opINPUT**:** stage1 **<=** T66**;**

**default:** stage1 **<=** T69**;**

**endcase**

T6**:** **if(**ch\_hit\_loop**==**1'b1**)**

**begin**

**if(**cache\_hit**==**1'b1**)** **begin** //Handle cache hit

stage1 **<=** T7**;**

ch\_hit\_loop **<=** 1'b0**;**

ch\_miss\_loop **<=** 5'b00000**;**

**end**

**else** **begin** //HANDLE MISS

**if(**ch\_miss\_loop**==**5'b01011**)** **begin**

ch\_miss\_loop **<=** 5'b00000**;**

ch\_hit\_loop **<=** 1'b0**;**

stage1 **<=** T7**;**

**end**

**else** **begin**

ch\_miss\_loop **<=** **(**ch\_miss\_loop **+** 1**);**

stage1 **<=** T6**;**

**end**

**end**

**end**

**else** **begin**

ch\_hit\_loop **<=** **(**ch\_hit\_loop **+** 1**);**

stage1 **<=** T6**;**

**end**

T7**:** stage1 **<=** T8**;**

T8**:** **case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T67**;**

opSTA**:** stage1 **<=** T67**;**

opSTB**:** stage1 **<=** T67**;**

opINPUT**:** stage1 **<=** T67**;**

**default:** stage1 **<=** T70**;**

**endcase**

T9**:** **case(**instr**[**7**:**3**])**

opADD**:** stage1 **<=** T11**;**

opSUB**:** stage1 **<=** T13**;**

opOR**:** stage1 **<=** T15**;**

opAND**:** stage1 **<=** T17**;**

opLOAD**:** stage1 **<=** T33**;**

opLDA**:** stage1 **<=** T37**;**

opLDB**:** stage1 **<=** T40**;**

**endcase**

T10**:** stage1 **<=** T55**;**

T11**:** stage1 **<=** T55**;**

T12**:** stage1 **<=** T55**;**

T13**:** stage1 **<=** T55**;**

T14**:** stage1 **<=** T55**;**

T15**:** stage1 **<=** T55**;**

T16**:** stage1 **<=** T55**;**

T17**:** stage1 **<=** T55**;**

T18**:** stage1 **<=** T55**;**

T19**:** **case(**instr**[**1**])**

flMUL**:** **case(**mdr\_data**[**0**])**

0**:** stage1 **<=** T61**;** //Even Parity

1**:** stage1 **<=** T21**;** //Odd Parity

**endcase**

flDIV**:** **case(**mdr\_data**[**0**])**

0**:** stage1 **<=** T63**;** //Even Parity

1**:** stage1 **<=** T25**;** //Odd Parity

**endcase**

**endcase**

T20**:** stage1 **<=** T55**;**

T21**:** stage1 **<=** T62**;**

T22**:** stage1 **<=** T23**;**

T23**:** stage1 **<=** T55**;**

T24**:** stage1 **<=** T55**;**

T25**:** stage1 **<=** T64**;**

T26**:** stage1 **<=** T27**;**

T27**:** stage1 **<=** T55**;**

T28**:** stage1 **<=** T55**;**

T29**:** stage1 **<=** T55**;**

T30**:** stage1 **<=** T55**;**

T31**:** stage1 **<=** T55**;**

T32**:** stage1 **<=** T55**;**

T33**:** stage1 **<=** T55**;**

T34**:** stage1 **<=** T35**;**

T35**:** **begin**

**if(**instr**[**7**:**3**]==**opINPUT**)** **begin** input\_recv **<=** 1'b1**;** **end**

stage1 **<=** T71**;**

**end**

T36**:** stage1 **<=** T55**;**

T37**:** stage1 **<=** T55**;**

T38**:** stage1 **<=** T35**;**

T39**:** stage1 **<=** T55**;**

T40**:** stage1 **<=** T55**;**

T41**:** stage1 **<=** T35**;**

T42**:** **if(**rdy\_recv**==**1'b1**)** **begin**

stage1 **<=** T43**;** **end**

**else** **begin** stage1 **<=** T42**;** **end**

T43**:** **if(**input\_rdy**==**1'b1**)** **begin**

**case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

**endcase** **end**

**else** **begin** stage1 **<=** T43**;** **end**

T44**:** stage1 **<=** T35**;**

T45**:** **if(**input\_recv **==** 1'b1**)** **begin**

stage1 **<=** T55**;**

input\_recv **<=** 1'b0**;**

**end**

**else** **begin** stage1 **<=** T44**;** **end**

T46**:** **if(**rdy\_out**==**1'b1**)** **begin** stage1 **<=** T47**;** **end**

**else** **begin** stage1 **<=** T46**;** **end**

T47**:** **if(**out\_dev\_rdy**==**1'b1**)** **begin** stage1 **<=** T4**;** **end**

**else** **begin** stage1 **<=** T47**;** **end**

T48**:** stage1 **<=** T49**;**

T49**:** **if(**out\_recv**==**1'b1**)** **begin** stage1 **<=** T55**;** **end**

**else** **begin** stage1 **<=** T48**;** **end**

T50**:** stage1 **<=** T55**;**

T51**:** stage1 **<=** T52**;**

T52**:** stage1 **<=** T55**;**

T53**:** stage1 **<=** T55**;**

T54**:** **case(**instr**[**7**:**3**])**

opSHFT**:** **case(**instr**[**2**:**0**])**

flLS0**:** stage1 **<=** T57**;**

flLS1**:** stage1 **<=** T58**;**

flRS0**:** stage1 **<=** T59**;**

flRS1**:** stage1 **<=** T60**;**

**endcase**

opMULDIV**:** stage1 **<=** T19**;**

**endcase**

T55**:** **if(**stg0\_state**==**1'b1**)** **begin**

stage1 **<=** T56**;**

**end**

**else** stage1 **<=** T55**;**

T56**:** **if(**stg0\_state**==**1'b1**)** **begin** //Digest OPcode

**case(**instr**[**7**:**3**])**

opADD**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opSUB**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opOR**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opAND**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opCOMP**:** stage1 **<=** T18**;**

opMULDIV**:** **case(**instr**[**2**:**0**])**

flMUL\_DIR**:** stage1 **<=** T0**;**

flMUL\_IND**:** stage1 **<=** T4**;**

flDIV\_DIR**:** stage1 **<=** T0**;**

flDIV\_IND**:** stage1 **<=** T4**;**

**endcase**

opSHFT**:** stage1 **<=** T0**;**

opBRA**:** stage1 **<=** T51**;**

opRTS**:** stage1 **<=** T53**;**

opRTI**:** stage1 **<=** T53**;**

opLOAD**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opSTOR**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

**endcase**

opLDA**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opSTA**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

**endcase**

opLDB**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

flIMM**:** stage1 **<=** T9**;**

**endcase**

opSTB**:** **case(**instr**[**2**:**0**])**

flDIR**:** stage1 **<=** T0**;**

flIND**:** stage1 **<=** T4**;**

**endcase**

opINPUT**:** stage1 **<=** T42**;**

opOUTPUT**:** stage1 **<=** T46**;**

opNOP**:** stage1 **<=** T50**;**

**default:** stage1 **<=** T55**;**

**endcase**

**end**

**else** **begin** stage1 **<=** T56**;** **end** //Bubble pipeline

T57**:** stage1 **<=** T28**;**

T58**:** stage1 **<=** T29**;**

T59**:** stage1 **<=** T30**;**

T60**:** stage1 **<=** T31**;**

T61**:** stage1 **<=** T20**;**

T62**:** stage1 **<=** T22**;**

T63**:** stage1 **<=** T24**;**

T64**:** stage1 **<=** T26**;**

T65**:** **case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T34**;**

opSTA**:** stage1 **<=** T38**;**

opSTB**:** stage1 **<=** T41**;**

opINPUT**:** stage1 **<=** T44**;**

**default:** stage1 **<=** T2**;**

**endcase**

T66**:** stage1 **<=** T6**;**

T67**:** **case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T34**;**

opSTA**:** stage1 **<=** T38**;**

opSTB**:** stage1 **<=** T41**;**

opINPUT**:** stage1 **<=** T44**;**

**default:** stage1 **<=** T2**;**

**endcase**

T68**:** stage1 **<=** T2**;**

T69**:** stage1 **<=** T6**;**

T70**:** stage1 **<=** T2**;**

T71**:** **if(**ch\_hit\_loop**==**1'b1**)** **begin**

**if(**cache\_hit**==**1'b1**)** **begin** //Handle cache hit

**case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T55**;**

opSTA**:** stage1 **<=** T55**;**

opSTB**:** stage1 **<=** T55**;**

opINPUT**:** stage1 **<=** T55**;**

**default:** stage1 **<=** T3**;**

**endcase**

ch\_hit\_loop **<=** 1'b0**;**

ch\_miss\_loop **<=** 5'b00000**;**

**end** **else** **begin** //HANDLE MISS

**if(**ch\_miss\_loop**==**5'b01011**)** **begin**

**case(**instr**[**7**:**3**])**

opSTOR**:** stage1 **<=** T55**;**

opSTA**:** stage1 **<=** T55**;**

opSTB**:** stage1 **<=** T55**;**

opINPUT**:** stage1 **<=** T55**;**

**default:** stage1 **<=** T3**;**

**endcase**

ch\_miss\_loop **<=** 5'b00000**;**

ch\_hit\_loop **<=** 1'b0**;**

**end**

**else** **begin**

ch\_miss\_loop **<=** **(**ch\_miss\_loop **+** 1**);**

stage1 **<=** T71**;**

**end**

**end**

**end** **else** **begin**

ch\_hit\_loop **<=** **(**ch\_hit\_loop **+** 1**);**

stage1 **<=** T71**;**

**end**

**default:** stage1 **<=** T55**;**

**endcase**

**end**

**end**

**always** **@** **(**stage1**)** **begin**

**case(**stage1**)**

T0**:** **begin**

ctrl **<=** CP0**;**

stg1\_state **<=** 1'b0**;**

rdy\_recv **<=** 1'b1**;**

rdy\_out **<=** 1'b1**;**

**end**

T1**:** ctrl **<=** CP1**;**

T2**:** ctrl **<=** CP2**;**

T3**:** ctrl **<=** CP3**;**

T4**:** **begin**

ctrl **<=** CP4**;**

stg1\_state **<=** 1'b0**;**

**end**

T5**:** ctrl **<=** CP5**;**

T6**:** ctrl **<=** CP6**;**

T7**:** ctrl **<=** CP7**;**

T8**:** ctrl **<=** CP8**;**

T9**:** **begin**

ctrl **<=** CP9**;**

stg1\_state **<=** 1'b0**;**

**end**

T10**:** ctrl **<=** CP10**;**

T11**:** ctrl **<=** CP11**;**

T12**:** ctrl **<=** CP12**;**

T13**:** ctrl **<=** CP13**;**

T14**:** ctrl **<=** CP14**;**

T15**:** ctrl **<=** CP15**;**

T16**:** ctrl **<=** CP16**;**

T17**:** ctrl **<=** CP17**;**

T18**:** **begin**

ctrl **<=** CP18**;**

stg1\_state **<=** 1'b0**;**

**end**

T19**:** ctrl **<=** CP19**;**

T20**:** ctrl **<=** CP20**;**

T21**:** ctrl **<=** CP21**;**

T22**:** ctrl **<=** CP22**;**

T23**:** ctrl **<=** CP23**;**

T24**:** ctrl **<=** CP24**;**

T25**:** ctrl **<=** CP25**;**

T26**:** ctrl **<=** CP26**;**

T27**:** ctrl **<=** CP27**;**

T28**:** ctrl **<=** CP28**;**

T29**:** ctrl **<=** CP29**;**

T30**:** ctrl **<=** CP30**;**

T31**:** ctrl **<=** CP31**;**

T32**:** ctrl **<=** CP32**;**

T33**:** ctrl **<=** CP33**;**

T34**:** ctrl **<=** CP34**;**

T35**:** ctrl **<=** CP35**;**

T36**:** ctrl **<=** CP36**;**

T37**:** ctrl **<=** CP37**;**

T38**:** ctrl **<=** CP38**;**

T39**:** ctrl **<=** CP39**;**

T40**:** ctrl **<=** CP40**;**

T41**:** ctrl **<=** CP41**;**

T42**:** **begin**

ctrl **<=** CP42**;**

stg1\_state **<=** 1'b0**;**

**end**

T43**:** ctrl **<=** CP43**;**

T44**:** ctrl **<=** CP44**;**

T45**:** ctrl **<=** CP45**;**

T46**:** **begin**

ctrl **<=** CP46**;**

stg1\_state **<=** 1'b0**;**

**end**

T47**:** ctrl **<=** CP47**;**

T48**:** **begin**

ctrl **<=** CP48**;**

output\_data **<=** mdr\_data**;**

**end**

T49**:** ctrl **<=** CP49**;**

T50**:** **begin**

ctrl **<=** CP50**;**

stg1\_state **<=** 1'b0**;**

**end**

T51**:** **begin**

ctrl **<=** CP51**;**

stg1\_state **<=** 1'b0**;**

**end**

T52**:** ctrl **<=** CP52**;**

T53**:** **begin**

ctrl **<=** CP53**;**

stg1\_state **<=** 1'b0**;**

**end**

T54**:** ctrl **<=** CP54**;**

T55**:** ctrl **<=** CP55**;**

T56**:** **begin**

ctrl **<=** CP56**;**

stg1\_state **<=** 1'b1**;**

**end**

T57**:** **begin**

ctrl **<=** CP57**;**

num\_shift **<=** ir\_data**[**2**:**0**];**

**end**

T58**:** **begin**

ctrl **<=** CP58**;**

num\_shift **<=** ir\_data**[**2**:**0**];**

**end**

T59**:** **begin**

ctrl **<=** CP59**;**

num\_shift **<=** ir\_data**[**2**:**0**];**

**end**

T60**:** **begin**

ctrl **<=** CP60**;**

num\_shift **<=** ir\_data**[**2**:**0**];**

**end**

T61**:** **begin**

ctrl **<=** CP61**;**

num\_shift **<=** **(**mdr\_data**[**3**:**0**]** **>>** 1**);**

**end**

T62**:** **begin**

ctrl **<=** CP62**;**

num\_shift **<=** **(**mdr\_data**[**3**:**0**]** **>>** 1**);**

**end**

T63**:** **begin**

ctrl **<=** CP63**;**

num\_shift **<=** **((**mdr\_data**[**3**:**0**]** **>>** 1**)+**1**);**

**end**

T64**:** **begin**

ctrl **<=** CP64**;**

num\_shift **<=** **((**mdr\_data**[**3**:**0**]** **>>** 1**)+**1**);**

**end**

T65**:** ctrl **<=** CP65**;**

T66**:** ctrl **<=** CP66**;**

T67**:** ctrl **<=** CP67**;**

T68**:** ctrl **<=** CP68**;**

T69**:** ctrl **<=** CP69**;**

T70**:** ctrl **<=** CP70**;**

T71**:** ctrl **<=** CP71**;**

**default:** ctrl **<=** CP0**;**

**endcase**

**end**

**endmodule**

## Cache.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Cache : Fully Associative Cache - Behavioral Style (Parameterized)

// 4 Word Cache - Data: 8 bits wide, Address: 8 bits wide

// Replacement Implementation: Least Recently Used (LRU)

//

// Inputs: Addr, enab, clr, rw, data\_in

// Addr: Target memory address

// data\_in: input line for data, Write to target address

// enab: Chip enable line

// clr: Active low synchronous clear

// rw: Read/Write control line

//

// Outputs: data\_out, addr0, addr1, addr2, addr3, data0, data1, data2, data3, hit

// data\_out: Output data port, Read from target address

// addr0-3: Current contents of address registers within cache

// data0-3: Current contents of data registers within cache

// hit: Flags if the address was matched in the cache

//

//

// rw enab clr function

// x x 0 Clear all cache contents to zero \*Top Priority

// x 0 1 RAM Chip not enabled - Do not read or write

// 0 1 1 Read Target Address

// 1 1 1 Write

//

//////////////////////////////////////////////////////////////////////////////////

/\*module cache(clk,clr,enab,rw,Addr,data\_in,data\_out, hit\_out, addr0,

addr1, addr2, addr3, data0, data1, data2, data3, access0, access1, access2, access3,

ram0, ram1, ram2, ram3, ram4, ram5, ram6, ram7, state, curr\_LRU,

cache\_hit, target\_addr, target\_data, target\_rw\_out, c\_addrIN\_out, c\_dataIN\_out);\*/

**module** cache**(**clk**,**clr**,**enab**,**rw**,**Addr**,**data\_in**,**data\_out**,** hit\_out**,**

addr0**,** addr1**,** addr2**,** addr3**,** data0**,** data1**,** data2**,** data3**,**

ram0**,** ram1**,** ram2**,** ram3**,** ram4**,** ram5**,** ram6**,** ram7**,** ram8**,** ram9**,** ram10**,** ram11**,** ram12**,** ram13**,** ram14**,** ram15**,**

curr\_LRU**,** cache\_hit**,** target\_rw\_out**,** c\_dataIN\_out**,** state**,** ram\_data\_in\_monitor**,** ram\_addr\_in\_monitor**);**

//Specify address and data width

**parameter** d\_width **=** 8**;**

**parameter** a\_width **=** 8**;**

**parameter** n **=** 4**;** //Cache size

//Input Ports

**input** clk**,** clr**,** enab**,** rw**;**

**input** **[**a\_width**-**1**:**0**]** Addr**;**

**input** **[**d\_width**-**1**:**0**]** data\_in**;**

//Output Ports

**output** hit\_out**;**

**output** **reg** **[**d\_width**-**1**:**0**]** data\_out**;**

// output [a\_width:0] c\_addrIN\_out;

**output** **[**d\_width**:**0**]** c\_dataIN\_out**;**

**output** **[**a\_width**-**1**:**0**]** addr0**;**

**output** **[**a\_width**-**1**:**0**]** addr1**;**

**output** **[**a\_width**-**1**:**0**]** addr2**;**

**output** **[**a\_width**-**1**:**0**]** addr3**;**

**output** **[**d\_width**-**1**:**0**]** data0**;**

**output** **[**d\_width**-**1**:**0**]** data1**;**

**output** **[**d\_width**-**1**:**0**]** data2**;**

**output** **[**d\_width**-**1**:**0**]** data3**;**

/\*output [1:0] access0;

output [1:0] access1;

output [1:0] access2;

output [1:0] access3;\*/

//Output Ports For Monitoring RAM Contents

**output** **[**a\_width**-**1**:**0**]** ram0**;**

**output** **[**a\_width**-**1**:**0**]** ram1**;**

**output** **[**a\_width**-**1**:**0**]** ram2**;**

**output** **[**a\_width**-**1**:**0**]** ram3**;**

**output** **[**a\_width**-**1**:**0**]** ram4**;**

**output** **[**a\_width**-**1**:**0**]** ram5**;**

**output** **[**a\_width**-**1**:**0**]** ram6**;**

**output** **[**a\_width**-**1**:**0**]** ram7**;**

**output** **[**a\_width**-**1**:**0**]** ram8**;**

**output** **[**a\_width**-**1**:**0**]** ram9**;**

**output** **[**a\_width**-**1**:**0**]** ram10**;**

**output** **[**a\_width**-**1**:**0**]** ram11**;**

**output** **[**a\_width**-**1**:**0**]** ram12**;**

**output** **[**a\_width**-**1**:**0**]** ram13**;**

**output** **[**a\_width**-**1**:**0**]** ram14**;**

**output** **[**a\_width**-**1**:**0**]** ram15**;**

//Declare Cache Registers

**reg** **[**d\_width**-**1**:**0**]** cache\_data **[**n**-**1**:**0**];**

**reg** **[**a\_width**-**1**:**0**]** cache\_addr **[**n**-**1**:**0**];**

**reg** **[**1**:**0**]** cache\_access **[**n**-**1**:**0**];**

//Declare Cache Flag Registers

**output** **reg** **[**1**:**0**]** curr\_LRU**;** //Index of current least recently used address

**output** **reg** **[**1**:**0**]** cache\_hit**;** //Index of cache hit

**reg** **[**d\_width**-**1**:**0**]** target\_addr**;** //Target memory address to be saved on miss

**reg** **[**d\_width**-**1**:**0**]** target\_data**;** //Target data to be saved on a miss (write)

**reg** hit**;**

**wire** hit\_wire**;**

**assign** hit\_wire**=**hit**;**

**assign** hit\_out**=**hit\_wire**;**

**wire** **[**7**:**0**]** c\_addrIN\_wire**;**

**wire** **[**7**:**0**]** c\_dataIN\_wire**;**

// assign c\_addrIN\_wire = Addr;

**assign** c\_dataIN\_wire **=** data\_in**;**

// assign c\_addrIN\_out = c\_addrIN\_wire;

**assign** c\_dataIN\_out **=** c\_dataIN\_wire**;**

**output** target\_rw\_out**;**

**wire** target\_rw\_wire**;**

**reg** target\_rw**;** //Tartget Read or Write Value to save on miss

**assign** target\_rw\_wire **=** target\_rw**;**

**assign** target\_rw\_out **=** target\_rw\_wire**;**

**integer** i**;**

**output** **reg** **[**3**:**0**]** state**;** //Current State Register

**reg** **[**d\_width**-**1**:**0**]** ram\_data\_in\_w**;**

//Assign Cache Data Monitor Outputs

**assign** data0 **=** cache\_data**[**0**];**

**assign** data1 **=** cache\_data**[**1**];**

**assign** data2 **=** cache\_data**[**2**];**

**assign** data3 **=** cache\_data**[**3**];**

//Assign Cache Memory Address Monitor Outputs

**assign** addr0 **=** cache\_addr**[**0**];**

**assign** addr1 **=** cache\_addr**[**1**];**

**assign** addr2 **=** cache\_addr**[**2**];**

**assign** addr3 **=** cache\_addr**[**3**];**

//Assign Cache Access Output

/\*assign access0 = cache\_access[0];

assign access1 = cache\_access[1];

assign access2 = cache\_access[2];

assign access3 = cache\_access[3];\*/

//Declare DATA Ram unit and wires to control the RAM

**reg** ram\_clr**,** ram\_rw**,** ram\_enab**;**

**reg** **[**a\_width**-**1**:**0**]** ram\_addr**;**

**reg** **[**d\_width**-**1**:**0**]** ram\_data\_in**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_data\_out**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_data\_in\_monitor\_w**,** ram\_addr\_in\_monitor\_w**;**

**assign** ram\_data\_in\_monitor\_w **=** ram\_data\_in**;**

**assign** ram\_addr\_in\_monitor\_w **=** ram\_addr**;**

**output** **[**d\_width**-**1**:**0**]** ram\_data\_in\_monitor**;**

**output** **[**a\_width**-**1**:**0**]** ram\_addr\_in\_monitor**;**

**assign** ram\_data\_in\_monitor **=** ram\_data\_in\_monitor\_w**;**

**assign** ram\_addr\_in\_monitor **=** ram\_addr\_in\_monitor\_w**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem0**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem1**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem2**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem3**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem4**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem5**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem6**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem7**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem8**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem9**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem10**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem11**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem12**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem13**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem14**;**

**wire** **[**d\_width**-**1**:**0**]** ram\_mem15**;**

//Connect RAM contents with Cache Output Ports

**assign** ram0 **=** ram\_mem0**;**

**assign** ram1 **=** ram\_mem1**;**

**assign** ram2 **=** ram\_mem2**;**

**assign** ram3 **=** ram\_mem3**;**

**assign** ram4 **=** ram\_mem4**;**

**assign** ram5 **=** ram\_mem5**;**

**assign** ram6 **=** ram\_mem6**;**

**assign** ram7 **=** ram\_mem7**;**

**assign** ram8 **=** ram\_mem8**;**

**assign** ram9 **=** ram\_mem9**;**

**assign** ram10 **=** ram\_mem10**;**

**assign** ram11 **=** ram\_mem11**;**

**assign** ram12 **=** ram\_mem12**;**

**assign** ram13 **=** ram\_mem13**;**

**assign** ram14 **=** ram\_mem14**;**

**assign** ram15 **=** ram\_mem15**;**

ram DATA\_RAM**(**clk**,** ram\_clr**,** ram\_enab**,** ram\_rw**,** ram\_addr**,** ram\_data\_in**,**

ram\_mem0**,** ram\_mem1**,** ram\_mem2**,** ram\_mem3**,** ram\_mem4**,**

ram\_mem5**,** ram\_mem6**,** ram\_mem7**,** ram\_mem8**,** ram\_mem9**,**

ram\_mem10**,** ram\_mem11**,** ram\_mem12**,** ram\_mem13**,** ram\_mem14**,**

ram\_mem15**,** ram\_data\_out**);**

**initial** **begin**

curr\_LRU **<=** 2'b00**;**

hit **<=** 1'b0**;**

cache\_hit **<=** 2'b11**;**

ram\_clr **<=** 1'b1**;**

**end**

**always** **@** **(posedge** clk**)** **begin**

**if(**clr**==**1'b0**)** **begin** //Clear Cache + DATA RAM

state **<=** 0**;**

**end**

**else** **if(**enab**==**1'b0**)** **begin** //High Z State for output if chip not enabled

state **<=** 0**;**

**end**

**else** **if(**enab**==**1'b1**)** **begin** //Only Read/Write if Cache Chip Enabled

**case(**state**)**

0**:** //Initial State

**begin**

hit **<=** 1'b0**;** //Initialize the test condition

//Test if target address exists in cache entries

**for(**i**=**0**;** i**<**n**;** i**=**i**+**1**)** **begin:**Read\_Hit\_Loop

**if(**Addr**==**cache\_addr**[**i**])** **begin** //HIT @ Index i

cache\_hit **<=** i**;**

hit **<=** 1**;**

**end**

**end**

target\_addr **<=** Addr**;**

target\_data **<=** data\_in**;**

state **<=** 1**;**

**if(**rw**==**1'b0**)** **begin** //read miss

target\_rw **<=** 0**;**

**end**

**else** **if** **(**rw**==**1'b1**)** **begin** //write miss

target\_rw **<=** 1**;**

**end**

**end** //End Hit test

1**:** **begin** //Identify hit or miss

**if(**hit**==**1**)** **begin** //HIT - T0

state **<=** 0**;** **end** //Reset

**else** **if(**hit**==**0**)** **begin**

state **<=** 2**;** //MISS - T1

**end**

**else** **begin**

hit **<=** 1'bZ**;**

state **<=** 0**;**

**end**

**end**

2**:** state **<=** 3**;**

3**:** **begin**

**if(**target\_rw**==**1'b0**)**

state **<=** 4**;**

**else** **if(**target\_rw**==**1'b1**)**

state **<=** 6**;**

**end**

4**:** state **<=** 5**;**

5**:** state **<=** 8**;**

6**:** state **<=** 7**;**

7**:** state **<=** 8**;**

8**:** state **<=** 9**;**

9**:** state **<=** 10**;**

10**:** state **<=** 11**;**

11**:** state **<=** 12**;**

12**:** **begin**

**if(**target\_rw**==**1'b0**)** //Read Miss

state **<=** 13**;**

**else** **if(**target\_rw**==**1'b1**)** //Write Miss

state **<=** 14**;**

**end**

13**:** state **<=** 0**;**

14**:** state **<=** 0**;**

**default:** state **<=** 0**;**

**endcase**

**end** //End Read/WRITE if Cache Enabled

**end** //End @ Posedge

**always** **@** **(**state**)** **begin**

**if(**clr**==**1'b0**)** **begin**

//ram\_clr <= 1'b0;

**for(**i**=**0**;** i**<**4**;** i**=**i**+**1**)** **begin:**CLR\_loop

cache\_data**[**i**]** **<=** 8'b00000000**;**

cache\_addr**[**i**]** **<=** 8'b00000000**;**

cache\_access**[**i**]** **<=** 0**;**

**end**

curr\_LRU **<=** 2'b00**;**

**end**

**if(**enab**==**1'b1**)** **begin**

**case(**state**)**

0**:** //HIT Test

**begin**

//Wait for next clock cycle

**end**

1**:** //HIT

**begin**

**if(**hit**==**1'b1**)** **begin** //Update Access Records for LRU

**for(**i**=**0**;** i**<**n**;** i**=**i**+**1**)** **begin:**Update\_Access\_Loop

**if(**i**!=**cache\_hit**)** **begin**

**if(**cache\_access**[**i**]>**cache\_access**[**cache\_hit**])** **begin**

//Outdated Access record, decrement records greater than

//the hit record by 1. Hit record will be set to highest

//access metric of 3, indicating most recently used.

cache\_access**[**i**]** **<=** cache\_access**[**i**]-**1**;**

**if(**cache\_access**[**i**]==**0**)** **begin** curr\_LRU **<=** i**;** **end**

**end**

**end**

**end** //End Update\_Access\_Loop

cache\_access**[**cache\_hit**]** **<=** 3**;** //Update hit index to MRU

**if(**rw**==**1'b0**)** **begin** //Hit Read

data\_out **<=** cache\_data**[**cache\_hit**];**

**end** **else** **begin** //Hit Write

cache\_data**[**cache\_hit**]** **<=** data\_in**;**

**end**

**end**

**end**

2**:** //Miss - Prepare to write to RAM from cache

**begin**

ram\_enab **<=** 1'b1**;** //enable ram

ram\_rw **<=** 1'b1**;** //write

ram\_addr **<=** cache\_addr**[**curr\_LRU**];**

ram\_data\_in **<=** cache\_data**[**curr\_LRU**];**

**end**

3**:** //Miss - Write LRU entry to RAM

**begin**

ram\_addr **<=** cache\_addr**[**curr\_LRU**];**

ram\_data\_in **<=** cache\_data**[**curr\_LRU**];**

**end**

4**:** //Miss READ- Prepare to Read from RAM

**begin**

ram\_rw **<=** 1'b0**;**

ram\_addr **<=** target\_addr**;**

**end**

5**:** //Miss READ - Fill Cache with target address

**begin**

cache\_data**[**curr\_LRU**]** **<=** ram\_data\_out**;**

cache\_addr**[**curr\_LRU**]** **<=** target\_addr**;**

**end**

6**:** //Miss WRITE - Write Target to RAM

**begin**

//ram\_addr <= target\_addr;

//ram\_data\_in <= target\_data;

**end**

7**:** //Miss WRITE - Fill CURR LRU

**begin**

cache\_data**[**curr\_LRU**]** **<=** data\_in**;**

cache\_addr**[**curr\_LRU**]** **<=** target\_addr**;**

**end**

8**:** //Miss - Update Cache Access Records

**begin**

**for(**i**=**0**;** i**<**n**;** i**=**i**+**1**)** **begin:**Update\_Access\_Miss

**if(**i**!=**curr\_LRU**)** **begin**

**if(**cache\_access**[**i**]==**2'b00**)** **begin**

curr\_LRU **<=** i**;**

**end** **else** **begin**

cache\_access**[**i**]** **<=** cache\_access**[**i**]-**1**;**

**end**

**end** **else** **if(**i**==**curr\_LRU**)** **begin**

cache\_access**[**i**]** **<=** 3**;**

**end**

**end**

**end**

9**:** //Miss - Set new LRU

**begin**

**for(**i**=**0**;** i**<**n**;** i**=**i**+**1**)** **begin:**Update\_LRU

**if(**i**!=**curr\_LRU**)** **begin**

**if(**cache\_access**[**i**]==**2'b00**)** **begin**

curr\_LRU **<=** i**;**

**end**

**end**

**end**

**end**

10**:** //Miss - Do Nothing (Eat Up Clock Cycles For Delay)

**begin**

ram\_enab **<=** 1'b0**;**

**end**

11**:** //Miss - Do Nothing (Eat Up Clock Cycles For Delay)

**begin**

ram\_enab **<=** 1'b0**;**

**end**

12**:** //Miss - Do Nothing (Eat Up Clock Cycles For Delay)

**begin**

ram\_enab **<=** 1'b0**;**

**end**

13**:** //Miss READ - Output Targeted Memory Data

**begin**

i **=** cache\_access**[**3**];**

data\_out **<=** cache\_data**[**i**];**

**end**

14**:** //Miss WRITE - Do Nothing

**begin**

ram\_enab **<=** 1'b0**;**

**end**

**endcase**

**end**

**end**

**endmodule**

## Ram.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// RAM : Random Access Memory module - Behavioral Style (Parameterized)

// RAM unit has 8 bit wide data field and 256 addresses (2\*\*8)

//

// Inputs: Addr, enab, clr, rw, data\_in

// Addr: Target memory address

// data\_in: input line for data, Write to target address

// enab: Chip enable line

// clr: Active low synchronous clear

// rw: Read/Write control line

//

// Outputs: mem0, mem1, mem2, mem3, mem4, mem5, mem6, mem7, data\_out

// mem0-7 are 8 outputs used for checking the current

// contents of the RAM chip

// data\_out: Output data port, Read from target address

//

// rw enab clr function

// x x 0 Clear all RAM contents to zero \*Top Priority

// x 0 1 RAM Chip not enabled - Do not read or write

// 0 1 1 Read Target Address

// 1 1 1 Write

//

//////////////////////////////////////////////////////////////////////////////////

**module** ram**(**clk**,** clr**,** enab**,** rw**,** Addr**,** data\_in**,** mem0**,** mem1**,** mem2**,** mem3**,** mem4**,** mem5**,**

mem6**,** mem7**,** mem8**,** mem9**,** mem10**,** mem11**,** mem12**,** mem13**,** mem14**,** mem15**,**

data\_out**);**

**parameter** d\_width **=** 8**;**

**parameter** a\_width **=** 8**;**

//Input Ports

**input** clk**,** clr**,** enab**,** rw**;**

**input** **[**a\_width**-**1**:**0**]** Addr**;**

**input** **[**d\_width**-**1**:**0**]** data\_in**;**

//Output Ports

**output** **[**d\_width**-**1**:**0**]** mem0**;**

**output** **[**d\_width**-**1**:**0**]** mem1**;**

**output** **[**d\_width**-**1**:**0**]** mem2**;**

**output** **[**d\_width**-**1**:**0**]** mem3**;**

**output** **[**d\_width**-**1**:**0**]** mem4**;**

**output** **[**d\_width**-**1**:**0**]** mem5**;**

**output** **[**d\_width**-**1**:**0**]** mem6**;**

**output** **[**d\_width**-**1**:**0**]** mem7**;**

**output** **[**d\_width**-**1**:**0**]** mem8**;**

**output** **[**d\_width**-**1**:**0**]** mem9**;**

**output** **[**d\_width**-**1**:**0**]** mem10**;**

**output** **[**d\_width**-**1**:**0**]** mem11**;**

**output** **[**d\_width**-**1**:**0**]** mem12**;**

**output** **[**d\_width**-**1**:**0**]** mem13**;**

**output** **[**d\_width**-**1**:**0**]** mem14**;**

**output** **[**d\_width**-**1**:**0**]** mem15**;**

**output** **reg** **[**d\_width**-**1**:**0**]** data\_out**;**

//Declare memory register

**reg** **[**d\_width**-**1**:**0**]** memory **[**2**\*\***a\_width**-**1**:**0**];**

//Define Loop Variable i

**integer** i**;**

//Assign mem0-7 to first 8 memory indices

**assign** mem0 **=** memory**[**0**];**

**assign** mem1 **=** memory**[**1**];**

**assign** mem2 **=** memory**[**2**];**

**assign** mem3 **=** memory**[**3**];**

**assign** mem4 **=** memory**[**4**];**

**assign** mem5 **=** memory**[**5**];**

**assign** mem6 **=** memory**[**6**];**

**assign** mem7 **=** memory**[**7**];**

**assign** mem8 **=** memory**[**8**];**

**assign** mem9 **=** memory**[**9**];**

**assign** mem10 **=** memory**[**10**];**

**assign** mem11 **=** memory**[**11**];**

**assign** mem12 **=** memory**[**12**];**

**assign** mem13 **=** memory**[**13**];**

**assign** mem14 **=** memory**[**14**];**

**assign** mem15 **=** memory**[**15**];**

**initial** **begin**

memory**[**0**]** **=** 8'b00000000**;**

memory**[**1**]** **=** 8'b00000001**;**

memory**[**2**]** **=** 8'b01111111**;**

memory**[**3**]** **=** 8'b11101111**;**

memory**[**4**]** **=** 8'b00011000**;**

memory**[**5**]** **=** 8'b00000100**;**

memory**[**6**]** **=** 8'b11011011**;**

memory**[**7**]** **=** 8'b10011001**;**

memory**[**8**]** **=** 8'b00000000**;**

memory**[**9**]** **=** 8'b00000000**;**

memory**[**10**]** **=** 8'b00000000**;**

memory**[**11**]** **=** 8'b00000000**;**

memory**[**12**]** **=** 8'b00000000**;**

memory**[**13**]** **=** 8'b00000000**;**

memory**[**14**]** **=** 8'b00000000**;**

memory**[**15**]** **=** 8'b00000000**;**

memory**[**16**]** **=** 8'b00000000**;**

memory**[**17**]** **=** 8'b00000000**;**

memory**[**18**]** **=** 8'b00000000**;**

memory**[**19**]** **=** 8'b00000000**;**

memory**[**20**]** **=** 8'b00000000**;**

memory**[**21**]** **=** 8'b00000000**;**

memory**[**22**]** **=** 8'b00000000**;**

memory**[**23**]** **=** 8'b00000000**;**

memory**[**24**]** **=** 8'b00000000**;**

memory**[**25**]** **=** 8'b00000000**;**

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memory**[**254**]** **=** 8'b00000000**;**

memory**[**255**]** **=** 8'b00000000**;**

**end**

//Handle CLR/READ/WRITE at positive edge of clk

**always** **@(posedge** clk**)** **begin**

**if(**clr**==**1'b0**)** **begin:**clrBlock //Clear memory contents

**for(**i**=**0**;** i**<(**2**\*\***a\_width**);** i**=**i**+**1**)** **begin:**Clr\_Loop

memory**[**i**]** **<=** 0**;**

data\_out **<=** 8'b00000000**;**

**end**

**end**

**else** **if(**enab**==**1'b1**)** **begin** //Only Read/Write if RAM Chip enabled

**if(**rw**==**1'b0**)** **begin** //Read

data\_out **<=** memory**[**Addr**];**

**end**

**else** **if(**rw**==**1'b1**)** **begin** //Write

memory**[**Addr**]** **<=** data\_in**;**

**end**

**end**

**else** **if(**enab**==**1'b0**)** **begin** //High Z state for output if chip not enabled

data\_out **<=** 8'b01010101**;**

**end**

**end**

**endmodule**

## iRam.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// RAM : Random Access Memory module - Behavioral Style (Parameterized)

// RAM unit has 8 bit wide data field and 256 addresses (2\*\*8)

//

// Inputs: Addr, enab, clr, rw, data\_in

// Addr: Target memory address

// data\_in: input line for data, Write to target address

// enab: Chip enable line

// clr: Active low synchronous clear

// rw: Read/Write control line

//

// Outputs: mem0, mem1, mem2, mem3, mem4, mem5, mem6, mem7, data\_out

// mem0-7 are 8 outputs used for checking the current

// contents of the RAM chip

// data\_out: Output data port, Read from target address

//

// rw enab clr function

// x x 0 Clear all RAM contents to zero \*Top Priority

// x 0 1 RAM Chip not enabled - Do not read or write

// 0 1 1 Read Target Address

// 1 1 1 Write

//

//////////////////////////////////////////////////////////////////////////////////

//module ram(clk, clr, enab, rw, Addr, data\_in, mem0, mem1, mem2, mem3, mem4, mem5,

// mem6, mem7, data\_out);

**module** iram**(**clk**,** clr**,** enab**,** rw**,** Addr**,** data\_out**);**

**parameter** d\_width **=** 16**;**

**parameter** a\_width **=** 8**;**

//Input Ports

**input** clk**,** clr**,** enab**,** rw**;**

**input** **[**a\_width**-**1**:**0**]** Addr**;**

//input [d\_width-1:0] data\_in;

//Output Ports

/\*output [d\_width-1:0] mem0;

output [d\_width-1:0] mem1;

output [d\_width-1:0] mem2;

output [d\_width-1:0] mem3;

output [d\_width-1:0] mem4;

output [d\_width-1:0] mem5;

output [d\_width-1:0] mem6;

output [d\_width-1:0] mem7;\*/

**output** **reg** **[**d\_width**-**1**:**0**]** data\_out**;**

//Declare memory register

**reg** **[**d\_width**-**1**:**0**]** memory **[**2**\*\***a\_width**-**1**:**0**];**

//Define Loop Variable i

**integer** i**;**

//Assign mem0-7 to first 8 memory indices

/\*assign mem0 = memory[0];

assign mem1 = memory[1];

assign mem2 = memory[2];

assign mem3 = memory[3];

assign mem4 = memory[4];

assign mem5 = memory[5];

assign mem6 = memory[6];

assign mem7 = memory[7];\*/

**initial** **begin**

memory**[**0**]** **=** 16'b0101001000000001**;**

memory**[**1**]** **=** 16'b0000001000000010**;**

memory**[**2**]** **=** 16'b0101100000000101**;**

memory**[**3**]** **=** 16'b1000100000000101**;**

memory**[**4**]** **=** 16'b0001000000000101**;**

memory**[**5**]** **=** 16'b0010100000000010**;**

memory**[**6**]** **=** 16'b0001001000000101**;**

memory**[**7**]** **=** 16'b0000101000001000**;**

memory**[**8**]** **=** 16'b0101100000000001**;**

memory**[**9**]** **=** 16'b0101000000000101**;**

memory**[**10**]** **=** 16'b0001000000000001**;**

memory**[**11**]** **=** 16'b0101100000000010**;**

memory**[**12**]** **=** 16'b0000101000000111**;**

memory**[**13**]** **=** 16'b0010100000000010**;**

memory**[**14**]** **=** 16'b0101100100000101**;**

memory**[**15**]** **=** 16'b0010101100000010**;**

memory**[**16**]** **=** 16'b0010001000001011**;**

memory**[**17**]** **=** 16'b0000001000010010**;**

memory**[**18**]** **=** 16'b0001001000000101**;**

memory**[**19**]** **=** 16'b0101100000000100**;**

memory**[**20**]** **=** 16'b0111100000000000**;**

memory**[**21**]** **=** 16'b0111100000000000**;**

memory**[**22**]** **=** 16'b0111100000000000**;**

memory**[**23**]** **=** 16'b0111100000000000**;**

memory**[**24**]** **=** 16'b0000001001100010**;**

memory**[**25**]** **=** 16'b0001101000000100**;**

memory**[**26**]** **=** 16'b0101100100000010**;**

memory**[**27**]** **=** 16'b1001100100000010**;**

memory**[**28**]** **=** 16'b0000000000000000**;**

memory**[**29**]** **=** 16'b0000000000000000**;**

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memory**[**149**]** **=** 16'b0000000000000000**;**

memory**[**150**]** **=** 16'b1001101001101111**;**

memory**[**151**]** **=** 16'b1010000000000110**;**

memory**[**152**]** **=** 16'b0101000000000110**;**

memory**[**153**]** **=** 16'b0100100000000000**;**

memory**[**154**]** **=** 16'b0000000000000000**;**

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memory**[**253**]** **=** 16'b0000000000000000**;**

memory**[**254**]** **=** 16'b0000000000000000**;**

memory**[**255**]** **=** 16'b0000000000000000**;**

**end**

//Handle CLR/READ/WRITE at positive edge of clk

**always** **@(posedge** clk**)** **begin**

**if(**clr**==**1'b0**)** **begin:**clrBlock //Clear memory contents

memory**[**0**]** **=** 16'b0101001000000001**;**

memory**[**1**]** **=** 16'b0000001000000010**;**

memory**[**2**]** **=** 16'b0101100000000101**;**

memory**[**3**]** **=** 16'b1000100000000101**;**

memory**[**4**]** **=** 16'b0001000000000101**;**

memory**[**5**]** **=** 16'b0010100000000010**;**

memory**[**6**]** **=** 16'b0001001000000101**;**

memory**[**7**]** **=** 16'b0000101000001000**;**

memory**[**8**]** **=** 16'b0101100000000001**;**

memory**[**9**]** **=** 16'b0101000000000101**;**

memory**[**10**]** **=** 16'b0001000000000001**;**

memory**[**11**]** **=** 16'b0101100000000010**;**

memory**[**12**]** **=** 16'b0000101000000111**;**

memory**[**13**]** **=** 16'b0010100000000010**;**

memory**[**14**]** **=** 16'b0101100100000101**;**

memory**[**15**]** **=** 16'b0010101100000010**;**

memory**[**16**]** **=** 16'b0010001000001011**;**

memory**[**17**]** **=** 16'b0000001000010010**;**

memory**[**18**]** **=** 16'b0001001000000101**;**

memory**[**19**]** **=** 16'b0101100000000100**;**

memory**[**20**]** **=** 16'b0111100000000000**;**

memory**[**21**]** **=** 16'b0111100000000000**;**

memory**[**22**]** **=** 16'b0111100000000000**;**

memory**[**23**]** **=** 16'b0111100000000000**;**

memory**[**24**]** **=** 16'b0000001001100010**;**

memory**[**25**]** **=** 16'b0001101000000100**;**

memory**[**26**]** **=** 16'b0101100100000010**;**

memory**[**27**]** **=** 16'b1001100100000010**;**

memory**[**28**]** **=** 16'b0000000000000000**;**

memory**[**29**]** **=** 16'b0000000000000000**;**

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memory**[**150**]** **=** 16'b1001101001101111**;**

memory**[**151**]** **=** 16'b1010000000000110**;**

memory**[**152**]** **=** 16'b0101000000000110**;**

memory**[**153**]** **=** 16'b0100100000000000**;**

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memory**[**253**]** **=** 16'b0000000000000000**;**

memory**[**254**]** **=** 16'b0000000000000000**;**

memory**[**255**]** **=** 16'b0000000000000000**;**

**end**

**else** **if(**enab**==**1'b1**)** **begin** //Only Read/Write if RAM Chip enabled

**if(**rw**==**1'b0**)** **begin** //Read

data\_out **<=** memory**[**Addr**];**

**end**

**else** **if(**rw**==**1'b1**)** **begin** //Write

//memory[Addr] <= data\_in;

**end**

**end**

**else** **if(**enab**==**1'b0**)** **begin** //High Z state for output if chip not enabled

data\_out **<=** 16'b1000000010000000**;**

**end**

**end**

**endmodule**

## MHVPIS.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Maskable Hardware Vectorized Priority Interrupt System

//

// 4 different interrupts handled using priority assignment.

//

// PRIORITY | Interrupt Service Routine

// ------------------------------------

// 0 | Zero ALU output

// 1 | Overflow (ALU) Output

// 2 | Illegal OPcode

// 3 | INPUT/OUTPUT Interrupt

//

//

//////////////////////////////////////////////////////////////////////////////////

**module** MHVPIS**(**clk**,** itr\_clr**,** itr\_in**,** mask\_in**,** itr\_en**,** i\_pending**,** PC\_out**,** ITR\_register**,** MASK\_register**);**

**input** clk**;** //Input clock signal

//input clr; //Active low clear for whole system

**input** itr\_clr**;** //Clear pending interrupts

**input** itr\_en**;** //Enable or disable interrupt handler

**input** **[**3**:**0**]** mask\_in**;** //Register containing interrupt mask vector (size: 4)

**input** **[**3**:**0**]** itr\_in**;** //Vector containing interrupt input signals

**output** i\_pending**;** //Pending interrupt

**output** **[**7**:**0**]** PC\_out**;** //Memory address containing ISR

**output** **[**3**:**0**]** ITR\_register**,** MASK\_register**;**

**reg** **[**7**:**0**]** isr\_addr1**,** isr\_addr2**;** //ISR Addresses

**reg** **[**7**:**0**]** isr\_addr3**,** isr\_addr4**;** //ISR Addresses

**initial** **begin** //define ISR Addresses

isr\_addr1**[**7**:**0**]** **=** 8'b10010110**;** //ISR4 150 - Handle Zero Output

isr\_addr2**[**7**:**0**]** **=** 8'b10110100**;** //ISR2 180 - Handle Overflow

isr\_addr3**[**7**:**0**]** **=** 8'b11011100**;** //ISR3 220 - Bad Opcode

isr\_addr4**[**7**:**0**]** **=** 8'b11001000**;** //ISR1 200 - Handle IO

**end**

**wire** **[**3**:**0**]** itr\_and\_w**;**

**wire** **[**1**:**0**]** encoder\_w**;**

**wire** itr\_pending\_w**;**

**wire** **[**3**:**0**]** itr\_reg\_w**;**

**wire** **[**3**:**0**]** mask\_reg\_w**;**

**assign** MASK\_register **=** mask\_reg\_w**;**

**assign** ITR\_register **=** itr\_reg\_w**;**

//module ld\_st\_reg(clk, clr, set, in, out);

//Interrupt Register - Load Store

ld\_st\_reg\_4bit ITR\_REG**(**clk**,** itr\_clr**,** itr\_en**,** itr\_in**,** itr\_reg\_w**);**

//Mask Register - Load Store

ld\_st\_reg\_4bit MASK\_REG**(**clk**,** itr\_clr**,** itr\_en**,** mask\_in**,** mask\_reg\_w**);**

//priority logic

// ITR1: 1000

// ITR2: 0100

// ITR3: 0010

// ITR4: 0001

**and** andITR1**(**itr\_and\_w**[**0**],** itr\_reg\_w**[**0**],** mask\_reg\_w**[**0**]);**//Priority: 1

**and** andITR2**(**itr\_and\_w**[**1**],** itr\_reg\_w**[**1**],** mask\_reg\_w**[**1**]);**//Priority: 2

**and** andITR3**(**itr\_and\_w**[**2**],** itr\_reg\_w**[**2**],** mask\_reg\_w**[**2**]);**//Priority: 3

**and** andITR4**(**itr\_and\_w**[**3**],** itr\_reg\_w**[**3**],** mask\_reg\_w**[**3**]);**//Priority: 4

//Encoder - Using Priority Encoder - Select Target PC Address

//module pri\_encoder\_4\_2(in, enab, out, valid);

pri\_encoder\_4\_2 ENCODER**(**itr\_and\_w**,** 1'b1**,** encoder\_w**,** itr\_pending\_w**);**

//Check if interrupt pending should be enabled

**and** iPendingEnab**(**i\_pending**,** itr\_pending\_w**,** itr\_en**);**

//Select Output using mux 4x1 MUX. Output from Encoder = Select Lines

//module mux\_4\_1\_behavioral(i1, i2, i3, i4, sel, out);

mux\_4\_1 PC\_MUX**(**isr\_addr1**,** isr\_addr2**,** isr\_addr3**,** isr\_addr4**,** encoder\_w**,** PC\_out**);**

**endmodule**

## stack.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Module Name: stack

//

// Description:

// Parameterized stack with synchronous active low clear

//

// Control States

// 00 push

// 01 pop

// 10 Do nothing

// 11 Do nothing

//

//

//

//

//////////////////////////////////////////////////////////////////////////////////

**module** stack**(**en**,** clr**,** clk**,** con**,** data\_in**,** data\_out**);**

**parameter** width **=** 8**;** //the width of the data in bits

**parameter** depth **=** 3**;** // amout of data

**input** en**;** // enable

**input** clr**;** // clear all contents

**input** clk**;** // the clock

**input** **[**1**:**0**]** con**;** // controller signal. pop when con=01. push when con=00. do nothing when con=10/11;

**input** **[**width**-**1**:**0**]** data\_in**;**

**reg** full**;** // inform controller if stack full. 1 on full, else 0

**output** **reg** **[**width**-**1**:**0**]** data\_out**;**

**reg** **[(**2**\*\***depth**)-**1**:**0**]** size**;** // the amount of data in the stack at any given time

**reg** empty**;** // 1 if the stack is empty, else 0

**reg** **[**width**-**1**:**0**]** data **[(**2**\*\***depth**)-**1**:**0**];** // reg to hold the data

**integer** i**;**

**always@(posedge** clk**)**

**begin**

**if(**clr **==** 0**)**

**begin**

**for(**i**=**0**;** i**<(**2**\*\***depth**);** i**=**i**+**1**)**

**begin**

data**[**i**]** **<=** 0**;**

**end**

full **<=** 0**;**

empty **<=** 1**;**

size **<=** 0**;**

data\_out **<=** 0**;**

**end**

**else**

**begin**

**if** **(**en **==** 1**)** // if the stack is enabled

**begin**

**if** **(**con **==** 2'b00**)** // if controller says push

**begin**

**if(** full **==** 0 **)** //if stack not full

**begin**

**if(**size **<** **(**2**\*\***depth**))**

**begin**

data**[**size**]** **<=** data\_in**;** // store data

empty **<=** 0**;**

size **<=** size **+** 1**;** // increment

**end**

**else**

full **<=** 1**;** // stack is full - controller must pop to make room

**end**

**end**

**else** **if(** con **==** 2'b01**)** // pop --> controller = 1

**begin**

**if(**empty **==** 0**)** //if the stack is not empty

**begin**

**if(**size **>** 0**)**

**begin**

data\_out **<=** data**[**size**-**1**];** // output last data in

full **<=** 0**;**

size **<=** size **-** 1**;** // decrement

**end**

**else**

empty **<=** 1**;** //stack is empty

**end**

**end**

**end**

**end**

**end**

**endmodule**

## alu\_nbit.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Module Name: alu\_bitslice

//

// Data inputs: in0, in1, c\_in (carry in)

// control inputs: ctrl

// Output: alu\_out, c\_out (carry out), V (overflow)

//

// ctrl2 ctrl1 ctrl0 | ALU Operation

// 0 0 0 | in0 + in1 + c\_in (ADD)

// 0 0 1 | in0 + ~in1 + 1 (SUB)

// 0 1 0 | in0 | in1 (OR)

// 0 1 1 | in0 | ~in1 (OR)

// 1 0 0 | in0 & in1 (AND)

// 1 0 1 | in0 & ~in1 (AND)

// 1 1 0 | ~in0 (COMPLEMENT)

// 1 1 1 | ~in1 (COMPLEMENT)

//

//

//////////////////////////////////////////////////////////////////////////////////

**module** alu\_nbit**(**in0**,**in1**,**c\_in**,**ctrl**,**c\_out**,**alu\_out**,**V**,** Z**);**

**parameter** n**=**8**;**

**input** **[**n**-**1**:**0**]** in0**,**in1**;** //Input data1 and Input data2

**input** c\_in**;** //Carry In

**input** **[**2**:**0**]** ctrl**;** //ALU Control Lines

**output** c\_out**;** //Carry out

**output** **[**n**-**1**:**0**]** alu\_out**;** //ALU data Output

**output** V**;** //Overflow output

**output** Z**;** //Zero Output

**wire** **[**n**:**0**]** w\_c**;**

**wire** **[**n**-**1**:**0**]** zero\_check**;**

**assign** zero\_check**[**0**]** **=** alu\_out**[**0**];**

//Instantiate module alu\_bitslice(a,b,c,c\_in,c\_out,alu\_out);

genvar i**;**

**assign** w\_c**[**0**]=**c\_in**;**

**assign** c\_out **=** w\_c**[**n**];**

generate

**for(**i**=**0**;** i**<**n**;** i**=**i**+**1**)**

**begin:**submit

alu\_bitslice ALU\_slice**(**in0**[**i**],**in1**[**i**],**ctrl**,**w\_c**[**i**],**w\_c**[**i**+**1**],**alu\_out**[**i**]);**

**end**

**for(**i**=**0**;** i**<**n**-**1**;** i**=**i**+**1**)**

**begin:**or\_loop

**or** OR **(**zero\_check**[**i**+**1**],**alu\_out**[**i**+**1**],**zero\_check**[**i**]);**

**end**

endgenerate

**xor** overflow\_detect**(**V**,**w\_c**[**n**],**w\_c**[**n**-**1**]);**

//handle zero

**not(**Z**,**zero\_check**[**n**-**1**]);**

**endmodule**

## alu\_bitslice.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Module Name: alu\_bitslice

//

// Data inputs: a, b, c\_in (carry in)

// control inputs: c

// Output: f\_out, c\_out (carry out)

//

// Structural style - (Gate Level)

//

//////////////////////////////////////////////////////////////////////////////////

**module** alu\_bitslice**(**a**,**b**,**c**,**c\_in**,**c\_out**,**f\_out**);**

**input** a**;**

**input** b**;**

**input** **[**2**:**0**]** c**;**

**input** c\_in**;**

**output** f\_out**;**

**output** c\_out**;**

**wire** wire\_bfa\_out**,** w\_or\_out**,** w\_and\_out**,** w\_not\_out**,** w\_b**,** w\_not\_b\_out**,** w\_not\_a\_out**;**

**wire** w\_fout**;**

//Negate a and b (wires out)

**not** b\_not**(**w\_not\_b\_out**,**b**);**

**not** a\_not**(**w\_not\_a\_out**,**a**);**

//B is negated when C[0] is 1, use 2x1 mux to make selection

//module mux\_2\_1\_rtl(i1, i2, sel, out);

mux\_2\_1 MUX\_2x1\_1**(**b**,**w\_not\_b\_out**,**c**[**0**],**w\_b**);**

//Setup Binary Full Adder

//module bfa\_gate(i0, i1, ci, sout, cout);

bfa\_gate BFA**(**a**,**w\_b**,**c\_in**,**w\_bfa\_out**,**c\_out**);**

//OR Gate

**or** OR\_Gate**(**w\_or\_out**,** a**,** w\_b**);**

//AND Gate

**and** AND\_Gate**(**w\_and\_out**,** a**,** w\_b**);**

//The selection of ~a or ~b is made on c[0], use a 2x1 mux to make selection

//module mux\_2\_1\_rtl(i1, i2, sel, out);

mux\_2\_1 MUX\_2x1\_2**(**w\_not\_a\_out**,** w\_not\_b\_out**,** c**[**0**],** w\_not\_out**);**

//f\_out is determined on the selection of c[2] and c[1], use 4x1 mux

//module mux\_4\_1\_behavioral(i1, i2, i3, i4, sel, out);

mux\_4\_1 MUX\_4x1**(**w\_bfa\_out**,** w\_or\_out**,** w\_and\_out**,** w\_not\_out**,** c**[**2**:**1**],** w\_fout**);**

**assign** f\_out **=** w\_fout**;**

**endmodule**

## bfa\_gate.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Module Name: bfa\_gate

// Binary full adder with gate description

//

//////////////////////////////////////////////////////////////////////////////////

**module** bfa\_gate**(**i0**,** i1**,** ci**,** sout**,** cout**);**

**input** i0**,** i1**,** ci**;**

**output** sout**,** cout**;**

**wire** wxor**,** wand0**,** wand1**;**

// Output, input, input

**xor** Xor0**(**wxor**,** i0**,** i1**);**

**xor** Xor1**(**sout**,** wxor**,** ci**);**

**and** And0**(**wand0**,** wxor**,** ci**);**

**and** And1**(**wand1**,** i0**,** i1**);**

**or** Or0**(**cout**,** wand0**,** wand1**);**

**endmodule**

## dff\_syn\_low\_clr\_set.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Module Name: dff\_syn\_low\_clr\_set

//

//

// CLR and SET are Active Low. CLR -> Highest Priority

//

//////////////////////////////////////////////////////////////////////////////////

**module** dff\_syn\_low\_clr\_set**(**clk**,**d**,**set**,**clr**,**q**,**q\_cmp**);**

**input** clr**,** set**,** d**,** clk**;**

**output** **reg** q**;**

**output** q\_cmp**;**

**always** **@** **(posedge** clk**)** **begin**

**if(**clr**==**1'b0**)** **begin** q**=**1'b0**;** **end**

**else** **if(**set**==**1'b0**)** **begin** q**=**1'b1**;** **end**

**else** **begin** q**=**d**;** **end**

**end**

**assign** q\_cmp**=~**q**;**

**endmodule**

## ld\_st\_reg.v

`timescale 1ns **/** 1ps

///////////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Heath

// Accumulator Based Processor

//

//Parameterized load store register

//

// clr set funct

// 0 0 clear register to zero

// 0 1 clear register to zero

// 1 0 store

// 1 1 load from input

//

///////////////////////////////////////////////////////////////////////////////////////

**module** ld\_st\_reg**(**clk**,** clr**,** set**,** in**,** out**);**

**parameter** n **=** 8**;** //register size in bits

**input** **[**n**-**1**:**0**]** in**;** //load input

**input** set**;** //set

**input** clr**;** //active-low clear

**input** clk**;** //clock

**output** **reg** **[**n**-**1**:**0**]** out**;** //output

**always@(posedge** clk**)**

**begin**

**if(**clr **==** 0**)** //clear to 0s

**begin**

out **<=** 8'b00000000**;**

**end**

**else** **if(** **(**set**==**0**)** **&&** **(**clr**==**0**)** **)** //clear to 0s

**begin**

out **<=** 8'b00000000**;**

**end**

**else** **if(**set **==** 1**)** //load

**begin**

out **<=** in**;**

**end**

**else** //store

**begin**

out **<=** out**;**

**end**

**end**

**endmodule**

## ld\_St\_reg\_4bit.v

`timescale 1ns **/** 1ps

///////////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Heath

// Accumulator Based Processor

//

//Parameterized load store register

//

// clr set funct

// 0 0 clear register to zero

// 0 1 clear register to zero

// 1 0 store

// 1 1 load from input

//

///////////////////////////////////////////////////////////////////////////////////////

**module** ld\_st\_reg\_4bit**(**clk**,** clr**,** set**,** in**,** out**);**

**parameter** n **=** 4**;** //register size in bits

**input** **[**n**-**1**:**0**]** in**;** //load input

**input** set**;** //set

**input** clr**;** //active-low clear

**input** clk**;** //clock

**output** **reg** **[**n**-**1**:**0**]** out**;** //output

**always@(posedge** clk**)**

**begin**

**if(**clr **==** 0**)** //clear to 0s

**begin**

out **<=** 4'b0000**;**

**end**

**else** **if(** **(**set**==**0**)** **&&** **(**clr**==**0**)** **)** //clear to 0s

**begin**

out **<=** 4'b0000**;**

**end**

**else** **if(**set **==** 1**)** //load

**begin**

out **<=** in**;**

**end**

**else** //store

**begin**

out **<=** out**;**

**end**

**end**

**endmodule**

## mux\_2\_1.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Heath - Spring 2013

// Accumulator Based Processor

//

// 2x1 MUX operation -

// Select | OUTPUT

// 0 | i0

// 1 | i1

//

//////////////////////////////////////////////////////////////////////////////////

**module** mux\_2\_1**(**i0**,** i1**,** sel**,** out**);**

**input** **[**7**:**0**]** i0**,** i1**;**

**input** sel**;**

**output** **reg** **[**7**:**0**]** out**;**

**always** **@(**i0 **or** i1 **or** sel**)**

**begin**

**case(** sel **)**

1'b0**:** out **=** i0**;**

1'b1**:** out **=** i1**;**

**default:** out **=** 8'b00000000**;**

**endcase**

**end**

**endmodule**

## mux\_3\_1.v

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Heath - Spring 2013

// Accumulator Based Processor

//

// 3x1 MUX operation -

// Select | OUTPUT

// 00 | i0

// 01 | i1

// 10 | i2

//

//////////////////////////////////////////////////////////////////////////////////

**module** mux\_3\_1**(**i0**,** i1**,** i2**,** sel**,** out**);**

**input** **[**7**:**0**]** i0**,** i1**,** i2**;**

**input** **[**1**:**0**]** sel**;**

**output** **reg** **[**7**:**0**]** out**;**

**always** **@(**i0 **or** i1 **or** i2 **or** sel**)**

**begin**

**case(** sel **)**

2'b00**:** out **=** i0**;**

2'b01**:** out **=** i1**;**

2'b10**:** out **=** i2**;**

**default:** out **=** 8'b00000000**;**

**endcase**

**end**

**endmodule**

## mux\_4\_1.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Heath - Spring 2013

// Accumulator Based Processor

//

// 4x1 MUX operation -

// Select | OUTPUT

// 00 | i0

// 01 | i1

// 10 | i2

// 11 | i3

//

//////////////////////////////////////////////////////////////////////////////////

**module** mux\_4\_1**(**i0**,** i1**,** i2**,** i3**,** sel**,** out**);**

**input** **[**7**:**0**]** i0**,** i1**,** i2**,** i3**;**

**input** **[**1**:**0**]** sel**;**

**output** **reg** **[**7**:**0**]** out**;**

**always** **@(**i0 **or** i1 **or** i2 **or** i3 **or** sel**)**

**begin**

**case(** sel **)**

2'b00**:** out **=** i0**;**

2'b01**:** out **=** i1**;**

2'b10**:** out **=** i2**;**

2'b11**:** out **=** i3**;**

**default:** out **=** 8'b00000000**;**

**endcase**

**end**

**endmodule**

## mux\_5\_1.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Heath - Spring 2013

// Accumulator Based Processor

//

// 4x1 MUX operation -

//

// SELECT | OUTPUT

// 000 | i0

// 001 | i1

// 010 | i2

// 011 | i3

// 100 | i4

//

//////////////////////////////////////////////////////////////////////////////////

**module** mux\_5\_1**(**i0**,** i1**,** i2**,** i3**,** i4**,** sel**,** out**);**

**input** **[**7**:**0**]** i0**,** i1**,** i2**,** i3**,** i4**;**

**input** **[**2**:**0**]** sel**;**

**output** **reg** **[**7**:**0**]** out**;**

**always** **@(**i0 **or** i1 **or** i2 **or** i3 **or** i4 **or** sel**)**

**begin**

**case(** sel **)**

3'b000**:** out **=** i0**;**

3'b001**:** out **=** i1**;**

3'b010**:** out **=** i2**;**

3'b011**:** out **=** i3**;**

3'b100**:** out **=** i4**;**

**default:** out **=** 8'bZZZZZZZZ**;**

**endcase**

**end**

**endmodule**

## pc\_nbit.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// nbit\_pc : n-bit program counter built using behavioral syntax.

//

// Active low synchronous clear

//

// ctrl clr function

// x 0 Clear all PC bits to zero. \*Top Priority

// 00 1 Hold Count

// 01 1 Parallel Load

// 10 1 Increment by 1

// 11 1 increment by inc (increment variable)

//

//////////////////////////////////////////////////////////////////////////////////

**module** nbit\_pc**(**clk**,**clr**,** ctrl**,** pc\_in**,** pc\_out**);**

**parameter** n**=**8**;** //default 4-bit program counter

**parameter** inc**=**2**;** //default increment value

**input** clk**,** clr**;**

**input** **[**1**:**0**]** ctrl**;**

**input** **[**n**-**1**:**0**]** pc\_in**;**

**output** **reg** **[**n**-**1**:**0**]** pc\_out**;**

**always** **@(posedge** clk**)** **begin**

**if(**clr**==**0**)** **begin**

pc\_out **<=** 0**;**

**end**

**else** **begin**

**case(**ctrl**)**

0**:** pc\_out **<=** pc\_out**;** //Hold Count - Out = Previous state

1**:** pc\_out **<=** pc\_in**;** //Parallel load

2**:** pc\_out **<=** pc\_out**+**1**;** //Increment PC by 1

3**:** pc\_out **<=** pc\_out**+**inc**;** //Increment by increment variable.

**default:** pc\_out **<=** pc\_out**;** //Do nothing for any other case

**endcase**

**end**

**end**

**endmodule**

## pri\_encoder\_4\_2.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Priority Encoder 4 x 2

//

//////////////////////////////////////////////////////////////////////////////////

**module** pri\_encoder\_4\_2**(**in**,** enab**,** out**,** valid**);**

**input** **[**3**:**0**]** in**;**

**input** enab**;**

**output** **reg** **[**1**:**0**]** out**;**

**output** **reg** valid**;**

**always** **@** **(**in **or** enab**)** **begin**

**if(**enab**==**1'b0**)** **begin**

out **=** 2'bZZ**;**

valid **=** 1'b0**;**

**end**

**else** **begin**

**if(**in**[**3**]==**1'b1**)** **begin** out**=**2'b11**;** valid**=**1'b1**;** **end**

**else** **if(**in**[**2**]==**1'b1**)** **begin** out**=**2'b10**;** valid**=**1'b1**;** **end**

**else** **if(**in**[**1**]==**1'b1**)** **begin** out**=**2'b01**;** valid**=**1'b1**;** **end**

**else** **if(**in**[**0**]==**1'b1**)** **begin** out**=**2'b00**;** valid**=**1'b1**;** **end**

**else** **begin** out**=**2'bZZ**;** valid**=**1'b0**;** **end**

**end**

**end**

**endmodule**

## Shifter.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

// Sean McFeely

// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Shifter

// Priority (highest lowest): clr, set, clk

// set and clr are synchronous, and active low

//

// ctrl[1] ctrl[0] | Function:

// 0 0 | store

// 0 1 | Load in Parallel

// 1 0 | Left Shift

// 1 1 | Right Shift

//

//////////////////////////////////////////////////////////////////////////////////

**module** LdStr\_shifter**(**Reg\_in**,**clr**,**set**,**clk**,**Ls**,**Rs**,**ctrl**,**num\_shift**,**Reg\_out**);**

**parameter** n **=** 8**;** //8-bit accum reg + \*Note - if change must change num\_shift manually

**input** clr**,**set**,**clk**,**Ls**,**Rs**;** // Ls = Left Shift bit. Rs = Right Shift bit. (1 or 0)

**input** **[**1**:**0**]** ctrl**;** // control signal

**input** **[**n**-**1**:**0**]** Reg\_in**;** // input data to be operated on

**input** **[**2**:**0**]** num\_shift**;** // the number of shifts to execute (0 < num\_shift < 7)

**output** **reg** **[**n**-**1**:**0**]** Reg\_out**;**

**reg** curr**,** prev**;**

**integer** i**,** j**;**

**always@(posedge** clk**)** **begin**

**if(**clr **==** 1'b0**)** **begin** // Clear all bits to zero

Reg\_out **=** 8'b00000000**;**

**end**

**else** **if(**set **==** 1'b0**)** **begin** // Set all bits to one

Reg\_out **=** 8'b11111111**;**

**end**

**else** **begin**

**case(**ctrl**)**

2'b00**:begin** //Keep value stored in register

Reg\_out **=** Reg\_out**;**

**end**

2'b01**:begin** //Load in parallel

Reg\_out **=** Reg\_in**;**

**end**

2'b10**:begin** //Left Shift

**for(**i**=**0**;** i**<**num\_shift**;** i**=**i**+**1**)** **begin**

prev **=** Reg\_out**[**0**];**

Reg\_out**[**0**]** **=** Ls**;**

**for(**j**=**1**;**j**<**n**;**j**=**j**+**1**)** **begin**

curr **=** Reg\_out**[**j**];** //save current value

Reg\_out**[**j**]** **=** prev**;** //set current position value to previous position value

prev **=** curr**;**

**end**

**end**

**end**

2'b11**:begin** //Right Shift

**for(**i**=**0**;** i**<**num\_shift**;** i**=**i**+**1**)** **begin**

prev **=** Reg\_out**[**n**-**1**];**

Reg\_out**[**n**-**1**]** **=** Rs**;**

**for(**j**=(**n**-**2**);**j**>=**0**;**j**=**j**-**1**)** **begin**

curr **=** Reg\_out**[**j**];** //save current value

Reg\_out**[**j**]** **=** prev**;** //set current position value to previous position value

prev **=** curr**;**

**end**

**end**

**end**

**default:** Reg\_out **=** Reg\_out**;**

**endcase**

**end**

**end**

**endmodule**

## Stack.v

`timescale 1ns **/** 1ps

//////////////////////////////////////////////////////////////////////////////////

// Alex Hendren

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// EE480 - Spring 2013 - Heath

// Accumulator Based Processor

//

// Module Name: stack

//

// Description:

// Parameterized stack with synchronous active low clear

//

// Control States

// 00 push

// 01 pop

// 10 Do nothing

// 11 Do nothing

//

//

//

//

//////////////////////////////////////////////////////////////////////////////////

**module** stack**(**en**,** clr**,** clk**,** con**,** data\_in**,** data\_out**);**

**parameter** width **=** 8**;** //the width of the data in bits

**parameter** depth **=** 3**;** // amout of data

**input** en**;** // enable

**input** clr**;** // clear all contents

**input** clk**;** // the clock

**input** **[**1**:**0**]** con**;** // controller signal. pop when con=01. push when con=00. do nothing when con=10/11;

**input** **[**width**-**1**:**0**]** data\_in**;**

**reg** full**;** // inform controller if stack full. 1 on full, else 0

**output** **reg** **[**width**-**1**:**0**]** data\_out**;**

**reg** **[(**2**\*\***depth**)-**1**:**0**]** size**;** // the amount of data in the stack at any given time

**reg** empty**;** // 1 if the stack is empty, else 0

**reg** **[**width**-**1**:**0**]** data **[(**2**\*\***depth**)-**1**:**0**];** // reg to hold the data

**integer** i**;**

**always@(posedge** clk**)**

**begin**

**if(**clr **==** 0**)**

**begin**

**for(**i**=**0**;** i**<(**2**\*\***depth**);** i**=**i**+**1**)**

**begin**

data**[**i**]** **<=** 0**;**

**end**

full **<=** 0**;**

empty **<=** 1**;**

size **<=** 0**;**

data\_out **<=** 0**;**

**end**

**else**

**begin**

**if** **(**en **==** 1**)** // if the stack is enabled

**begin**

**if** **(**con **==** 2'b00**)** // if controller says push

**begin**

**if(** full **==** 0 **)** //if stack not full

**begin**

**if(**size **<** **(**2**\*\***depth**))**

**begin**

data**[**size**]** **<=** data\_in**;** // store data

empty **<=** 0**;**

size **<=** size **+** 1**;** // increment

**end**

**else**

full **<=** 1**;** // stack is full - controller must pop to make room

**end**

**end**

**else** **if(** con **==** 2'b01**)** // pop --> controller = 1

**begin**

**if(**empty **==** 0**)** //if the stack is not empty

**begin**

**if(**size **>** 0**)**

**begin**

data\_out **<=** data**[**size**-**1**];** // output last data in

full **<=** 0**;**

size **<=** size **-** 1**;** // decrement

**end**

**else**

empty **<=** 1**;** //stack is empty

**end**

**end**

**end**

**end**

**end**

**endmodule**

# Assembler Implementation

# Testing and Verification

## Test Programs

### Straight Line Control Flow

### Straight Line Control Flow with Looping Structures

### Subroutine Execution

### HVPI System

## Validation

### Straight Line Control Flow

### Straight Line Control Flow with Looping Structures

### Subroutine Execution

### HVPI System

# Conclusion

The current accumulator processor design is constructed using a single cycle model. To maximize performance, the controller will be built to support a two-stage pipeline. A two-stage pipeline will enable the processor to perform multiple operations under the same clock cycle; this is achieved by connecting components on individual bus lines thus preventing collision. Collision would occur when multiple functional units attempt to write to a bus during the same clock cycle. In addition to the pipelined approach, the processor implements a 4 word cache on the data memory thus improving latency associated with memory access. An MVHIPS is implemented to service interrupts as they occur during program execution by the processor. All of the components encompassed within the processor can be found in modern day processors, the problems to be faced will educate the team in dealing with real world design and troubleshooting exercises.

# References

To be updated as references are used.