Stage 0 - Instruction Fetch

	Global	PC		IR1_0		IR0_0		ACC_s_reg		Instruction Memory		MHVPIS		MUX_PC		PC Stack			Accum Stack		
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	clr	PC_ctrl[1]	PC_ctrl[0]	IR1_c0	IR1_s0	IR0_c0	IR0_s0	ACC_s_reg_clr	ACC_s_reg_set	imem_rw	imem_en	itr_clr	itr_en	CP9	CP8	PCs_en	PCs_ctrl[1]	PCs_ctrl[0]	ACCs_en	ACCs_ctrl[1]	ACCs_ctrl[0]
T0	1	0	1	1	0	1	0	1	0	0	1	0	0	1	0	1	1	0	1	1	0
T1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T2	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	0	1	0	0
T3	1	0	1	1	0	1	0	1	0	0	1	1	1	0	1	1	1	0	1	1	0
T4	1	0	0	1	1	1	1	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T5	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T6	1	1	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T7	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T8	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T9	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T10	1	0	1	1	0	1	0	1	0	0	1	1	1	1	1	1	1	0	1	1	0
T11	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T12	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	0	1	0	0
T13	1	0	0	1	0	1	0	1	0	0	1	0	1	0	0	1	0	1	1	0	1
T14	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0
T15	1	0	1	1	0	1	0	1	1	0	1	0	1	0	0	1	1	1	1	1	1