

Stage 1 - Instruction Execution

	Global	A	ACC	ALU				A_MUX		B	B_MUX		CACHE		CCR	IR_1				MAR	MDR	MUX_ACC			MUX_ALU			MUX_MAR	MUX_MDR			Shifter					
	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	clr	A_s	ACC_s	Alu_ctrl[2]	Alu_ctrl[1]	Alu_ctrl[0]	c_in	CP12	CP11	B_s	CP14	CP13	CH_en	CH_rw	CCR_s	IRO_c1	IRO_s1	IR1_c1	IR1_s1	Mar_s	Mdr_s	CP4	CP3	CP2	CP1b	CP1	CP0	CP10	CP7	CP6	CP6	Sh_ctrl[1]	Sh_ctrl[0]	LS	RS	set	
T0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1	0	0	0	0	1	
T1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0	1	1	0	0	1	1	0	0	0	0	1	
T2	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1	
T3	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1	0	1	1	0	0	0	0	0	1	
T4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0	1	
T5	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0	1	
T6	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1	
T7	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	1	0	1	1	0	0	1	0	0	0	1	
T8	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	0	0	1	1	0	0	0	0	0	1	
T9	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1	
T10	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0	1	
T11	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	0	0	1	
T12	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	1	
T13	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	0	1	
T14	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	0	1	1	1	0	0	0	0	0	1	
T15	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	1	1	1	1	0	0	0	0	0	1	
T16	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0	1	
T17	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	0	1	
T18	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0	1	1	0	0	0	0	0	1	
T19	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	
T20	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T21	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	
T22	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T23	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	
T24	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T25	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	1
T26	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T27	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	
T28	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T29	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T30	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T31	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T32	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	
T33	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	1	
T34	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	0	1	1	0	0	0	0	1	
T35	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	1	
T36	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	1	
T37	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	1	
T38	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	0	0	1	
T39	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	
T40	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	
T41	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	0	0	1	0	0	0	0	1	
T42	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	1	

T43	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1		
T44	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1		
T45	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T46	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T47	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T48	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T49	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T50	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T51	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T52	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	
T53	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	1	
T54	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1		
T55	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T56	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1		
T57	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1		
T58	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	1		
T59	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	1	
T60	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	1	
T61	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1		
T62	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	1		
T63	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	1	
T64	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0	1	
T65	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	1	
T66	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	
T67	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	
T68	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	
T69	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	
T70	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	
T71	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	
	clr	A_s	ACC_s	Alu_ctrl[2]	Alu_ctrl[1]	Alu_ctrl[0]	c_in	CP12	CP11	B_s	CP14	CP13	CH_en	CH_rw	CCR_s	IRO_c1	IRO_s1	IR1_c1	IR1_s1	Mar_s	Mdr_s	CP4	CP3	CP2	CP1b	CP1	CP0	CP10	CP7	CP6	CP6	Sh_ctrl[1]	Sh_ctrl[0]	LS	RS	set
	Global	A	ACC	ALU				A_MUX		B	B_MUX		CACHE		CCR	IR_1				MAR	MDR	MUX_ACC				MUX_ALU		MUX_MAR	MUX_MDR	Shifter						