

Logic Gates

CSE 4205: Digital Logic Design

Aashnan Rahman

Junior Lecturer

Department of Computer Science and Engineering (CSE)
Islamic University of Technology

01

Logic Gates

Device performing logical operations

Logic Gates

An **electric circuit** that **operate** on **one or more input signals** to generate an **output signal based** on **specific requirement(s)**

Switching Circuits / Binary Signal

Binary logic variable A can be represented as a switch A as following :

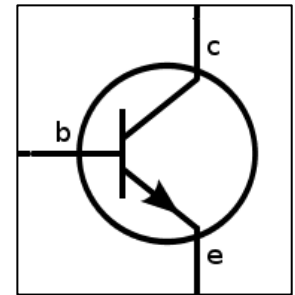
switch ON
logic 1



switch OFF
logic 0

Electronic digital circuits uses transistors as switches

- Conduct current → **switch on**
- Doesn't conduct current → **switch off**



02

Basic Gates

Building blocks used in digital electronics

AND Gate

It produces a high output (logic 1) only when all of its inputs are high; if any input is low (logic 0), the output will also be low.



Figure 5: 2 input AND Gate

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: Truth Table of AND Gate

$$F = A . B$$

OR Gate

Outputs a high signal (logic 1) if at least one of its inputs is high. If all inputs are low (logic 0), only then will the output be low.



Figure 6: 2 input OR Gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Table 3: Truth Table of OR Gate

$$F = A + B$$

NOT Gate

It operates on a single input and a single output. It performs a logical inversion.

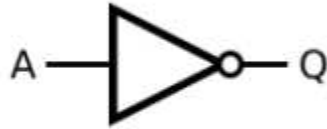


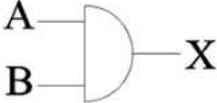
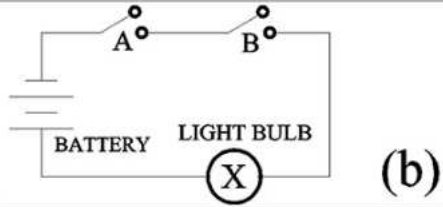
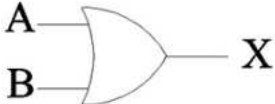
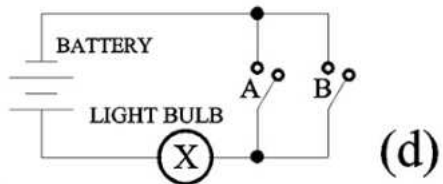
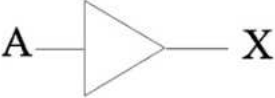
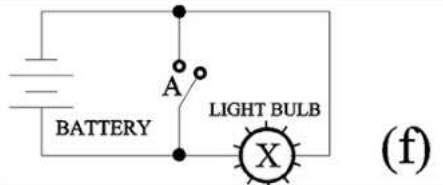
Figure 7: 1 input NOT Gate

Input	Output
0	1
1	0

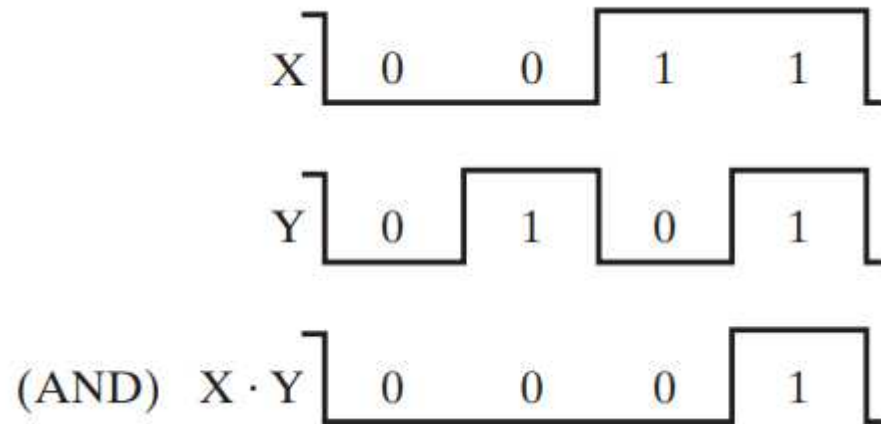
Table 4: Truth Table of NOT Gate

$$F = \bar{A}$$

Equivalent Circuits

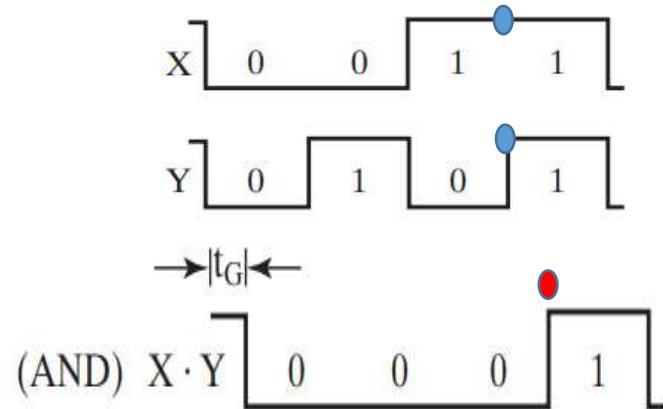
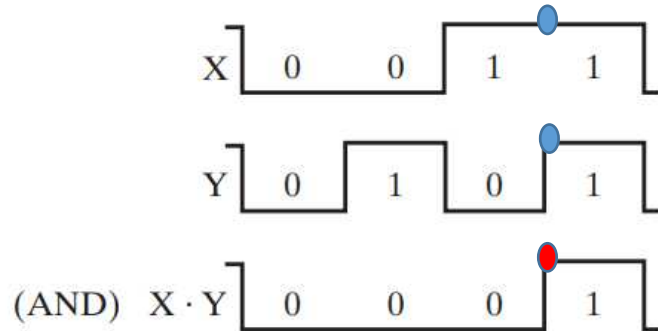
LOGIC GATE (SYMBOL)	ELECTRICAL EQUIVALENT
 AND GATE (a)	 (b)
 OR GATE (c)	 (d)
 NOT GATE (e)	 (f)

Timing Diagram



Gate Delay

Length of time it takes for an input change to result in the corresponding output change



03

Universal Gates

Can construct any other logic gate

NAND Gate

Complement of AND. Only Low when all inputs are high.



Figure 8: 2 input NAND Gate

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Table 5: Truth Table of NAND Gate

$$F = \overline{A \cdot B}$$

NOR Gate

Complement of OR. Only High when all inputs are low.



Figure 10: 2 input NOR Gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Table 7: Truth Table of NOR Gate

$$F = \overline{A + B}$$

04

Exclusive Gates

True only under specific conditions of exclusivity

XOR Gate

Odd 1 selector



Figure 11: 2 input XOR Gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Table 8: Truth Table of X-OR Gate

$$F = A \oplus B = \bar{A}B + A\bar{B}$$

X-NOR Gate

Even 1 selector



Figure 12: 2 input X-OR Gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

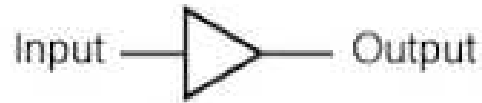
Table 9: Truth Table of NOR Gate

$$F = \overline{A \oplus B} = A \odot B = (A \cdot B) + (\overline{A} \cdot \overline{B})$$

Buffer

A type of logic gate that amplifies a signal without changing its logic level.

"Buffer" gate



Input	Output
0	0
1	1

Thank You !!

Feel free to ask any questions