**CHX002**

**DDRPHY**

**Specification**

**V0.7**

Revision History

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Rev #** | **Status\*** | **Date** | **Author** | **Reason for change/description** |
| V0.1 | D | 2016/12/1 | Martin Si | Draft version.  Copy from T16\_CMT003\_DDRPHY BYTE Spec V05.docx.  Mainly change is:   1. DCLK structure from PLL to different BYTE |
| V0.2 | U | 2017/3/9 | Martin Si | Draft version. Based on T16\_CMT002\_DDRPHY BYTE Spec V08.docx.  1. Modify DDR\_BYTECLK\_BUF\_S24 description and clock structure in part 2.3  2. Delete Package description in part 6.4  3. update Bump map  4. ~~add new input pin for latch mode test: LATCHUP\_NDTREE\_N~~  5. add new input pin for tuning feedback delay: DLL\_FBDLY2~0  6. add frequency change note in chapter 5.6  7. add new input pin for ODT dynamic enable (page 30) : LEADINGOE\_X\_ODT & LEADINGOE\_X\_ODT\_X4  8. change LEADINGOE\_X & LEADINGOE\_X\_X4 for COMPPD dynamic enable only |
| V0.3 | U | 2017/7/18 | Martin Si | 1. separate DRVMODE\_P & DRVMODE\_N of DQ/DQS pad,  delete pin:  DRVMODE\_P2~0  DRVMODE\_N2~0  add pin:  DQ\_DRVMODE\_P2~0  DQ\_DRVMODE\_N2~0  DQS\_DRVMODE\_P2~0  DQS\_DRVMODE\_N2~0 |
| V0.4 | U | 2017/7/21 | Martin Si | 1. Add pin VREF\_MODE2 to separate low/high 4 bit VREFC\_CTRL |
| V0.5 | U | 2017/8/10 | Martin Si | 1. delete pin  DCLK & DCLK800\_IN  VCDL\_SRCTRL1~0 & VCDL\_SFCTRL1~0  2. add pin for input clock  DCLKP & DCLKN  DCLKP\_EN & DCLKN\_EN  DCLK800P & DCLK800N  DCLK800P\_EN & DCLK800N\_EN  BUFRX\_BIASEN  BUFRX\_PTATEN  BUFRX\_DIGBUFEN  BUFRX\_IBP100U\_IN\_0  BUFRX\_IBP100U\_IN\_1  BUFRX\_IBP100U\_OUT\_0  BUFRX\_IBP100U\_OUT\_1  3. add pin for debug  DCLKOP\_OUT  DCLKD\_OUT  DCLKS\_OUT  DCLKDSI\_OUT  DQSN\_OUT  4. add pin for Clock Duty Tuning  DCLK1600\_SRCTRL1~0  DCLK1600\_SFCTRL1~0  DCLK800\_SRCTRL1~0  DCLK800\_SFCTRL1~0  DCLKO\_SRCTRL1~0  DCLKO\_SFCTRL1~0  DCLKOP\_SRCTRL1~0  DCLKOP\_SFCTRL1~0  DCLKD\_SRCTRL1~0  DCLKD\_SFCTRL1~0  DCLKS\_SRCTRL1~0  DCLKS\_SFCTRL1~0  DCLKDSI\_SRCTRL1~0  DCLKDSI\_SFCTRL1~0  5. add reserved pin  DDRPHY\_REV15~DDRPHY\_REV0 |
| V0.6 | U | 2017/9/8 | Martin Si | 1. add output pin:  DDRPHY\_DBGOUT15~0  2. change pin description:  DDRPHY\_REV0 |
| V0.7 | U | 2017/11/15 | Martin Si | 1. modify pin description  DDRMODE1/0  DDRPHY\_REV 0/1/2 & 4/5/6  2. add debug table in DDRPHY\_DBGOUT description  3. modify external pin of VCDL Loop (DDRPHY\_REV0/1/2)  4. update internal constraint table in chapter 5.2.4 & 5.2.2  5. update delay description and add clock balance requirement in Part 2.1  6. update clock domain transfer margin table in 2.2  7. update DDR\_BYTECLK\_BUF structure in 2.3 |
|  |  |  |  |  |
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|  |  |  |  |  |

\*Statuses include: D: Draft, P: Pending review/frozen, U: Update needed, A: Approved

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# Introduction

## Features

- DDRPHY Data & strobe supports for:

- DDR4 X8 1600/1866/2133/2400/2666/3200

- DDR4 X4 1600/1866/2133/2400/2666/3200

- DDR4L X8 1600/1866/2133/2400/2666/3200

- DDR4L X4 1600/1866/2133/2400/2666/3200

- Transmitter

- Programmable clock phase for data transfer between different clock domain

- Programmable TX driver output resistance and drive strength

- Programmable Equalizer

- Programmable DQ TX per-bit-de-skew

- Receiver

- Programmable ODT resistance and ODT strength

- Programmable per-bit VREF value

- Programmable RX CTLE

- Programmable DQ RX per-bit-de-skew

- Programmable RX per-bit Strobe phase

- Separate data sampling by rise/fall edge of strobe

-Loading

-Max support 2S4R (2DIMM and 2Rank per DIMM)

## Process

Process: TSMC 16nm FFC LL (1P13M\_6X2Y2YY2R)

DC Spec

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Corner | Temperature | DVDD | VPP  (DDR4) | VPP  (DDR4L) |
| TT | 85 | 0.8 | 1.2 | 1.05 |
| SS | -40 | 0.72 | 1.14 | 0.945 |
| SS | 125 | 0.72 | 1.14 | 0.945 |
| FF | -40 | 0.88 | 1.26 | 1.155 |
| FF | 125 | 0.88 | 1.26 | 1.155 |

## Related Documents

1. DDR\_BYTECLK\_BUF\_S24 Specifications
2. T16 CHX002 DDR\_BYTECLK\_BUF layout guide
3. T16 CHX002 DDR\_PAD Specifications
4. T16 CHX002 PLLIN\_COMP\_ESD Specifications
5. T16 CHX002 VCDL\_CA Specifications
6. T16 DDR Bump Map & Whole Chip Bump map
7. CHX002 Pinlist

# DDR Top-Level Architecture

## DDR Clock Structure Diagram

There are 2 PLL in DDR system and REF clock is their reference clock.

PLLIN will output 1600MHz clock. PLLIN output clock to DRAMC core logic clock tree CTS delay is t1(<1ns) and to PLLIN feedback clock tree delay is also t1. Low frequency jitter in PLLIN bandwidth will be filtered between REF、PLLIN FB and DRAMC leaf clock.

PLLINDDR will output 1600MHz to DDRPHY and DDRIO logic near PHY. PLLINDDR output clock will be balanced through all byte DDRPHY by circuit design and its clock tree delay is t2 (delay~1ns). 1600M clock will be divided by 2 and sample signals from DRAMC in 800M clock domain, the divided clock tree delay is t3 (~100ps). PLLINDDR feedback clock tree delay is t2+t3 (>1ns). Low frequency jitter in PLLINDDR bandwidth will be filtered between REF、PLLINDDR FB and DDRPHY clock.

In the picture below, all the clock phase with red point will be aligned to same clock phase t0.



目前CMT003/CHX002的PLL 和clock structure 修改方案如下。黄色的粗线和绿色的线是需要circuit 做tree的，其他是APR tree。

1. PLLIN CKOUT1 1.6G output, CKOUT2 800M output 给logic用，feedback 800M clock, APR tree t1 feedback 长齐。
2. PLLINDDR CKOUT1 1.6G output, CKOUT2 800M output，由circuit 完全一直长到PHY的input，然后PHY 分别output 两个1.6G 和800M clock。这两个clock要求严格balance，skew控制在15+20ps内。这两个clock的绝对latency t2尽量小，在PLL内部和feedback t2 做balance。
3. T3是PHY output的APR tree，100ps左右，和PLLDDR 800M feedback外面的t3 balance。
4. DIO的逻辑需要经过下面clock domain的转换：
   1. PLLIN 800M -> PLLINDDR 800M 1/2T转换(follow Part 2.2.1)
   2. PLLINDDR 800M-> PLLINDDR 1600M 转换
   3. PLLINDDR 1600M -> PHY VCDL DCLKO 转换(follow Part 2.2.2)

5. Balance requirement

表格中所有的t3需要在TT、SS、FF下尽可能的balance, 总delay在100ps左右。如果不能meet各个corner下都balance，TT的优先级最高

## DDR clock jitter tolerance margin

### PLLIN and PLLDDR margin

|  |  |  |  |
| --- | --- | --- | --- |
| Item | Description | setup | hold |
| phase jitter | PLLIN and PLLDDR 1600M output phase jitter +/-120ps | 120 | 120 |
| t1 CTS jitter +/-80ps @2ns  (forward+feedback CTS Jitter included) | 80 | 80 |
| t2+t3 CTS jitter +/-25ps @500ps | 25 | 25 |
| Period Jitter | PLL output 15ps @1600M，21ps @ 800M(divided clock) | 21 | 0 |
| t1 CTS Jper 20ps @2ns | 20 | 0 |
| t2 CTS Jper 5ps @500ps | 5 | 0 |
| OCV | 2.1% on launch clock cell  2.1% on capture clock cell 7% on clock net  (Worst case t1 2ns, average cell and net 4.5%, DRAMC leaf t1 OCV and PLLIN feedback OCV) | 200 | 0 |
| 37ps clock uncertainty | 37 | 0 |
| 4.8% on launch clock cell  4.8% on capture clock cell  10% on clock net  (best case t1 1ns, average cell and net 7.5%, DRAMC leaf t1 COV and PLLIN feedback OCV) | 0 | 150 |
| 38ps clock uncertainty | 0 | 38 |
| SUM2 |  | 508 | 413 |

Clock tree requirement:

* + - 1. t0 may be separated to 2 parts. Circuit will do the clock tree to DRAMC core area boundary and to each DDRPHY area boundary in order to reduce t0 total delay. DRAMC internal clock tree will be done by BE tool.
      2. t2 path use M13 to transfer DDRPHY clock. Because of big buffer size, enough de-cap should be surrounded and good power connection is must.

### DDRPHY DCLK\_OUT to DCLKO margin

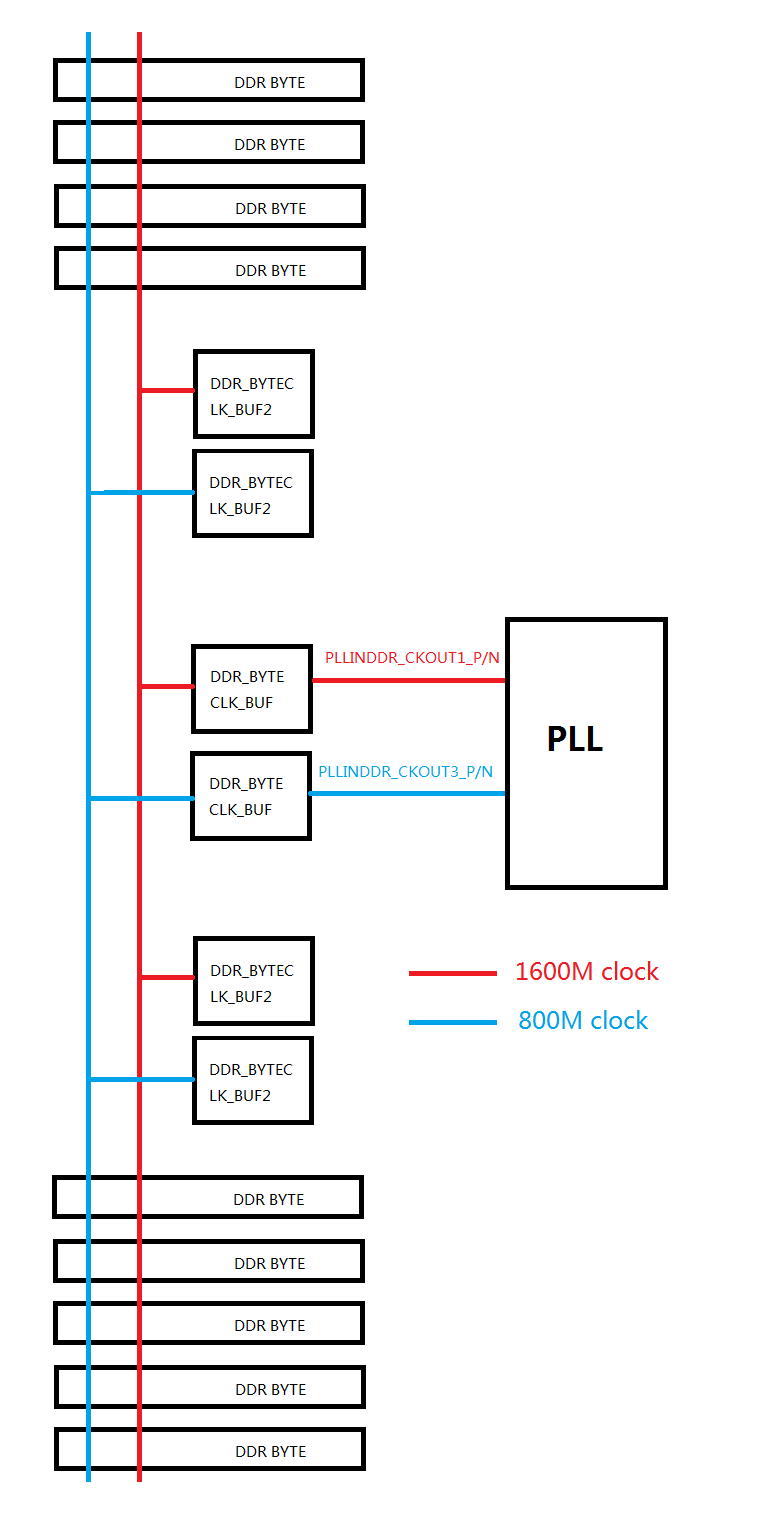
|  |  |  |  |
| --- | --- | --- | --- |
| Item | Description | setup | hold |
| phase jitter | ±20p（PLL高频）±10p（VCDL） | 30 | 30 |
| Period Jitter | ±15p（PLL）±5p（CTS）±10p（VCDL+PI） | 30 | 0 |
| Clock skew | ±5p | 5 | 5 |
| Phase skew  DCLKO和理想PH phase之间的skew | ±20p | 20 | 20 |
| Margin | ±25p | 25 | 25 |
| STA uncertainty |  | 110 | 80 |

### DDRPHY DCLKO and TXCLKD/S internal margin

|  |  |  |  |
| --- | --- | --- | --- |
| Item | Description | setup | hold |
| phase jitter | ±20p（PLL高频）±10p（VCDL） | 30 | 30 |
| Period Jitter | ±15p（PLL）±5p（CTS）±10p（VCDL+PI） | 30 | 0 |
| Clock skew | ±5p | 5 | 5 |
| Phase skew  DCLKO/DCLKD 和理想PH phase之间的skew | ±20p | 20 | 20 |
| Margin | ±25p | 25 | 25 |
| STA uncertainty |  | 110 | 80 |

## CHX002 DDR\_BYTECLK\_BUF\_S24

In CHX002, 6 DDR\_BYTECLK\_BUF per channel is used. PLL output clock is buffered (DDR\_BYTECLK\_BUF) to drive all CA BYTE via M13, then 4 repeater buffer (DDR\_BYTECLK\_BUF2 in below picture) is introduced to drive all data BYTE. Red/Blue path in picture is 1600M & 800M clock for DDRPHY.



# DDRPHY Architecture

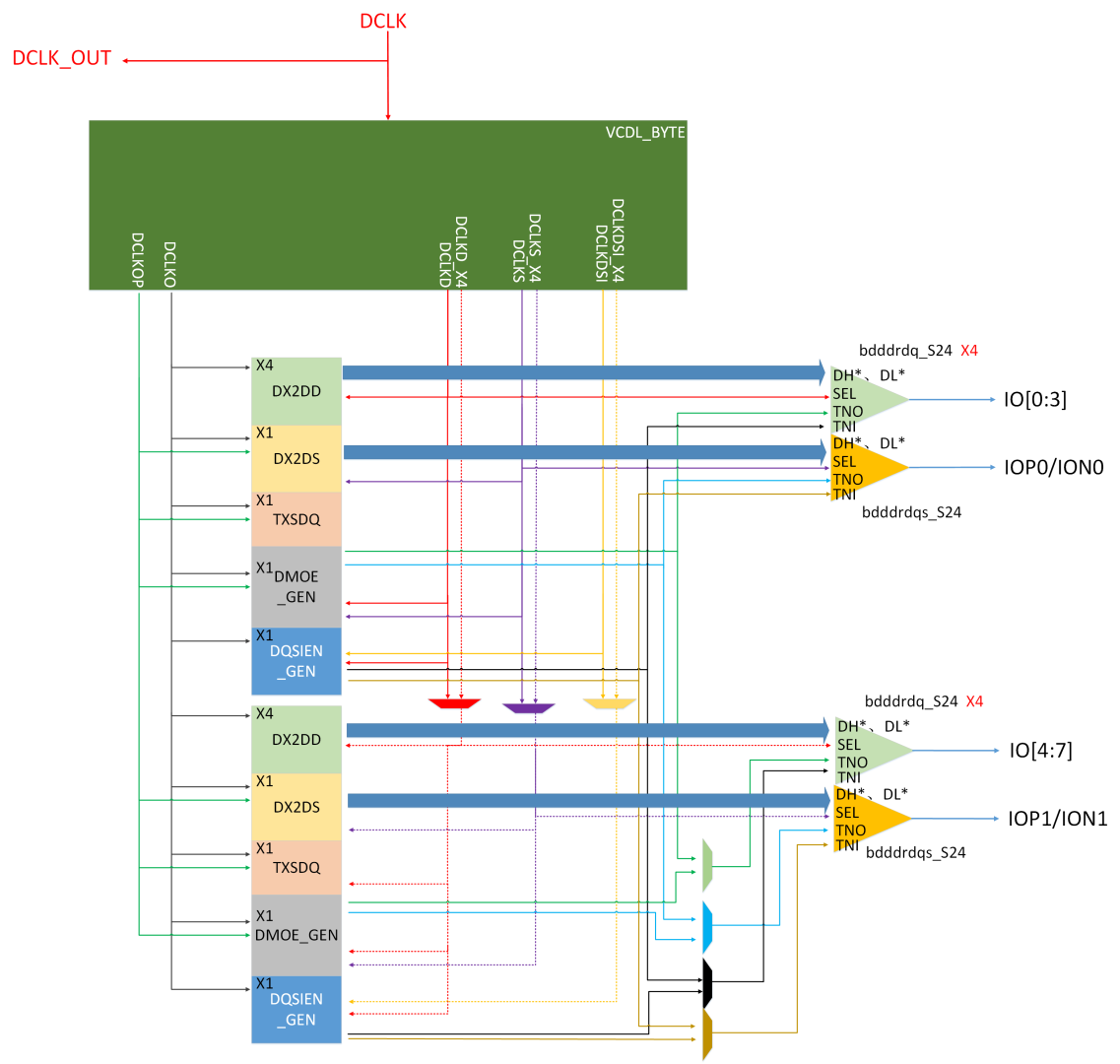
## DDRPHY IP List

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Group | Basic IP name | Size  (before shrink) | Number in PHY | Note |
| Analog | VCDL\_BYTE\_S24 | 606\*200 | 1 | TX DQS/DQ clock |
| DDRCKG\_DDRCLK\_S24 | 606\*50 | 1 | Clock tree balance |
| bdddrdq\_S24 | 44.976\*500 | 8 | DQ pad |
| bdddrdqs\_S24 | 89.952\*500 | 2 | DQS pad |
| padVCC4\_MEM\_S24 | 44.976\*500 | 1 | VCC pad |
| Cap Filler | 21.312\*500 | 1 |  |
| Digital | DX2DD |  | 8 | TX data |
| DX2DS |  | 2 | TX DQS |
| TXSDQ |  | 2 | TX data select |
| DMOE\_GEN |  | 2 | TX output enable |
| DQSIEN\_GEN |  | 2 | RX input enable |
| RXDIO |  | 8 | RX data |



## DDRPHY Clock Scheme

### TX clock scheme

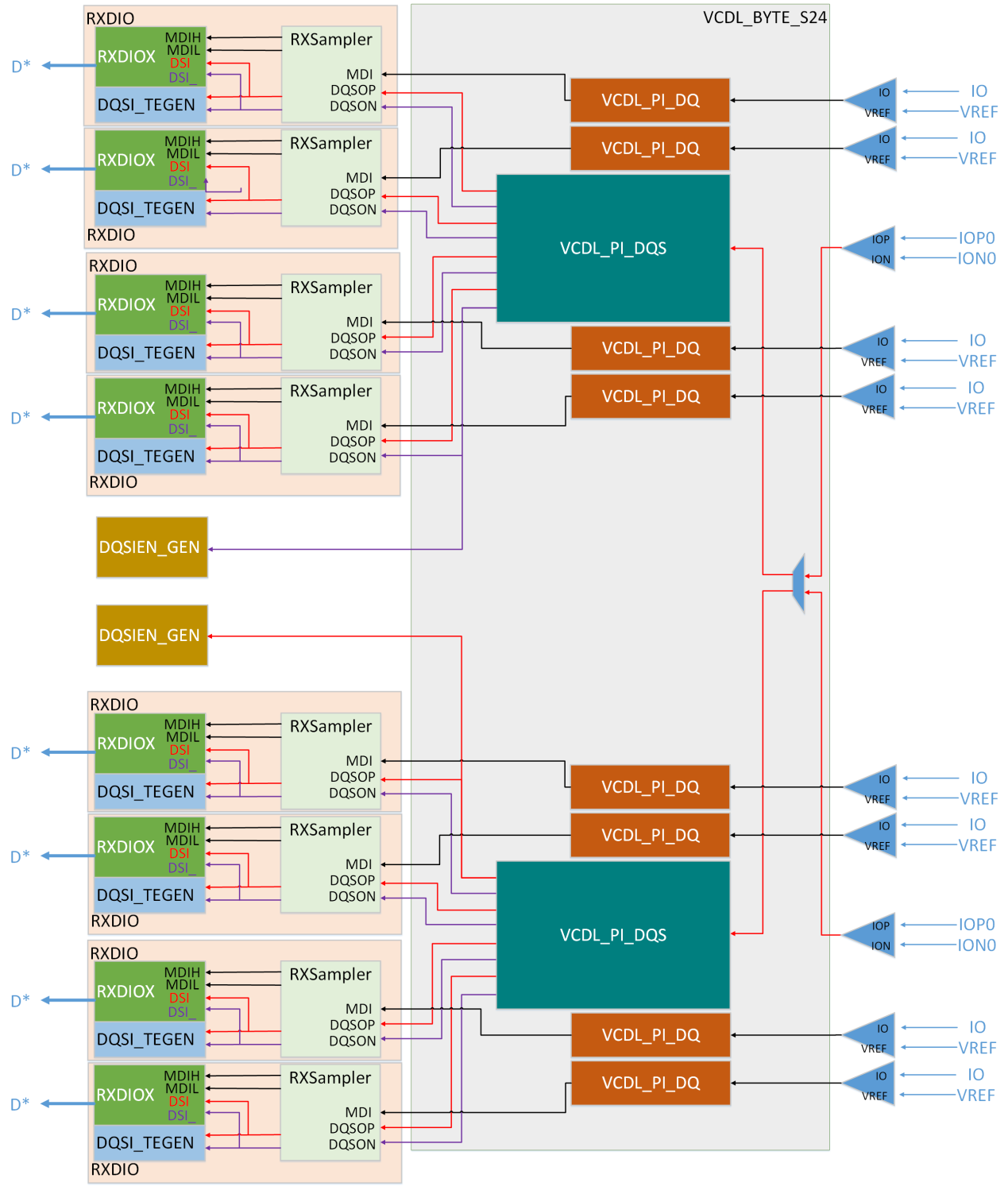


Note:

* + - 1. VCDL\_BYTE\_S24 input clock frequency is full speed DDR clock
      2. All clock generated by VCDL\_BYTE\_S24 is full speed DDR clock with programmable 64 phase, including DCLKO、DCLKOP、DCLKD、DCLKS、DCLKDSI、DCLKD\_X4、DCLKS\_X4 and DCLKDSI\_X4
      3. MD\* inputted to DX2DDs is sampled at DCLKO falling edge by external logic IPs. Then DX2DD & DX2DS capture data by DCLKO rising edge.
      4. Skew and jitter requirement between different clock please refer to chapter on timing
      5. Per-Bit-De-skew is composed by bdddrdq, not in DDRCKG\_DDRCLK

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| VCDL\_BYTE\_S24 output clock to DIOs list | | | | | |
| Clock Name  DIO Name | DCLKO | DCLKOP | DCLKD  &  DCLKD\_X4 | DCLKS  &  DCLKS\_X4 | DCLKDSI  &  DCLKDSI\_X4 |
| DX2DD | Y |  | Y |  |  |
| DX2DS | Y | Y |  | Y |  |
| TXSDQ | Y | Y |  |  |  |
| DMOE\_GEN | Y | Y | Y | Y |  |
| DQSIEN\_GEN | Y |  | Y |  | Y |

### RX Clock Scheme



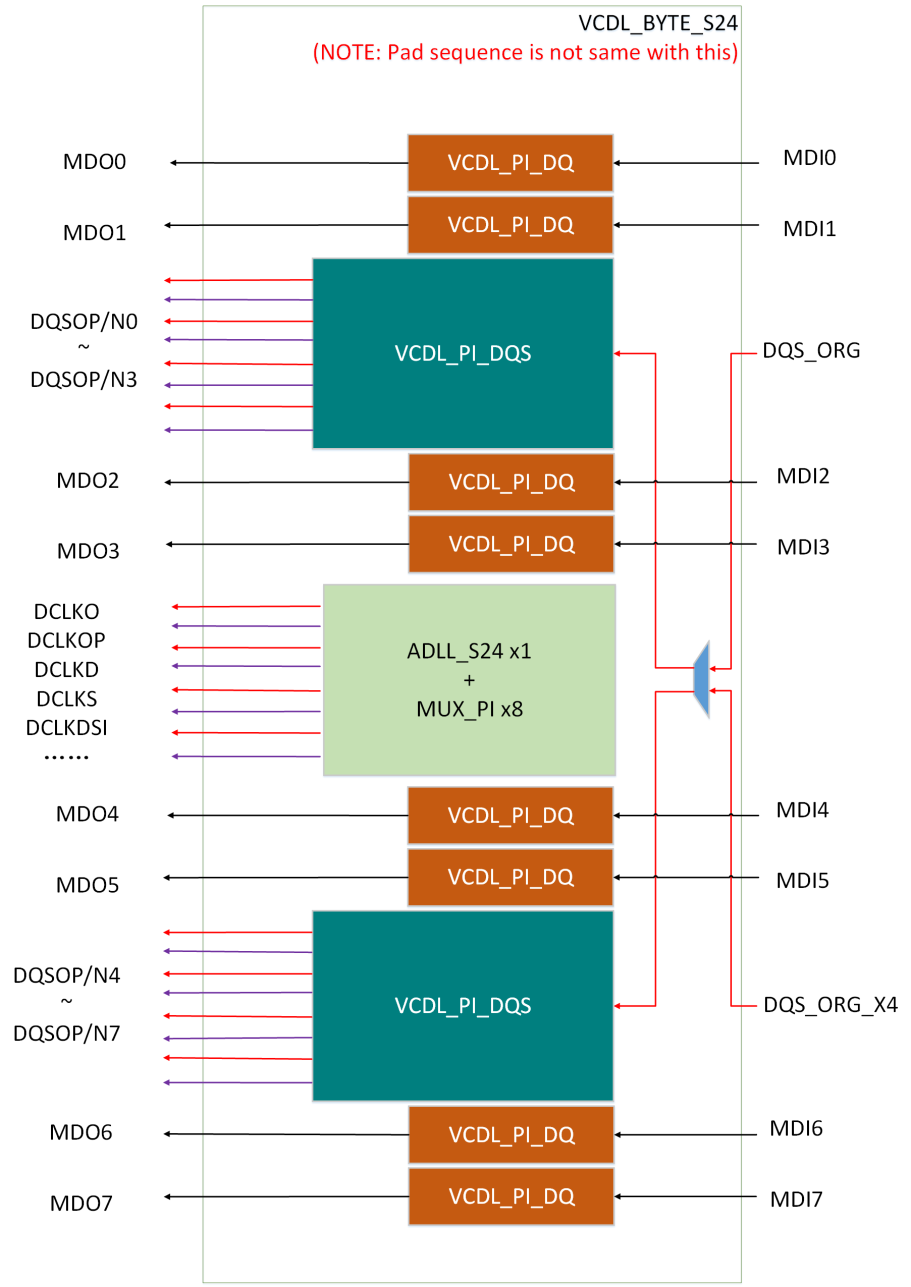
Note:

* + - 1. DQSOP\*/DQSON\* for each RXSampler is not of same delay with other RXSampler.
      2. Cell TNI\_Detector is included in bdddrdqs\_S24
      3. 2 VCDL\_PI\_DQS will operate in either X8 or X4 mode, which means connection between RXDIO\* to bdddrdq\_S24\* could not be changed in different X8/X4 mode.
      4. 2 DQSIEN\_GEN output signal: TNID & TNIS to all DQ/DQS pad input is of same delay.

## DDRPHY Block Description

### VCDL\_BYTE\_S24

VCDL\_BYTE\_S24 is composed of ADLL, 8 MUX\_PI, 8 VCDL\_PI\_DQ, 2 VCDL\_PI\_DQS and other basic cell. ADLL+MUX\_PI(8) would generate 8 clock with 64 phase tunable for DIOs. Both VCDL\_PI\_DQS will work for X8 or X4 mode. And path from DQS\_ORG/DQS\_ORG\_X4 to each VCDL\_PI\_DQS input is balanced.

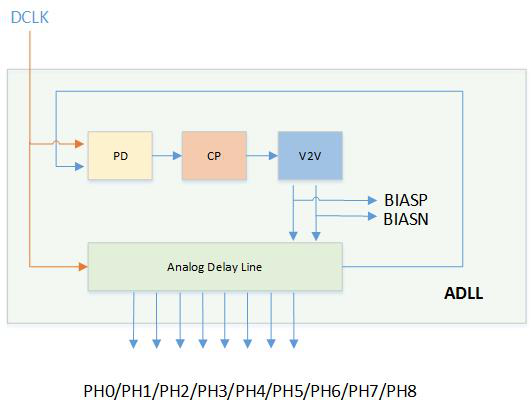


#### ADLL\_S24

ADLL is composed of several basic cells, such as phase detector (PD), charge pump (CP), v2v cell (V2V), analog delay line, and phase interpolator (PI). In general, there is one ADLL in 8’bit DDRPHY.

PD check the phase difference of input clock DCLK and feedback clock output from delay line in ADLL loop, then generate UP/DN signal for CP to increase/decrease the analog delay line control signal: BIASP & BIASN.

1. Total 8 full speed clock with 45℃ phase difference with each adjacent clock generated by ADLL will be applied to all TX/RX clock PI
2. Analog signal bus: BiasP/BiasN will be used for RX path VCDL\_PI\_DQS and VCDL\_PI\_DQ analog delay line too.



Note:

1. When DLL\_LOCKOK rise to high, it means the delay value of delay line chain is equal to one cycle of DCLK.
2. DLL\_CKRANGE pin should follow DDR work frequency.
3. DLL\_REFDLY is used to tuning the VCDL chain delay value.

#### MUX\_PI

MUX\_PI is used to generate clock with 64 programmable phase. Each MUX\_PI need 9 phase input clock as below picture from phase 0 to phase 360℃. Then 8 phase will be interpolated via either 2 adjacent clock. So each MUX\_PI output clock phase can be tuned among 64 step by setting PH\_\*<5:0>, one step is T/64. For example, below picture illustrates how to generate one phase between 4T/8 and 5T/8, and any clock from 33T/64~39T/64 can be output of MUX\_PI according to their setting.

Phase 0T/8 lrhhhflllrhhhflllrhhhfll

Phase 1T/8 llrhhhflllrhhhflllrhhhfl

Phase 2T/8 lllrhhhflllrhhhflllrhhhf

Phase 4T/8 llllrhhhflllrhhhflllrhhh

Phase 5T/8 lllllrhhhflllrhhhflllrhh

Phase 6T/8 llllllrhhhflllrhhhflllrh

Phase 7T/8 lllllllrhhhflllrhhhflllr

Phase 8T/8 llllllllrhhhflllrhhhflll

Phase 4T/8 lrhhhhhhhhhhhhhhhhhhhhh

Phase 33T/64 llrhhhhhhhhhhhhhhhhhhhh

Phase 34T/64 lllrhhhhhhhhhhhhhhhhhhh

Phase 35T/64 llllrhhhhhhhhhhhhhhhhhh

Phase 36T/64 lllllrhhhhhhhhhhhhhhhhh

Phase 37T/64 llllllrhhhhhhhhhhhhhhhh

Phase 38T/64 lllllllrhhhhhhhhhhhhhhh

Phase 39T/64 llllllllrhhhhhhhhhhhhhh

Phase 5T/8 lllllllllrhhhhhhhhhhhhh

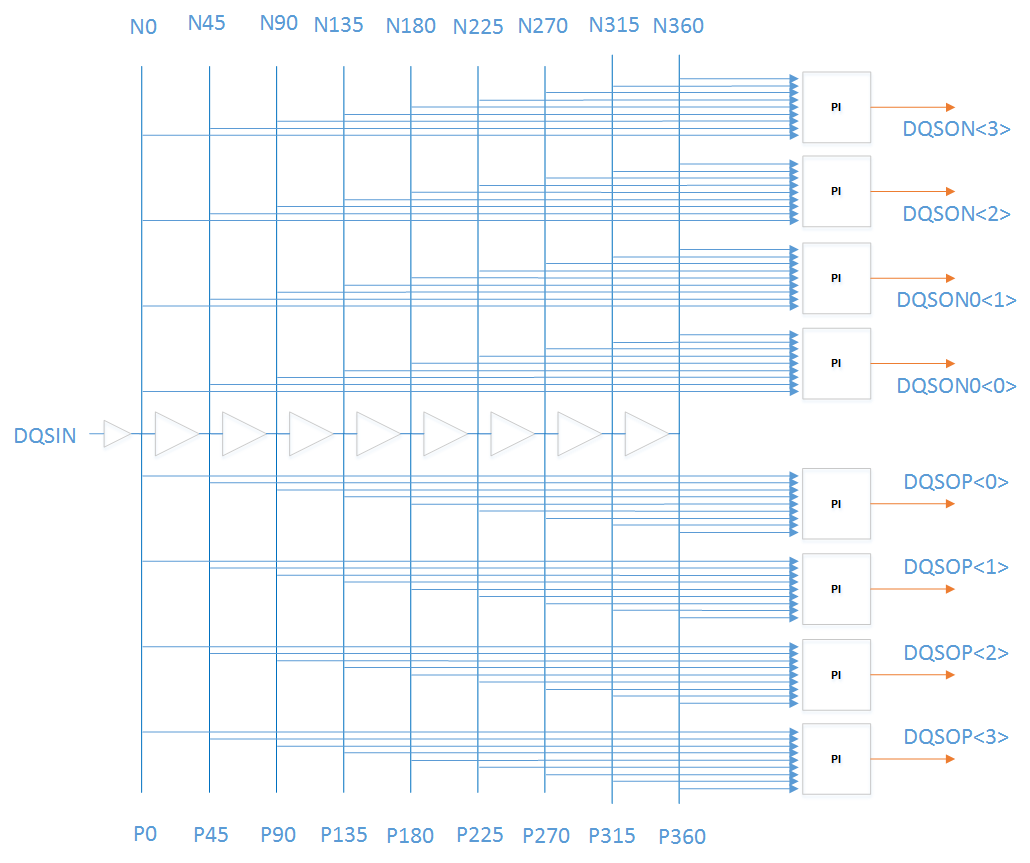
#### VCDL\_PI\_DQS\_S24

VCDL\_PI\_DQS is composed of VCDL (voltage controlled delay line) chain and several MUX\_PI for DQSOP\* and DQSON\*, which is input clock of RXSampler in RXDIO.

VCDL can work only after DLL\_LOCKOK rise to high. The delay value of each VCDL cell is T/8, controlled by BiasP & BiasN from ADLL. There are total 8 VCDL cell and 9 clock from phase 0 to phase 360℃ by step 45℃ would be generated as input clock of all PI in VCDL\_PI\_DQS.

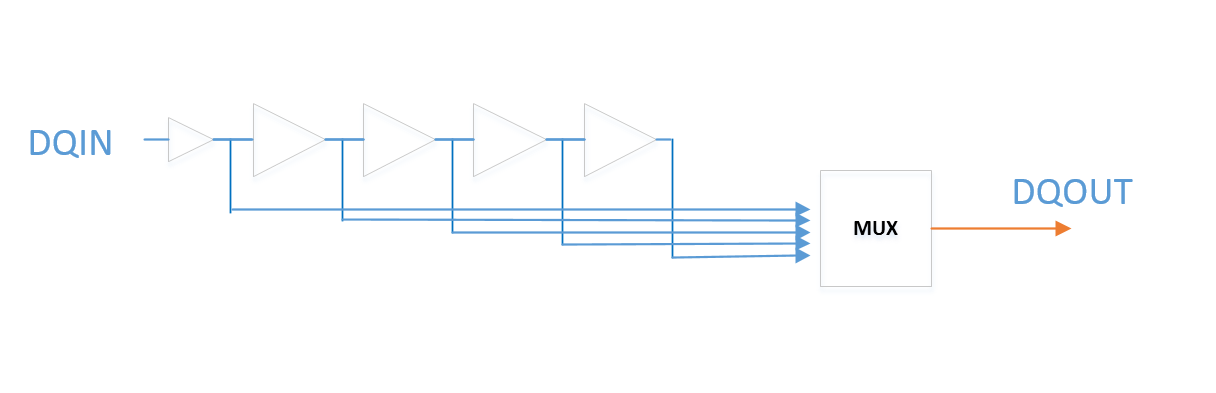
Each PI would generate corresponding clock with phase programmable range from 0 to 1T by step T/64. And RX work range of each MUX\_PI may diff with other.

There are 8 MUX\_PI in one VCDL\_PI\_DQS\_S24, and total 16 MUX\_PI for RX path in one DDRPHY.

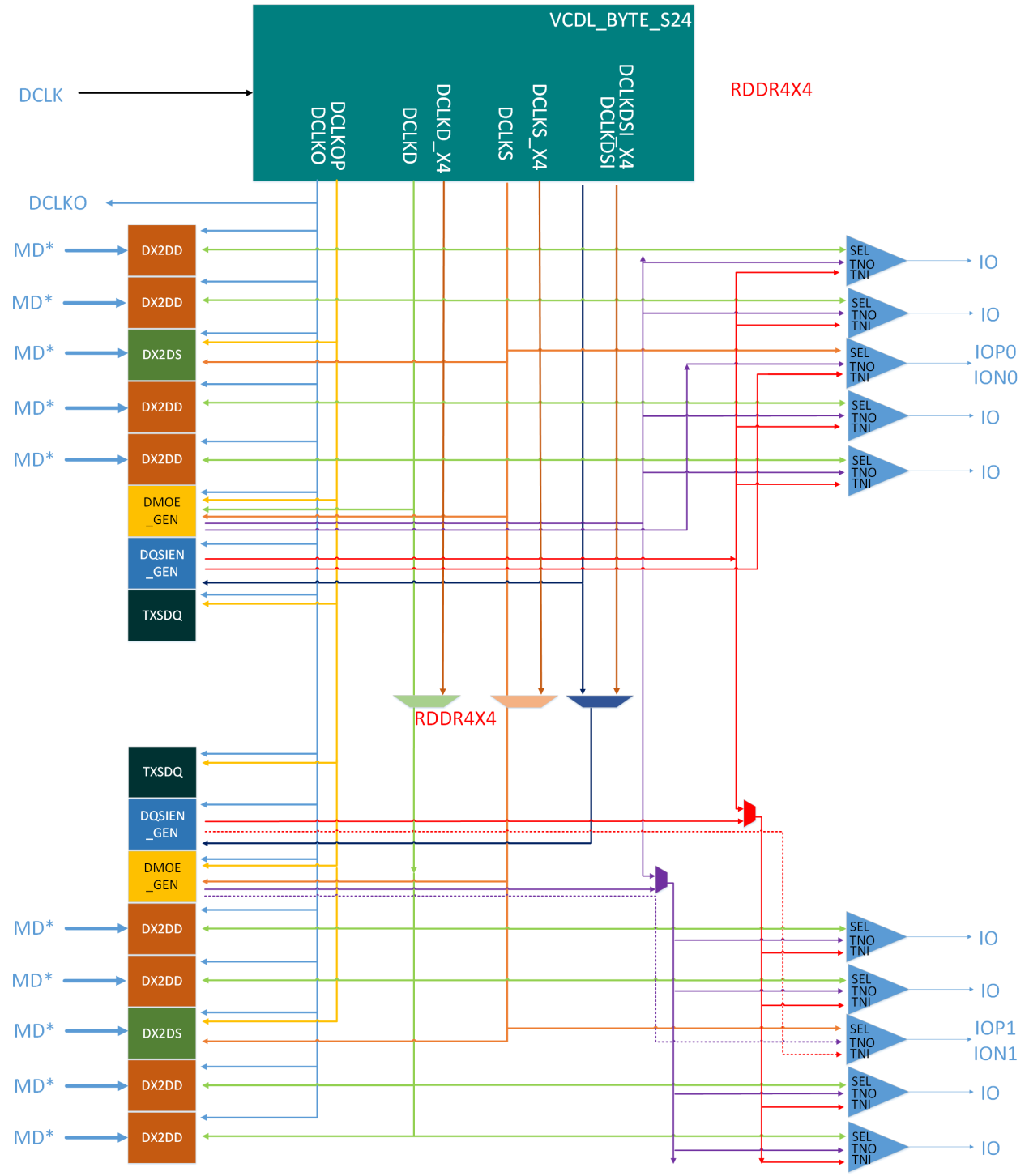


#### VCDL\_PI\_DQ\_S24

VCDL\_PI\_DQS is composed of VCDL chain and MUX, which is used to coarse tuning de-skew between different DQ in one BYTE. DQ can delay by 5 setting, which is 0,T/8,T/4,3T/8, and T/2.



### DDRCKG\_DDRCLK\_S24



### Logic DIOs

#### TXSDQ



#### DX2DD

#### DX2DS



#### DMOE\_GEN



#### DQSIEN\_GEN

#### RXDIO

### DDRIO

DDRIO list as below, and please refer to T16 CHX002 DDR PAD spec\* for detail.

Bdddrdq\_S24 ( total 8)

bdddrdqs\_S24 (total 2)

padVCC4\_MEM\_S24 (total 1)

# DDRPHY Interface List

## External DC Supply

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Domain | I/O | Description |
| DVDD | Core | Power | Core power supply |
| DVSS | Ground | Ground | Ground for core & IO & RVPP domain |
| VPP | VPP | Power | IO pad power supply, typical 1.2V for DDR4 & 1.05V for DDR4L |

## External Signal Pins

### BUFRX for clock

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Power Domain | I/O | Description |
| DCLKP  DCLKN | CORE | I | Input full speed differential clock from PLL, 800MHz~1600MHz |
| DCLK800P  DCLK800N | CORE | I | Input half speed differential clock from PLL  400MHz~800MHz |
| DCLKP\_EN  DCLKN\_EN | CORE | I | DCLKP & DCLKN enable  1: enable DCLKP & DCLKN(default)  0: disable DCLKP & DCLKN |
| DCLK800P\_EN  DCLK800N\_EN | CORE | I | DCLK800P & DCLK800N enable  1: enable DCLK800P & DCLK800N(default)  0: disable DCLK800P & DCLK800N |
| DCLK1600\_SRCTRL1  DCLK1600\_SRCTRL0  DCLK1600\_SFCTRL1  DCLK1600\_SFCTRL0 | Core | I | Duty tuning for DCLK1600 input clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| DCLK800\_SRCTRL1  DCLK800\_SRCTRL0  DCLK800\_SFCTRL1  DCLK800\_SFCTRL0 | Core | I | Duty tuning for DCLK800 input clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| BUFRX\_BIASEN | CORE | I | Enable DCLKP/N & DCLK800P/N bias current  1: enable(default)  0:disable |
| BUFRX\_PTATEN | CORE | I | select current of PTAT or BUFRX\_IBP100U\_IN  1: PTAT current  0: BUFRX\_IBP100U\_IN\_0/1 current |
| BUFRX\_DIGBUFEN | CORE | I | DCLKP/N & DCLK800P/N mode  0: analog mode(default)  1: digital mode |
| BUFRX\_IBP100U\_IN\_0  BUFRX\_IBP100U\_IN\_1 | CORE | I | 100uA bias current input |
| BUFRX\_IBP100U\_OUT\_0  BUFRX\_IBP100U\_OUT\_1 | CORE | O | 100uA bias current output |
| DDRPHY\_REV15  DDRPHY\_REV14  DDRPHY\_REV13  DDRPHY\_REV12  DDRPHY\_REV11  DDRPHY\_REV10  DDRPHY\_REV9  DDRPHY\_REV8  DDRPHY\_REV7  DDRPHY\_REV3 | CORE | I | DDRPHY\_REV3 & 7~15 Reserved |
| DDRPHY\_REV6  DDRPHY\_REV5  DDRPHY\_REV4 |  |  | Debug signal control.  Refer debug table in DDRPHY\_DBGOUT descrition. |
| DDRPHY\_REV2  DDRPHY\_REV1 | CORE | I | used for de-glitch enable of TX clock phase change ( DCLKO/DCLKOP/DCLKD/DCLKS/DCLKDSI)  REV2:1=11: enable de-glitch, 2T loss  REV2:1=10: enable de-glitch, 1T loss  REV2:1=00: disable de-glitch  REV2:1=01: Reserved  (Same description in VCDL\_BYTE) |
| DDRPHY\_REV0 | CORE | I | Connect to VCDL\_BYTE DLL\_CP\_EN, used to enable bias current advanced by DLL\_EN.  1: always enable bias  0: enable bias only when DLL\_EN=0  (Same description in VCDL\_BYTE) |
| DDRPHY\_DEBUGOUT15  DDRPHY\_DEBUGOUT14  DDRPHY\_DEBUGOUT13  DDRPHY\_DEBUGOUT12  DDRPHY\_DEBUGOUT11  DDRPHY\_DEBUGOUT10  DDRPHY\_DEBUGOUT9  DDRPHY\_DEBUGOUT8  DDRPHY\_DEBUGOUT7  DDRPHY\_DEBUGOUT6  DDRPHY\_DEBUGOUT5  DDRPHY\_DEBUGOUT4  DDRPHY\_DEBUGOUT3  DDRPHY\_DEBUGOUT2  DDRPHY\_DEBUGOUT1  DDRPHY\_DEBUGOUT0 | CORE | O | Debug signal output  Debug table as below. |

|  |  |  |  |
| --- | --- | --- | --- |
|  | DDRPHY\_REV4=1 | DDRPHY\_REV5=1 | DDRPHY\_REV6=1 |
| DDRPHY\_DEBUGOUT15 | TNI\_GATE | TNI\_GATE | TNI\_GATE |
| DDRPHY\_DEBUGOUT14 |  |  | Bit6 TE15 |
| DDRPHY\_DEBUGOUT13 |  |  | Bit6 TE0 |
| DDRPHY\_DEBUGOUT12 |  |  | RSTEN |
| DDRPHY\_DEBUGOUT11 |  | DSODT | MDI6 |
| DDRPHY\_DEBUGOUT10 |  | CMPENDQS | DQSP6 |
| DDRPHY\_DEBUGOUT9 |  | CMPENDQ | DQSN6 |
| DDRPHY\_DEBUGOUT8 |  | DQIEN | DQSIEN\_HEAD2 |
| DDRPHY\_DEBUGOUT7 |  | DSIEN | DQSIEN\_HEAD0 |
| DDRPHY\_DEBUGOUT6 |  | DQODT | DDWPG2 |
| DDRPHY\_DEBUGOUT5 | DL\_DQS of DX2DS |  |  |
| DDRPHY\_DEBUGOUT4 | DH\_DQS of DX2DS |  |  |
| DDRPHY\_DEBUGOUT3 | TNOS of DMOE\_GEN |  |  |
| DDRPHY\_DEBUGOUT2 | TNOD of DMOE\_GEN |  |  |
| DDRPHY\_DEBUGOUT1 | DLO of DX2DD0 |  |  |
| DDRPHY\_DEBUGOUT0 | DHO of DX2DD0 |  |  |

### VCDL\_BYTE

#### ADLL\_S24+MUX\_PI for TX

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Power Domain | I/O | Description |
| DLL\_EN | CORE | I | ADLL enable  DLL\_EN=1, ADLL enable  DLL\_EN=0, ADLL disable |
| DDRPHY\_REV0 | CORE | I | used to enable bias current advanced by DLL\_EN.  1: always enable bias, large power  0: enable bias only when DLL\_EN=0 |
| DDRPHY\_REV2  DDRPHY\_REV1 | CORE | I | used for de-glitch enable of TX clock phase change ( DCLKO/DCLKOP/DCLKD/DCLKS/DCLKDSI)  REV2:1=11: enable de-glitch, 2T loss  REV2:1=10: enable de-glitch, 1T loss  REV2:1=00: disable de-glitch  REV2:1=01: Reserved |
| VCDL\_BYPASS | CORE | I | VCDL\_BYPASS=1: test mode to bypass delay line  VCDL\_BYPASS=0: normal work mode |
| DLL\_CKRANGE2  DLL\_CKRANGE1  DLL\_CKRANGE0 | CORE | I | Select corresponding setting for different DCLK frequency  3’b000~3’b011: reserved  3’b 100:400M~565M  3’b 101:565M~800M  3’b 110:800M~1.13G  3’b 111:1.13G~1.6G |
| DLL\_REFDLY2  DLL\_REFDLY1  DLL\_REFDLY0 | CORE | I | 3 bit delay setting to correct reference clock delay line in ADLL loop  Default: 3’b011 |
| DLL\_FBDLY2  DLL\_FBDLY1  DLL\_FBDLY0 | CORE | I | 3 bit delay setting to correct feedback delay line in ADLL loop  Default: 3’b011 |
| DLL\_V2VSEL2  DLL\_V2VSEL1  DLL\_V2VSEL0 | CORE | I | Tuning voltage range of BIASP/BIASN for analog delay line  Default:3’b100 |
| DLL\_BWSEL1  DLL\_BWSEL0 | CORE | I | Tuning charge current value for charge pump in ADLL to tuning bandwidth  Default:2’b01 |
| DLL\_WEAKLOCK | CORE | I | Weak lock control for lower power. When DLL\_WEAKLOCK asserted, ADLL loop is disabled and BIASP/BIASN will change slow by leakage.  DLL\_WEAKLOCK should be de-assert after given resume time.  DLL\_WEAKLOCK=1, weak lock enable  DLL\_WEAKLOCK=0, weak lock disable  (Note: resume time may be 0.1~1us, not final) |
| DLL\_WEAKLOCK\_GATE | Core | I | Gating DCLK when DLL\_WEAKLOCK enable  DLL\_WEAKLOCK\_GATE=1，gate DCLK  DLL\_WEAKLOCK\_GATE=1，not gate DCLK |
| PH\_DCLKO5  PH\_DCLKO4  PH\_DCLKO3  PH\_DCLKO2  PH\_DCLKO1  PH\_DCLKO0 | CORE | I | Phase setting for output clock: DCLKO  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKOP5  PH\_DCLKOP4  PH\_DCLKOP3  PH\_DCLKOP2  PH\_DCLKOP1  PH\_DCLKOP0 | CORE | I | Phase setting for output clock: DCLKOP  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKD5  PH\_DCLKD4  PH\_DCLKD3  PH\_DCLKD2  PH\_DCLKD1  PH\_DCLKD0 | CORE | I | Phase setting for output clock: DCLKD  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKD5\_X4  PH\_DCLKD4\_X4  PH\_DCLKD3\_X4  PH\_DCLKD2\_X4  PH\_DCLKD1\_X4  PH\_DCLKD0\_X4 | CORE | I | Phase setting for output clock: DCLKD\_X4  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKS5  PH\_DCLKS4  PH\_DCLKS3  PH\_DCLKS2  PH\_DCLKS1  PH\_DCLKS0 | CORE | I | Phase setting for output clock: DCLKS  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKS5\_X4  PH\_DCLKS4\_X4  PH\_DCLKS3\_X4  PH\_DCLKS2\_X4  PH\_DCLKS1\_X4  PH\_DCLKS0\_X4 | CORE | I | Phase setting for output clock: DCLKS\_X4  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKDSI5  PH\_DCLKDSI4  PH\_DCLKDSI3  PH\_DCLKDSI2  PH\_DCLKDSI1  PH\_DCLKDSI0 | CORE | I | Phase setting for output clock: DCLKDSI  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PH\_DCLKDSI5\_X4  PH\_DCLKDSI4\_X4  PH\_DCLKDSI3\_X4  PH\_DCLKDSI2\_X4  PH\_DCLKDSI1\_X4  PH\_DCLKDSI0\_X4 | CORE | I | Phase setting for output clock: DCLKDSI\_X4  6’b000000: Phase 0  ….  6’b111111: Phase 63 |
| PIEN\_DCLKO | CORE | I | Output clock enable: DCLKO |
| PIEN\_DCLKOP | CORE | I | Output clock enable: DCLKOP |
| PIEN\_DCLKD | CORE | I | Output clock enable: DCLKD |
| PIEN\_DCLKD\_X4 | CORE | I | Output clock enable: DCLKD\_X4 |
| PIEN\_DCLKS | CORE | I | Output clock enable: DCLKS |
| PIEN\_DCLKS\_X4 | CORE | I | Output clock enable: DCLKS\_X4 |
| PIEN\_DCLKDSI | CORE | I | Output clock enable: DCLKDSI |
| PIEN\_DCLKDSI\_X4 | CORE | I | Output clock enable: DCLKDSI\_X4 |
|  |  |  |  |
| DLL\_LOCKOK | CORE | O | ADLL loop lock OK flag  DLL\_LOCKOK =1 means ADLL loop lock and output clock is valid  DLL\_LOCKOK =0 means ADLL loop is unlocked and DDRPHY can’t work |
|  |  |  |  |
| DLL\_FALSELOCK\_DEBUG1  DLL\_FALSELOCK\_DEBUG0 | CORE | O | Debug signal for ADLL false lock |
| DLL\_CKPH\_DEBUG8  DLL\_CKPH\_DEBUG7  DLL\_CKPH\_DEBUG6  DLL\_CKPH\_DEBUG5  DLL\_CKPH\_DEBUG4  DLL\_CKPH\_DEBUG3  DLL\_CKPH\_DEBUG2  DLL\_CKPH\_DEBUG1  DLL\_CKPH\_DEBUG0 | CORE | O | Debug clock for ADLL loop clock phase output (high speed) |
| DLL\_CLK1600 | CORE | O | Debug clock for buffered full speed input PLL clock |
| DLL\_CLK800 | CORE | O | Debug clock for buffered half speed input PLL clock |

#### DDRCKG+RX VCDL\_PI\_ DQS + VCDL\_PI\_DQ

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| RDDRX4 | I | Core | DDR X4 mode setting  1’b1 X4 mode  1’b0 X8 mode |
| DCLKO\_SRCTRL1  DCLKO\_SRCTRL0  DCLKO\_SFCTRL1  DCLKO\_SFCTRL0 | I | Core | Duty tuning for DCLKO output clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| DCLKOP\_SRCTRL1  DCLKOP\_SRCTRL0  DCLKOP\_SFCTRL1  DCLKOP\_SFCTRL0 | I | Core | Duty tuning for DCLKOP output clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| DCLKD\_SRCTRL1  DCLKD\_SRCTRL0  DCLKD\_SFCTRL1  DCLKD\_SFCTRL0 | I | Core | Duty tuning for DCLKD output clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| DCLKS\_SRCTRL1  DCLKS\_SRCTRL0  DCLKS\_SFCTRL1  DCLKS\_SFCTRL0 | I | Core | Duty tuning for DCLKS output clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| DCLKDSI\_SRCTRL1  DCLKDSI\_SRCTRL0  DCLKDSI\_SFCTRL1  DCLKDSI\_SFCTRL0 | I | Core | Duty tuning for DCLKDSI output clock  20ps per step @ss -40C as below   |  |  |  |  | | --- | --- | --- | --- | | SRCTRL | SFCTRL | Rise delay | Fall delay | | 11 | 00 | +60 | +0 | | 10 | 00 | +40 | +0 | | 01 | 00 | +20 | +0 | | 00 | 00 | +0 | +0 | | 00 | 01 | +0 | +20 | | 00 | 10 | +0 | +40 | | 00 | 11 | +0 | +60 | |
| PH\_DQ[7:0]\_[2:0] | I | Core | DQ[7:0] per-bit-deskew, coarse tuning  DQ Delay from MDI[7:0] to MDO[7:0] increases by step=T/8 from code 000 to code 100  Code 101~111 reserved |
| PH\_DQS[7:0]P[5:0] | I | Core | DQSOP0[7:0] phase selection, fine tuning  Phase step is T/64 from code 0 to code 6’b111111 |
| PH\_DQS[7:0]N[5:0] | I | Core | DQSON0[7:0] phase selection, fine tuning  Phase step is T/64 from code 0 to code 6’b111111 |
| PIEN\_DQS  PIEN\_DQS\_X4 | I | Core | RX DQS PI enable for X8/X4 mode  1: enable (default)  0: disable |
| MUXEN\_DQ7  MUXEN\_DQ6  MUXEN\_DQ5  MUXEN\_DQ4  MUXEN\_DQ3  MUXEN\_DQ2  MUXEN\_DQ1  MUXEN\_DQ0 | I | Core | RX DQ MUX\_DQ enable for DQ[7:0]  1: enable (default)  0: disable |
| DQSP\_OUT | O | CORE | RX DQSP1 output debug signal |
| DQSN\_OUT | O | CORE | RX DQSN1 output debug signal |

### DIO

#### DCLKO\_OUT

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| DCLKO\_OUT | CORE | O | 64 phase programmable clock to controller near PHY, it is sync with internal clock of TXDIOs |
| DCLK\_OUT | CORE | O | Buffed DCLK to logic |
| DCLK800\_OUT | CORE | O | Buffed DCLK800\_IN to logic |

#### TXSDQ (Number=2)

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| WRDY\_IN WRDY\_IN\_X4 | I | Core |  |

#### DX2DD (Number=8)

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| MDL0\_[7:0] | I | Core |  |
| MDL1\_[7:0] | I | Core |  |
| MDH0\_[7:0] | I | Core |  |
| MDH1\_[7:0] | I | Core |  |
| TESTEN\_7  TESTEN\_6  TESTEN\_5  TESTEN\_4  TESTEN\_3  TESTEN\_2  TESTEN\_1  TESTEN\_0 | I | Core |  |
| TESTIN\_7  TESTIN\_6  TESTIN\_5  TESTIN\_4  TESTIN\_3  TESTIN\_2  TESTIN\_1  TESTIN\_0 | I | Core |  |

#### DX2DS (Number=2)

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| SDHXX\_PRE  SDHXX\_PRE\_X4 | I | Core |  |
| SDLXX\_PRE  SDLXX\_PRE\_X4 | I | Core |  |
| TESTIN\_DQS  TESTIN\_DQS\_X4 | I | Core |  |
| TESTEN\_DQS  TESTEN\_DQS\_X4 | I | Core |  |

#### DMOE\_GEN (Number=2)

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| MDOEDDX MDOEDDX\_X4 | I | Core |  |
| DQSOEDDX\_PRE  DQSOEDDX\_PRE\_X4 | I | Core |  |
| DQWPH1\_X8  DQWPH0\_X8  DQWPH1\_X4  DQWPH0\_X4 | I | Core |  |
| DSWPH1\_X8  DSWPH0\_X8  DSWPH1\_X4  DSWPH0\_X4 | I | Core |  |
| RST\_ | I | Core | RST\_ again，who control？ |
| DRAMDATAOE\_EN | I | Core |  |
| WLVL\_MODE | I | Core |  |
| RDSOLNGPRE1  RDSOLNGPRE0 | I | Core |  |
| DQTESTEN | I | Core | X4 need or not？ |
| DSTESTEN | I | Core | X4 need or not？ |
| TEST\_TNOD | I | Core |  |
| TEST\_TNOS | I | Core |  |

#### DQSIEN\_GEN(Number=2)

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| DQSIEN\_HEAD0X  DQSIEN\_HEAD0X\_X4 | I | Core |  |
| DQSIEN\_HEAD2X  DQSIEN\_HEAD2X\_X4 | I | Core |  |
| LEADINGOE\_X  LEADINGOE\_X\_X4 | I | Core |  |
| LEADINGOE\_X\_ODT  LEADINGOE\_X\_ODT\_X4 | I | Core |  |
| DDWPG2\_X  DDWPG2\_X\_X4 | I | Core |  |
| DSIEN1\_X8  DSIEN0\_X8  DSIEN1\_X4  DSIEN0\_X4 | I | Core |  |
| DMRLEN\_RST\_ | I | Core |  |
| RST\_ | I | Core | 与其他的RST\_是否相同 |
| RDSIEN | I | Core |  |
| RDQIEN | I | Core |  |
| FLOATDSI | I | Core | X4 need or not? |
| FLOATDQI | I | Core | X4 need or not? |
| RCMPEN\_ALWSON | I | Core |  |
| RCMPENDQ\_ON | I | Core |  |
| RCMPENDQS\_ON | I | Core |  |
| RDSODTON | I | Core |  |
| RDQODTON | I | Core |  |
| RODTEN | I | Core |  |
| ATPGEN | I | Core |  |
| ~~LATCHUP\_NDTREE\_N~~ | ~~I~~ | ~~CORE~~ | ~~DQ/DQS COMPPD control in Latch up / NDTREE mode~~  ~~0: DQ/DQS COMPPD=0~~  ~~1: normal read/write mode~~ |

#### RXDIO（Number=8）

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Power Domain | Description |
| DMRLEN\_RST\_ | I | Core |  |
| RXSAMPLER\_EN | I | Core |  |
| CNT\_DQSOPN1  CNT\_DQSOPN0 | I | Core |  |
| RST\_ | I | Core |  |
| LD0F\_b[7:0]  LD1F\_b[7:0]  LD2F\_b[7:0]  LD3F\_b[7:0]  LD4F\_b[7:0]  LD5F\_b[7:0]  LD6F\_b[7:0]  LD7F\_b[7:0] | O | Core |  |
| LD0R\_b[7:0]  LD1R\_b[7:0]  LD2R\_b[7:0]  LD3R\_b[7:0]  LD4R\_b[7:0]  LD5R\_b[7:0]  LD6R\_b[7:0]  LD7R\_b[7:0] | O | Core |  |

### PAD

#### bdddrdq (Number=8)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Signal Name | I/O | Power Domain | Description | |
| DQ\_NS3  DQ\_NS2  DQ\_NS1  DQ\_NS0 | I | core | Four bits driving setting for nmos pulling down  4’b0000 max output resistance  …  4’b1111 min output resistance | |
| DQ\_PS3  DQ\_PS2  DQ\_PS1  DQ\_PS0 | I | core | Four bits driving setting for pmos pulling up  4’b0000 max output resistance  …  4’b1111 min output resistance | |
| FTB\_DET | I | VPP | Feed through SUS mode power down control. TX / RX / ODT all disable, IO high-Z when FTB\_DET=1 | |
| DLY\_DQ[7:0]3  DLY\_DQ[7:0]2  DLY\_DQ[7:0]1  DLY\_DQ[7:0]0 | I | Core | Gray code TX Per-Bit-Deskew setting, total 16 step | |
| IO7  IO6  IO5  IO4  IO3  IO2  IO1  IO0 | IO | VPP | IO port to board | |
| DQ\_DRVMODE\_N2  DQ\_DRVMODE\_N1  DQ\_DRVMODE\_N0 | I | core | 000 | Output pull down 240ohm, Rnom/1 |
| 001 | Output pull down 120ohm, Rnom/2 |
| 010 | Output pull down 80ohm, Rnom/3 |
| 011 | Output pull down 60ohm, Rnom/4 |
| 100 | Output pull down 48ohm, Rnom/5 |
| 101 | Output pull down 40ohm, Rnom/6 |
| 110 | Output pull down 34ohm, Rnom/7 |
| 111 | Reserve |
| DQ\_DRVMODE\_P2  DQ\_DRVMODE\_P1  DQ\_DRVMODE\_P0 | I | core | 000 | Output pull up 240ohm, Rnom/1 |
| 001 | Output pull up 120ohm, Rnom/2 |
| 010 | Output pull up 80ohm, Rnom/3 |
| 011 | Output pull up 60ohm, Rnom/4 |
| 100 | Output pull up 48ohm, Rnom/5 |
| 101 | Output pull up 40ohm, Rnom/6 |
| 110 | Output pull up 34ohm, Rnom/7 |
| 111 | Reserve |
| ODTMODE2 ODTMODE1  ODTMODE0 | I | core | 000 | RODTpu/pd=240ohm, Rnom/1 |
| 001 | RODTpu/pd=120ohm, Rnom/2 |
| 010 | RODTpu/pd=80ohm, Rnom/3 |
| 011 | RODTpu/pd=60ohm, Rnom/4 |
| 100 | RODTpu/pd=48ohm, Rnom/5 |
| 101 | RODTpu/pd=40ohm, Rnom/6 |
| 110 | RODTpu/pd=34ohm, Rnom/7 |
| 111 | Reserve |
| DDRMODE1  DDRMODE0 | I | core | 00 | DDR3 1.35V, Rodt pu & pd both |
| 01 | LPDDR4 1.05V, RODT pd only |
| 10 | DDR4L 1.05V, RODT pu only |
| 11 | DDR4 1.2V, RODT pu only |
| DE1\_EN  DE2\_EN | I | Core | 00 | De\_emphasis disable |
|  | 01 | Two former bit de\_emphasis enable |
| 10 | Former bit de\_emphasis enable |
| 11 | Two former bit de\_emphasis and Former bit de\_emphasis all enable |
| EQ\_SET\_N3  EQ\_SET\_N2  EQ\_SET\_N1  EQ\_SET\_N0 | I | Core | 0000~1000 | DQ TX Pull down emphasis strength  0000 minimum  …  1000 maximum |
| 1001~1111 | Reserved |
| EQ\_SET\_P3  EQ\_SET\_P2  EQ\_SET\_P1  EQ\_SET\_P0 | I | Core | 0000~1000 | DQ TX Pull up emphasis strength  0000 minimum  …  1000 maximum |
| 1001~1111 | Reserved |
| VREF\_SEL | IN | core | NA | VREF selection.  1: VREF\_INT  0: VREF\_EXT  Default:1 |
| NDTREE | In | core | NA | NAND tree enable. (High active) |
| PI[7]  PI[6]  PI[5]  PI[4]  PI[3]  PI[2]  PI[1]  PI[0] | In | core | NA | NAND tree input. |
| PO[7]  PO[6]  PO[5]  PO[4]  PO[3]  PO[2]  PO[1]  PO[0] | Out | core | NA | NAND tree output. |
|  |  |  |  |  |
| BIASEN | In | Core | NA | DQ/DQS RX bias current enable  1: enable (default)  0: disable |
| CTLE\_EN | In | Core | NA | RX EQ enable  1:enable  0:disable |
| CTLE\_TUNE5  CTLE\_TUNE4  CTLE\_TUNE3  CTLE\_TUNE2  CTLE\_TUNE1  CTLE\_TUNE0 | In | Core |  | RX EQ tuning |
| RXMODE1  RXMODE0 | in | Core | 11 | For max Ron and min Rtt in DDR4 |
| 10 | For min Ron and max Rtt in DDR4 |
| 00 | For min Ron and max Rtt in DDR4L |
| 01 | For max Ron and min Rtt in DDR4L |
| ZIT7  ZIT6  ZIT5  ZIT4  ZIT3  ZIT2  ZIT1  ZIT0 | Out | core | NA | Output port to core, for test, driving same as ZI. ZIT=IO when COMPPD=1&TNI=1 ZIT=0 when COMPPD=0 or TNI=0 |
|  |  |  |  |  |
| DDR\_PAD\_INLP | IN | Core | 1 | SEL=1： ZI=DH  SEL=0： ZI=DL |
| 0 | COMPPD=1 & TNI=1： ZI=IO  Else： ZI=0 |
| VREFF[7:0]\_CTRL[3:0] | In | Core | NA | Fine Tuning for per-bit VREF  In X8 mode, VREFF[7:0]\_CTRL[3:0] share same range according to VREFC\_CTRL[5:0], there is 16 step for per-DQ-VREF  In X4 mode,  REFF[3:0]\_CTRL[3:0] share same range according to VREFC\_CTRL[5:0], and REFF[7:4]\_CTRL[3:0] share same range according to VREFC\_CTRL[5:0]\_X4.  Please refer to DDRIO padVCC4\_MEM spec for detail |
| VREF\_EXT | IO | VPP | NA | External VREF from PCB,  which value is 50% VPP |

#### bdddrdqs (Number=2)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin name** | **In/Out** | **domain** | **Value** | **Description** |
| DQS\_NS3  DQS\_NS2  DQS\_NS1  DQS\_NS0 | In | Core | NA | Four bits driving setting for nmos pulling down |
| DQS\_PS3  DQS\_PS2  DQS\_PS1  DQS\_PS0 | In | Core | NA | Four bits driving setting for pmos pulling up |
| EQS\_SET\_N3  EQS\_SET\_N2  EQS\_SET\_N1  EQS\_SET\_N0 | I | Core | 0000~1000 | DQS TX Pull down emphasis strength  0000 minimum  …  1000 maximum |
| 1001~1111 | Reserved |
| EQS\_SET\_P3 EQS\_SET\_P2  EQS\_SET\_P1  EQS\_SET\_P0 | I | Core | 0000~1000 | DQS TX Pull up emphasis strength  0000 minimum  …  1000 maximum |
| 1001~1111 | Reserved |
| DQS\_DRVMODE\_N2  DQS\_DRVMODE\_N1  DQS\_DRVMODE\_N0 | I | core | 000 | Output pull down 240ohm, Rnom/1 |
| 001 | Output pull down 120ohm, Rnom/2 |
| 010 | Output pull down 80ohm, Rnom/3 |
| 011 | Output pull down 60ohm, Rnom/4 |
| 100 | Output pull down 48ohm, Rnom/5 |
| 101 | Output pull down 40ohm, Rnom/6 |
| 110 | Output pull down 34ohm, Rnom/7 |
| 111 | Reserve |
| DQS\_DRVMODE\_P2  DQS\_DRVMODE\_P1  DQS\_DRVMODE\_P0 | I | core | 000 | Output pull up 240ohm, Rnom/1 |
| 001 | Output pull up 120ohm, Rnom/2 |
| 010 | Output pull up 80ohm, Rnom/3 |
| 011 | Output pull up 60ohm, Rnom/4 |
| 100 | Output pull up 48ohm, Rnom/5 |
| 101 | Output pull up 40ohm, Rnom/6 |
| 110 | Output pull up 34ohm, Rnom/7 |
| 111 | Reserve |
| PI\_DQS\_P  PI\_DQS\_N  PI\_DQS\_P\_X4  PI\_DQS\_N\_X4 | In | Core | NA | DQS、DQS\_X4 NAND Tree input |
| PO\_DQS\_P  PO\_DQS\_N  PO\_DQS\_P\_X4  PO\_DQS\_N\_X4 | Out | Core | NA | DQS、DQS\_X4 NAND Tree output |
| IOP  ION | IO | VPP | NA | X4 DQSP/N IO port to board. |
| IOP\_X4  ION\_X4 | IO | VPP | NA | X8 & X4[3:0] DQSP/N IO port to board. |
| ZITP  ZITP\_X4 | Out | core | NA | Output port to core, for test, driving same as ZI. ZITP=IOP when COMPPD=1&TNI=1 ZITP=0 when COMPPD=0 or TNI=0 |
| TNI\_SEL | In | Core | NA | DQS pre-amble calibration range selection:  1: TNI calibration DQS High  0: TNI calibration DQS Low |

#### padVCC4\_MEM (Number=1)

|  |  |  |  |
| --- | --- | --- | --- |
| Pin name | In/Out | domain | Description |
| PD\_BIAS | In | core | Powerdown control of Ibias.  1: enable bias  0: disable bias  Settle time of IBIAS is 100ns. |
| VREFC\_CTRL5  VREFC\_CTRL4  VREFC\_CTRL3  VREFC\_CTRL2  VREFC\_CTRL1  VREFC\_CTRL0 | In | core | VREF coarse control for per-bit-VREF for DQ[7:0] at VREF\_MODE2=0 or DQ[3:0] at VREF\_MODE=1 |
| VREFC\_CTRL5\_X4  VREFC\_CTRL4\_X4  VREFC\_CTRL3\_X4  VREFC\_CTRL2\_X4 VREFC\_CTRL1\_X4 VREFC\_CTRL0\_X4 | In | core | VREF coarse control for per-bit-VREF for DQ[7:4] at VREF\_MODE2=1 |
| VREF\_MODE | In | core | VREF mode selection  1 for coarse mode , step larger  0 for fine mode, step 0.0045V |
| VREF\_MODE2 | In | Core | Low/High 4 bit VREF control mode  1: Low/High 4 bit use separate VREFC\_CTRL5~0  0: Low/High 4 bit use same VREFC\_CTRL5~0 |
| VREF\_OVERLAP | In | core | Overlap mode for VREF calibration |
| VREF\_OVERLAP\_X4 | In | core | Overlap mode for VREF calibration |
| PD\_VREF | In | Core | Powerdown control of VREF  1: enable VREF  0: disable VREF  Settle time of VREF is 1us. |
| VREF\_TST2  VREF\_TST1  VREF\_TST0 | In | Core | VREF for test  000: VREFC\_H  001: VREFC\_L  010: VPP  011: DVDD  100: DVSS |
| IREF\_TST1  IREF\_TST0 | in | Core | IREF for test  01: IBN  10: IBP |
| VREF\_TST\_EN | in | Core | Test mode enable  1:enable |

## Internal Connection

### DDRPHY TXDIO

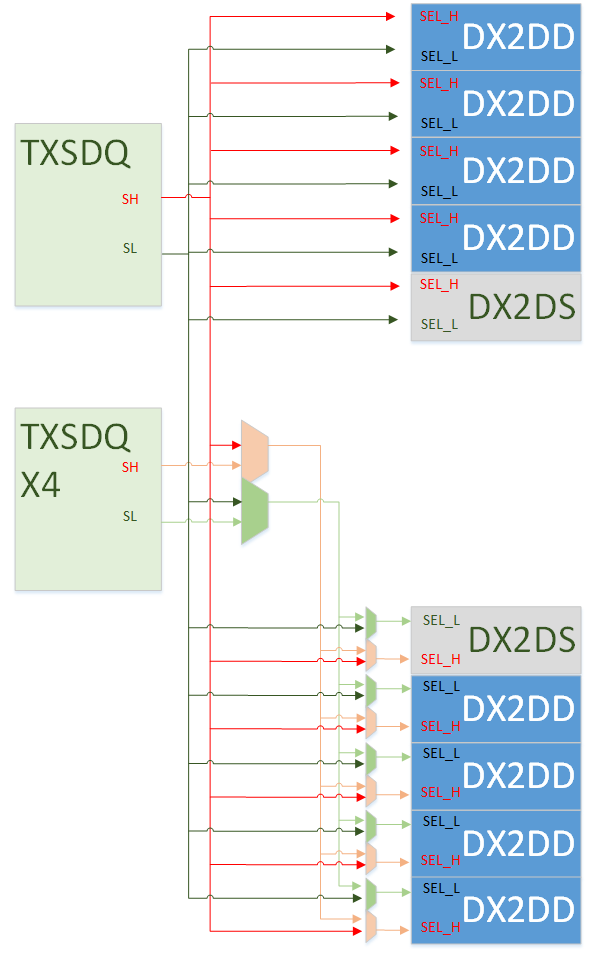
#### TXSDQ to DX2DD & DX2DS

SEL\_H/SEL\_L & SEL\_H\_X4/SEL\_L\_X4 from TXSDQ/TXSDQ\_X4 connect to DX2DD[7:0] and DX2DS & DX2DS\_X4 as below.

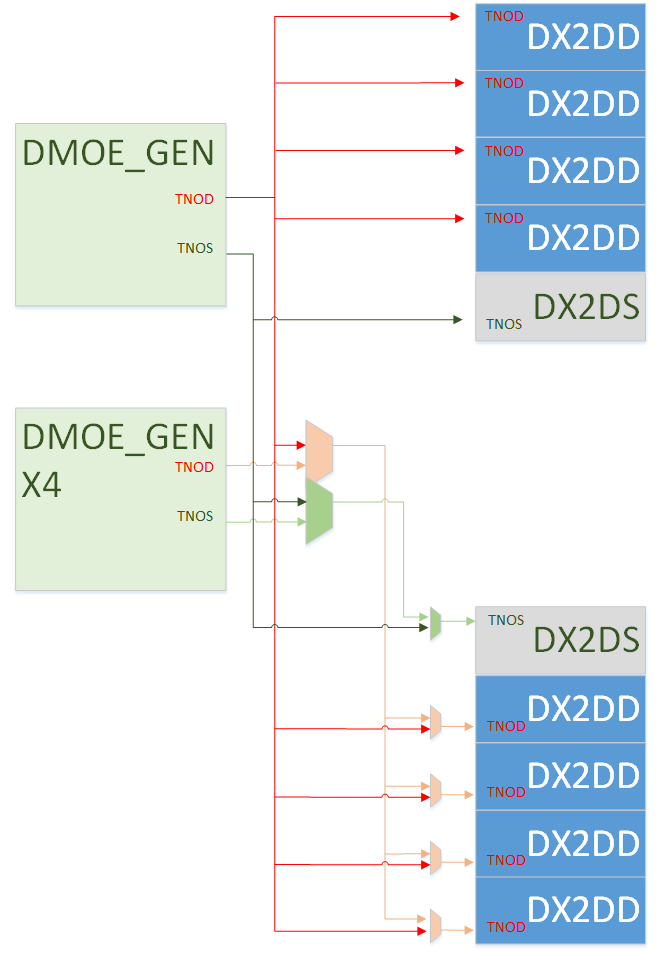
Timing requirement：

SEL\_H⬄SEL\_L⬄SEL\_H\_X4⬄SEL\_L\_X4 balance with each other

Each SEL should follow 5T/8 setup & -T/8 hold timing



#### DMOE\_GEN to DX2DD & DX2DS



### DDRPHY RXDIO

Tree for DQSIEN\_HEAD0, DQSIEN\_HEAD2, DDWPG2

### DDRPHY DDRCKG

Follow DDRCKG\_DDRCLK\_S24

TNOD/TNOS/TNOD\_X4/TNOS\_X4

TNID/TNIS/TNID\_X4/TNIS\_X4

DCLKO/DCLKOP

DCLKD/DCLKS/DCLKD\_X4/DCLKS\_X4

### DDRPHY DDRIO

COMPPD/ODT/NDTREE and others

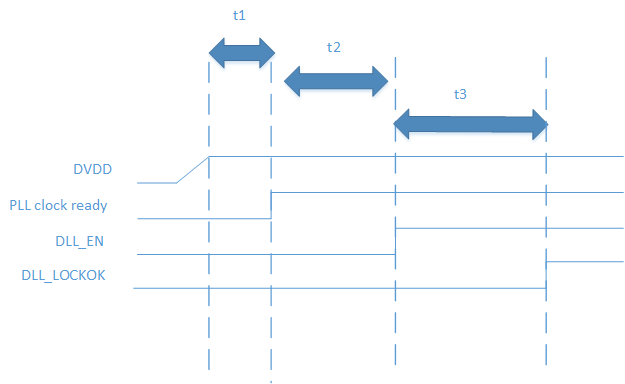
# Implement Note

## Power states

### Normal work state

After DLL\_EN asserts, ADLL need more than 8000 cycle to settle stable delay (total 1T in loop) with core power and PLL clock ready. If DLL\_LOCKOK doesn’t turns to logic High, it means different clock phase generated by ADLL and RX delay line is not accurate, and all logic IP can’t work normally.

In below picture, t1>0, t2>0 and t3>8000T



### DLL WeakLock Mode

Assert DLL\_WEAKLOCK will enable power saving mode, and DDRPHY could resume immediately when de-assert DLL\_WEAKLOCK. In this mode, DCLK will be gated by DLL\_WEAKLOCK, and delay of analog delay line will hold in certain time. Then DLL\_WEAKLOCK should be de-asserted and ADLL loop re-work to correct the delay of delay line. In Weaklock mode, DLL\_LOCKOK is always on.

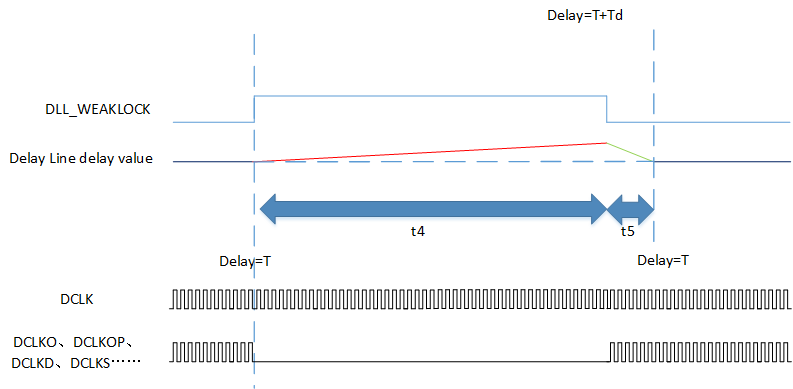
As below diagram, when DLL\_WEAKLOCK turns to 1, delay of delay line will change slowly. Delay will change to T+td in t4 time. Then controller turn off DLL\_WEAKLOCK mode, and delay will change back to T in t5 time.

In CMT003 DDRPHY, td is limited to 5% of T, such as for 1600MHz clock, td=31.25ps. In t5 time or later, DDRPHY can work fine.

td<5%T

t4<1us

t5>100ps



### DCLK turn off

WEAKLOCK mode could not be applied to case as below:

1. DVDD power down, suspend mode as example
2. DCLK is turn off for longer time than t4.

Once they happen, DLL\_EN should be de-asserted and it takes t3 time to resume DDRPHY after DLL\_EN assert again.

## Timing

### Balance Requirement

#### Path 1 SEL\_H/L & SEL\_H/L\_X4 from TXSDQ to DX2DD & DX2DS

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| TXSDQ | SH | DX2DD0  DX2DD1  DX2DD2  DX2DD3  DX2DD4  DX2DD5  DX2DD6  DX2DD7 | SEL\_H | T1 | T/2 setup & –T/4 hold time requirement |
| SL | DX2DD0  DX2DD1  DX2DD2  DX2DD3  DX2DD4  DX2DD5  DX2DD6  DX2DD7 | SEL\_L |
| TXSDQ\_X4 | SH | DX2DD4  DX2DD5  DX2DD6  DX2DD7 | SEL\_H |
|  | SL | DX2DD4  DX2DD5  DX2DD6  DX2DD7 | SEL\_L |

#### Path 2 TNOD/S & TNOD/S\_X4 from DMOE\_GEN to DX2DD/S & pads

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| DMOE\_GEN | TNOD | bdddrdq0  bdddrdq 1  bdddrdq 2  bdddrdq 3  bdddrdq 4  bdddrdq 5  bdddrdq 6  bdddrdq 7 | TNO | T2 |  |
| TNOS | bdddrdqs 0 | TNO |  |
| DMOE\_GEN\_X4 | TNOD | bdddrdq 4  bdddrdq 5  bdddrdq 6  bdddrdq 7 | TNO |  |
| TNOS | bdddrdqs 1 | TNO |  |
| DMOE\_GEN | TNOD | DX2DD0  DX2DD1  DX2DD2  DX2DD3  DX2DD4  DX2DD5  DX2DD6  DX2DD7 | TNOD | T3 |  |
| TNOS | DX2DS  DX2DS\_X4 | TNOS |  |
| DMOE\_GEN\_X4 | TNOD | DX2DD4  DX2DD5  DX2DD6  DX2DD7 | TNOD |  |
| TNOS | DX2DS\_X4 | TNOS |  |

#### Path 3 TNI & TNI\_X4 from DQSIEN\_GEN to bdddrdq[s]

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| DQSIEN\_GEN | TNID | bdddrdq0  bdddrdq 1  bdddrdq 2  bdddrdq 3  bdddrdq 4  bdddrdq 5  bdddrdq 6  bdddrdq 7 | TNI | T4 |  |
| TNIS | bdddrdqs 0 | TNI |  |
| DMOE\_GEN\_X4 | TNID | bdddrdq 4  bdddrdq 5  bdddrdq 6  bdddrdq 7 | TNO |  |
| TNIS | bdddrdqs 1 | TNO |  |

#### Path 4 DQSIEN\_GEN header signal to RXDIO

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| DQSIEN\_GEN | DQSIEN\_HEAD0 | RXDIO0  RXDIO1  RXDIO2  RXDIO3  RXDIO4  RXDIO5  RXDIO6  RXDIO7 | DQSIEN\_HEAD0 | T5 |  |
| DQSIEN\_HEAD2 | RXDIO0  RXDIO1  RXDIO2  RXDIO3  RXDIO4  RXDIO5  RXDIO6  RXDIO7 | DQSIEN\_HEAD2 |  |
|  | DDWPG2 | RXDIO0  RXDIO1  RXDIO2  RXDIO3  RXDIO4  RXDIO5  RXDIO6  RXDIO7 | DDWPG2 |  |
| DQSIEN\_GEN\_X4 | DQSIEN\_HEAD0 | RXDIO4  RXDIO5  RXDIO6  RXDIO7 | DQSIEN\_HEAD0 |  |
| DQSIEN\_HEAD2 | RXDIO4  RXDIO5  RXDIO6  RXDIO7 | DQSIEN\_HEAD2 |  |
| DDWPG2 | RXDIO4  RXDIO5  RXDIO6  RXDIO7 | DDWPG2 |  |

#### Path 4 DCLKO/DCLKOP/DCLKD/DCLKS/DCLKDSI & DCLKD\_X4 /DCLKS\_X4/DCLKDSI\_X4 from VCDL\_BYTE\_S24 to DIO & pads

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| VCDL\_BYTE\_S24 | DCLKO | DX2DD0  DX2DD1  DX2DD2  DX2DD3  DX2DD4  DX2DD5  DX2DD6  DX2DD7  TXSDQ  TXSDQ\_X4  DX2DS  DX2DS\_X4  DMOE\_GEN  DMOE\_GEN\_X4  DQSIEN\_GEN  DQSIEN\_GEN\_X4 | CLKO | T6 |  |
| DCLKO | PHY TOP | DCLKO |  |
| DCLKOP | TXSDQ  TXSDQ\_X4  DX2DS  DX2DS\_X4  DMOE\_GEN  DMOE\_GEN\_X4 | CLKOP |  |
| DCLKD | ~~DX2DD0~~  ~~DX2DD1~~  ~~DX2DD2~~  ~~DX2DD3~~  ~~DX2DD4~~  ~~DX2DD5~~  ~~DX2DD6~~  ~~DX2DD7~~  DMOE\_GEN  DQSIEN\_GEN | ~~TXCLK~~  TXCLKD |  |
| DCLKD\_X4 | ~~DX2DD4~~  ~~DX2DD5~~  ~~DX2DD6~~  ~~DX2DD7~~  DMOE\_GEN\_X4  DQSIEN\_GEN\_X4 | TXCLK  TXCLKD |  |
| DCLKS | DX2DS  DMOE\_GEN | TXCLK  TXCLKS |  |
| DCLKS\_X4 | DX2DS\_X4  DMOE\_GEN\_X4 | TXCLK  TXCLKS |  |
| DCLKDSI | DQSIEN\_GEN | CLKDSI |  |
| DCLKDSI\_X4 | DQSIEN\_GEN\_X4 | CLKDSI |  |

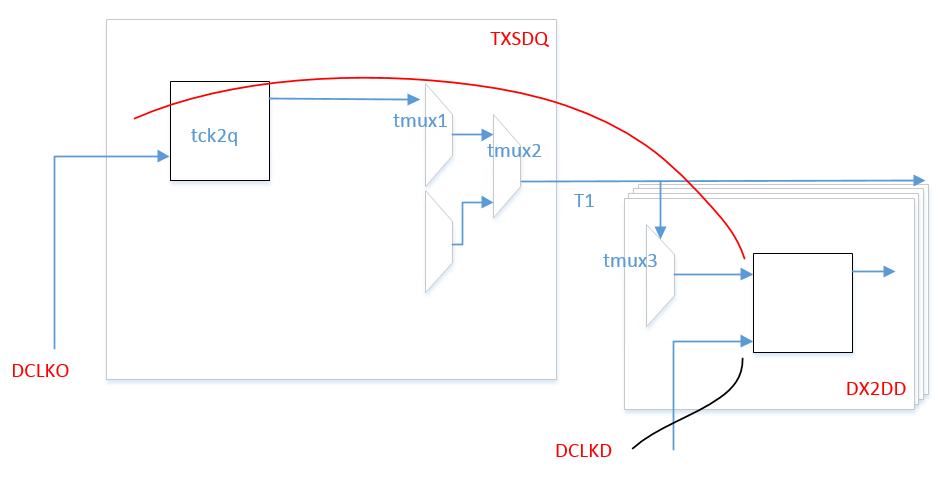
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| VCDL\_BYTE\_S24 | DCLKD | bdddrdq 0  bdddrdq 1  bdddrdq 2  bdddrdq 3  bdddrdq 4  bdddrdq 5  bdddrdq 6  bdddrdq 7 | SEL | T7 |  |
| DCLKD\_X4 | bdddrdq 4  bdddrdq 5  bdddrdq 6  bdddrdq 7 | SEL |  |
| DCLKS | bdddrdqs 0 | SEL |  |
| DCLKS\_X4 | bdddrdqs 1 | SEL |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Begin | | End | | Delay | Note |
| IP name | Port | IP name | Port |
| VCDL\_BYTE\_S24 | DCLKD | DX2DD0  DX2DD1  DX2DD2  DX2DD3  DX2DD4  DX2DD5  DX2DD6  DX2DD7 | TXCLK | T8 |  |
| DCLKD\_X4 | DX2DD4  DX2DD5  DX2DD6  DX2DD7 | TXCLK |  |

### External Constraint Requirement(less)

### Internal Constraint Requirement

#### SEL\_H/L setup/hold constraint

tck2q+tmux1+tmux2+T1+tmux3<5T/8-VCDL\_Jitter\_Skew-Tsetup  


#### TNOD/S & TNI header delay requirement

T3 delay as min as possible

T4<300ps

T5<300ps

#### DCLKD/S constraint

T6=T7

T7<T8

#### TXDIO internal

### Internal Constraint Conclusion Table

Internal timing requirement in Verilog module by FE as:



Actual timing calculation in schematic by CKT as:

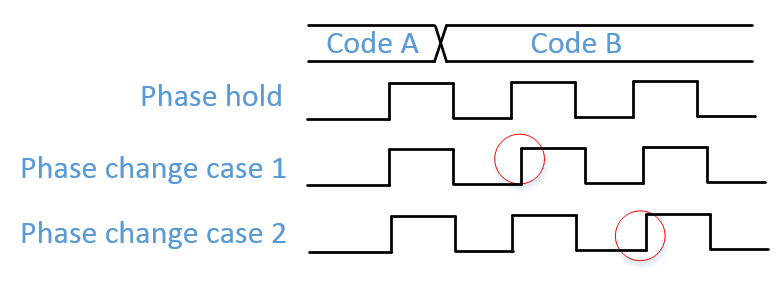


## VCDL\_BYPASS mode

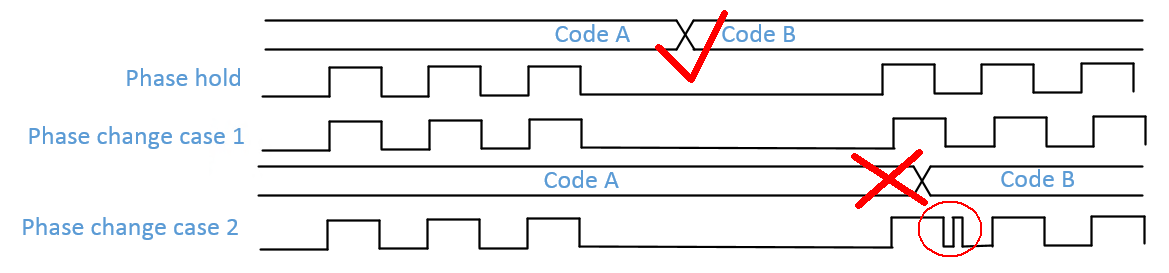
## Calibration(less)

## Glitch

For TX clock such as DCLKO/DCLKOP/DCLKD/…, when controller changes corresponding phase setting, there would be no glitch at each clock. It should be noted that, the output clock phase doesn’t follow the setting change immediately. It may take another 0.5~2T to change output clock phase to avoid glitch. Case 1 and case 2 are both possible in below picture.



There is no glitch-avoid function for VCDL\_PI\_DQS, so controller can change VCDL\_PI\_DQS phase setting when there is no DQS input. If VCDL\_PI\_DQS phase setting change in Reading Mode, DQS glitch would appear and DDR couldn’t work.



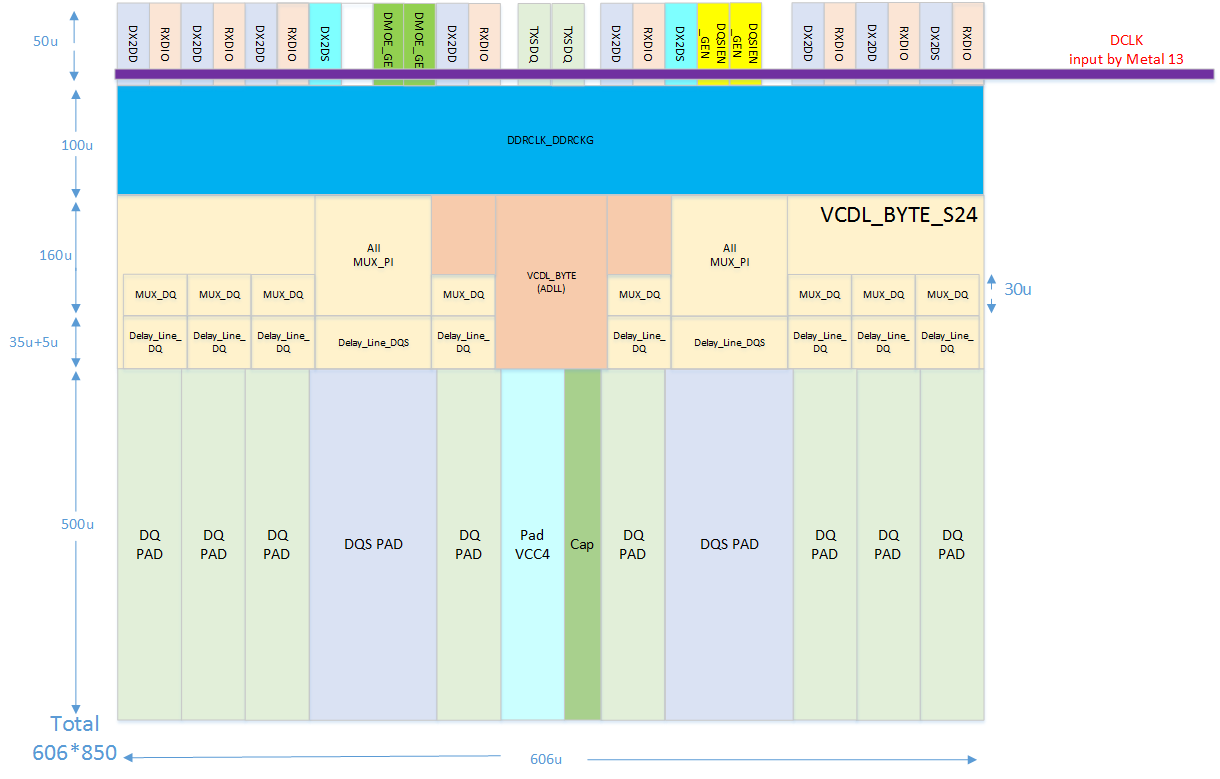
## Frequency change

**In normal operation, frequency can’t be changed.**

**When frequency change, DLL\_EN must be trigger from 0 to 1.**

# DDRPHY FloorPlan & BumpMap

## Floorplan

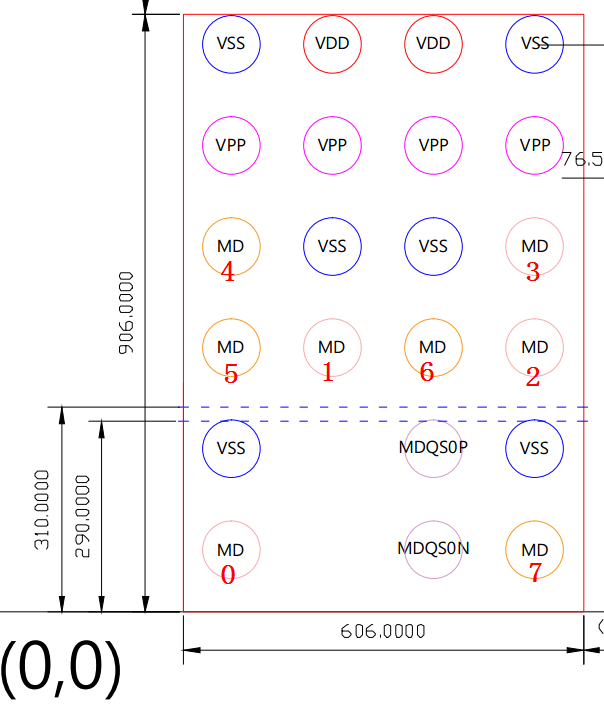


## Pad assignment

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| DQ4 | DQ5 | DQ0 | DQS9N  -DQS9P | DQ1 | VCC4  +CAP | DQ6 | DQS0P  -DQS0N | DQ7 | DQ2 | DQ3 |

## BumpMap

Version:T16 DDR Bump Map Ver.0.5 for CMT003



# Test(less)