# 1 DMDIOTOP\_CHA

## 1.1 CACLK

### 1.1.1 DIO\_DDRCOMP\_OFS\_MA

input signal from D0F3, output to ddr pad

### 1.1.2 DIO\_DDRMA\_1X

10 instances---DIO\_MA[0:9]\_0, connect to ddr pad (TNI/TNO), DL output to ddr pad go through DDRCKG\_CACLLK\_S24

### 1.1.3 DIO\_CKE

4 instances---DIO\_MCKE[0:3]\_0, connect to ddr pad(TNI/TNO), RASAO0 output to ddr pad go through DDRCKG\_CACLLK\_S24

### 1.1.4 DIO\_MCLKO

4 instances---DIO\_MCLKO[0:3]p\_0, connect to ddr pad(TNI/TNO), the DCLKO refer to

[chapter 1.14 GFX\_DLYCOMP\_S\_S24]

the input signal from d0f3 (**POWELL\_PE/D0F3\_0\_vsus/**)

### 1.1.5 DIO\_CS

4 instances---DIO\_MCS[0:3]\_0, connect to ddr pad(TNI/TNO), RASAO0 output to ddr pad go through DDRCKG\_CACLLK\_S24

## 1.2 CACLK\_1X

### 1.2.1 DIO\_DDRMA\_1X

13 instances --- 6 DIO\_MA[10:15]\_0 + 3 DIO\_MBA[2:0]\_0 + 1 DIO\_MSCAS\_0 + 1 DIO\_MSRAS\_0 + 1 DIO\_MSWE\_0 + 1 DIO\_PAR\_0

## 1.3 DDRIO\_INV\_SEL

the output clock CLKOUT connect to GFX\_DLYCOMP\_S\_S24,

该module的作用是反转clock signal, input from dramc\_clk\_ctrl

## 1.4 DDRCKG\_CACLK\_S24

对相应的pad 提供ODT, BA, CA, CKE, CS, DCLKO, RAS, CAS, WE, PAR.

同时，output ALERT signal给DRAMC from DDR pad.

也对CACLK/DIO\_MA module提供CMDCLK clock, DIO\_ODT提供DMDCLKCS clock

## 1.5 DDRCKG\_DDRCLK\_S24

## 1.6 DDRIO\_PERRANK\_MUX\_PHY

## 1.7 DDRPHY\_IP

### 1.7.1 DDRPHYA

#### 1.7.1.1 DQSIEN\_GEN

##### 1.7.1.1.1 ZIV11D\_DQSIEN

##### 1.7.1.1.2 DGP\_DFFLDP

#### 1.7.1.2 RXDIO\_S24

##### 1.7.1.2.1 RXDIO\_sdff1b\_rst

#### 1.7.1.3 TNOCTL

### 1.7.2 DIO\_DDRCOMP\_OFS

#### 1.7.2.1 PMTFFD2BWP\_DIO

### 1.7.3 DIO\_DDRPHY\_IP\_evinj

#### 1.7.3.1 DIO\_DDRPHY\_ALL\_evinj

##### 1.7.3.1.1 DIO\_DDRPHY\_DATA\_jessica

##### 1.7.3.1.2 DIO\_DMOE

TX data 的开关

##### 1.7.3.1.3 DMOE\_GEN\_evinj

##### 1.7.3.1.4 DQSIEN\_HEAD\_GEN\_evinj

##### 1.7.3.1.5 DRSEL\_GEN

#### 1.7.3.2 DX2DD

TX data

##### 1.7.3.2.1 DCONV\_WADV\_NEW

#### 1.7.3.3 DX2DS

TX DQS

##### 1.7.3.3.1 DCONV\_WADV\_NEW

#### 1.7.3.4 TXSDQ

TX data select

##### 1.7.3.4.1 DCONV\_WADV\_NEW

### 1.7.4 GFX\_DLYCOMP\_S\_S24

### 1.7.5 DLL\_DLYCOMPS\_S24

#### 1.7.5.1 DLL\_DLYCOMPS\_S24\_DLL\_PD\_DDR\_S24

#### 1.7.5.2 DLL\_DLYCOMPS\_S24\_GFX\_DLYCOMP\_S\_S24

#### 1.7.5.3 INIT\_BUF

#### 1.7.5.4 DLL\_DLYCOMPS\_S24\_TDI\_S24

### 1.7.6 DutyCOMP\_S24

### 1.7.7 REDUN\_DDRPHY\_IP

多余的RLT design，redundancy

## 1.8 DIO\_BUS\_DECODE

## 1.9 DIO\_BUS\_DECODE\_RANK

## 1.10 DIO\_BUS\_DESKEW\_DECODE

## 1.11 DIO\_DDRCOMP

### 1.11.1 CNTFRZ

## 1.12 DIO\_ODT

## 1.13 DutyCOMP\_S24

## 1.14 GFX\_DLYCOMP\_S\_S24

output CLKO clock signals to ddrpad go through DDRCKG\_CACLK\_S24

## 1.15 DLL\_DLY\_OFS

## 1.16 SEL\_REG\_PHY

## 1.17 dramc\_clk\_ctrl

### 1.17.1 DLL\_DLY\_OFS

### 1.17.2 CKLATCH\_DIO

### 1.17.3 CKLATCH2\_DIO

### 1.17.4 GFX\_DLYCOMP\_S\_S24

## 1.18 PMTFFD2BWP

meta stable cell, 用来处理亚稳态的问题