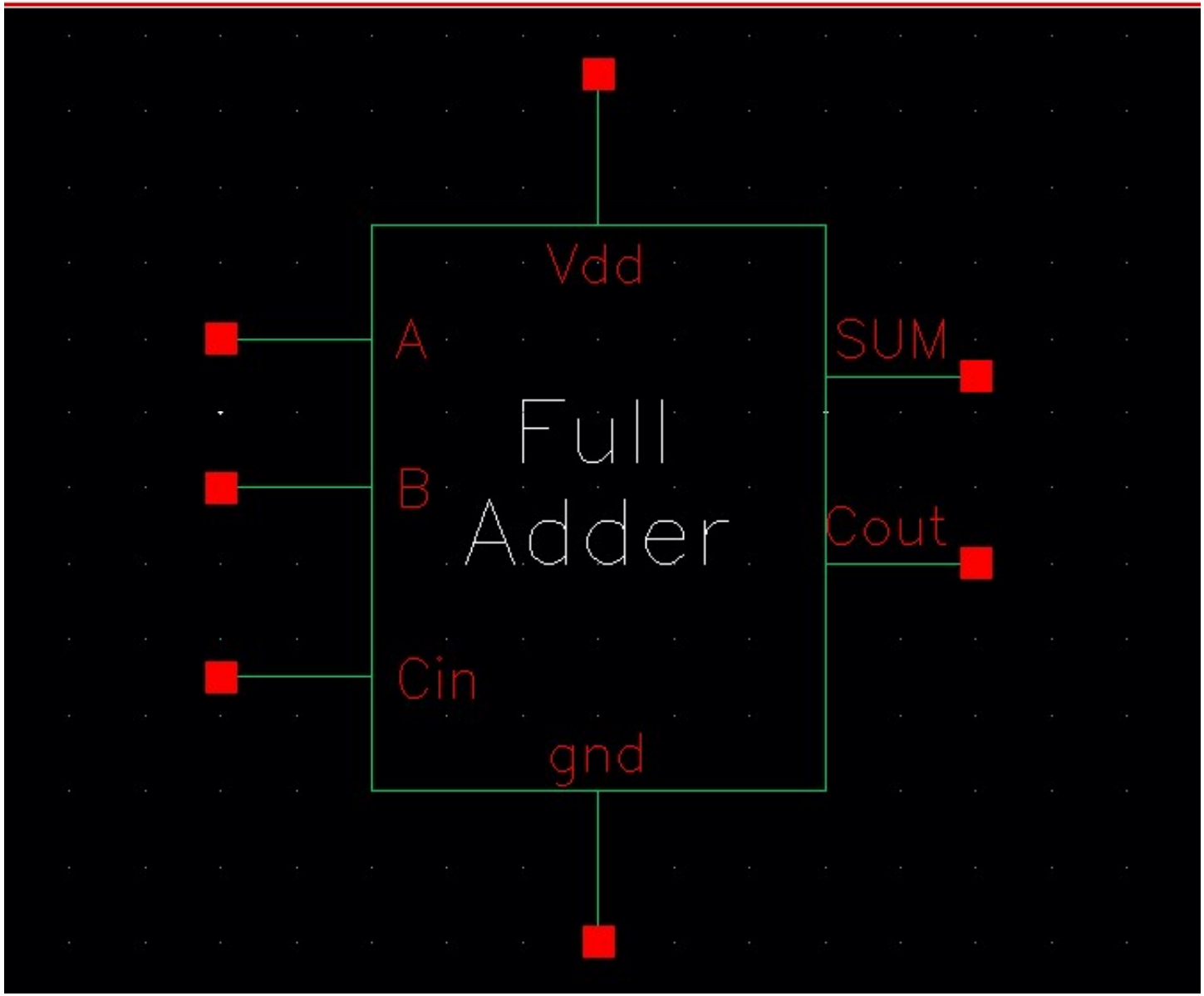
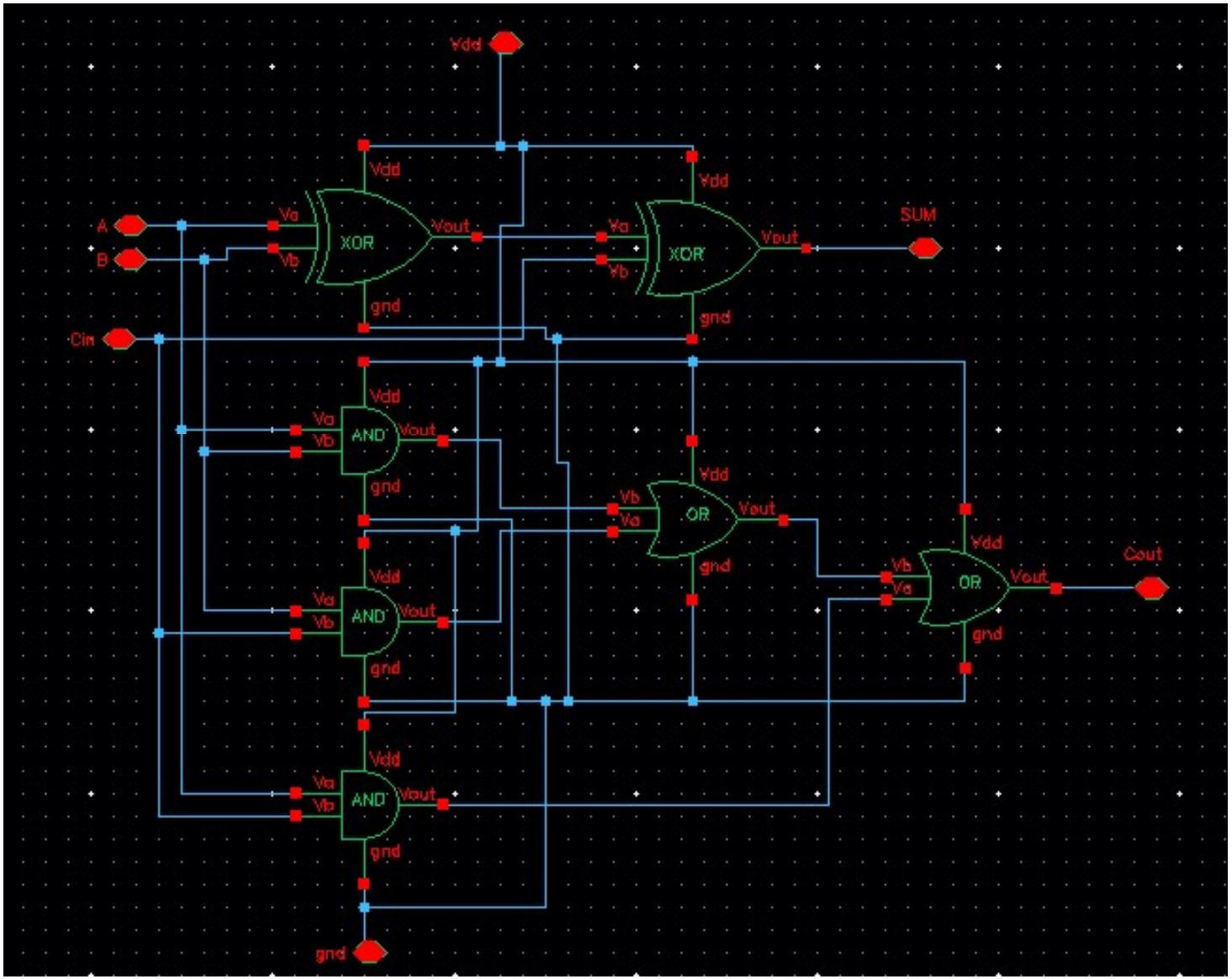
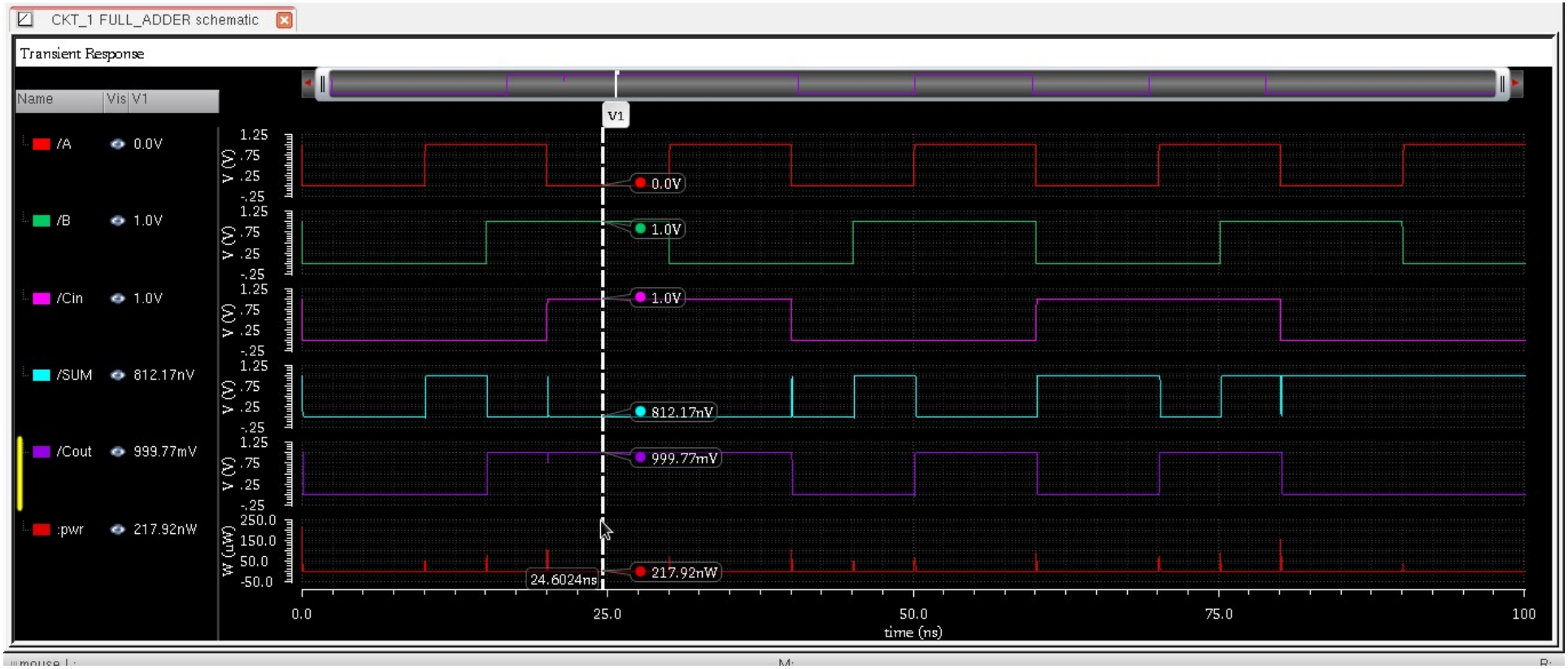
Symbolic Representation



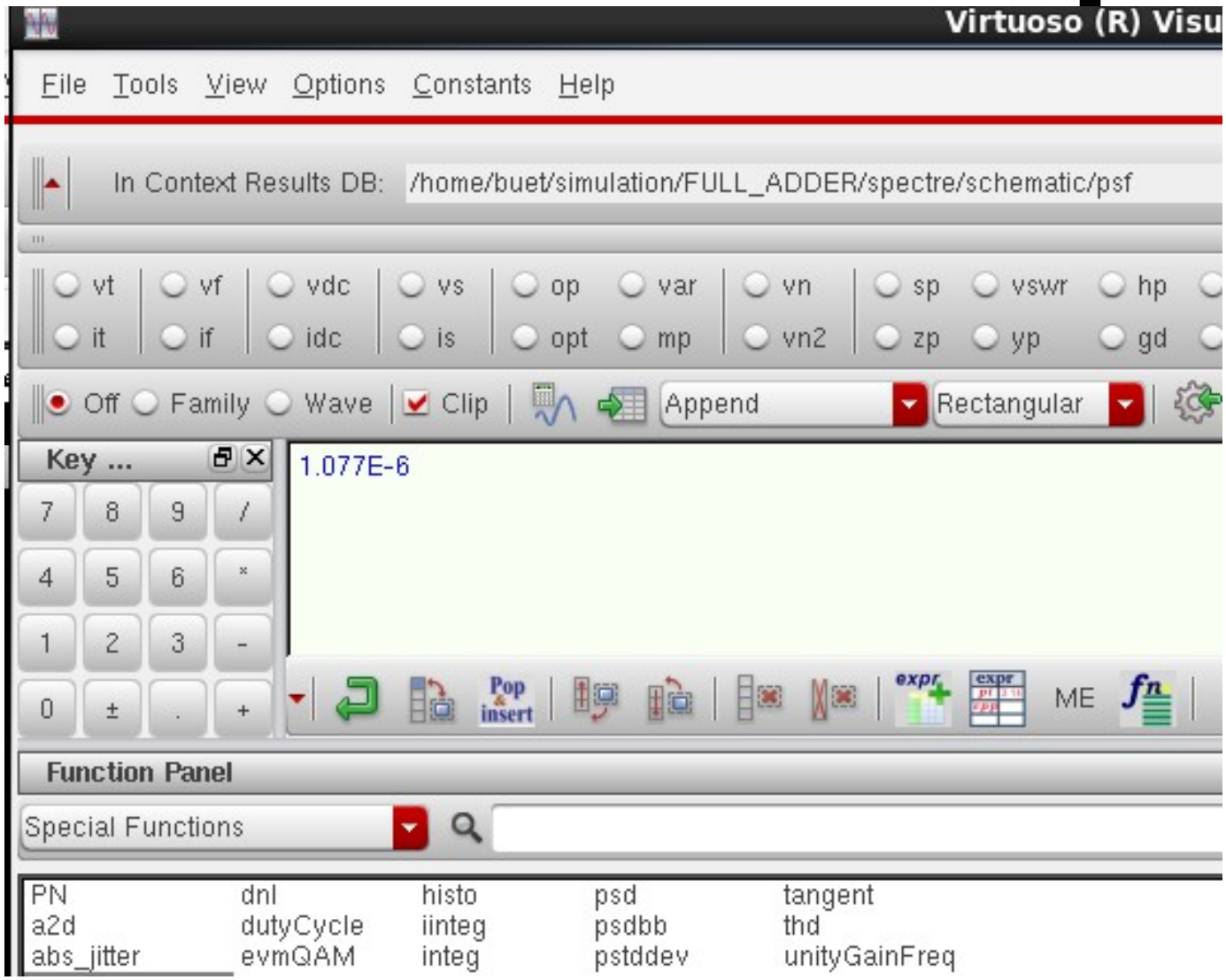
Schematic Representation



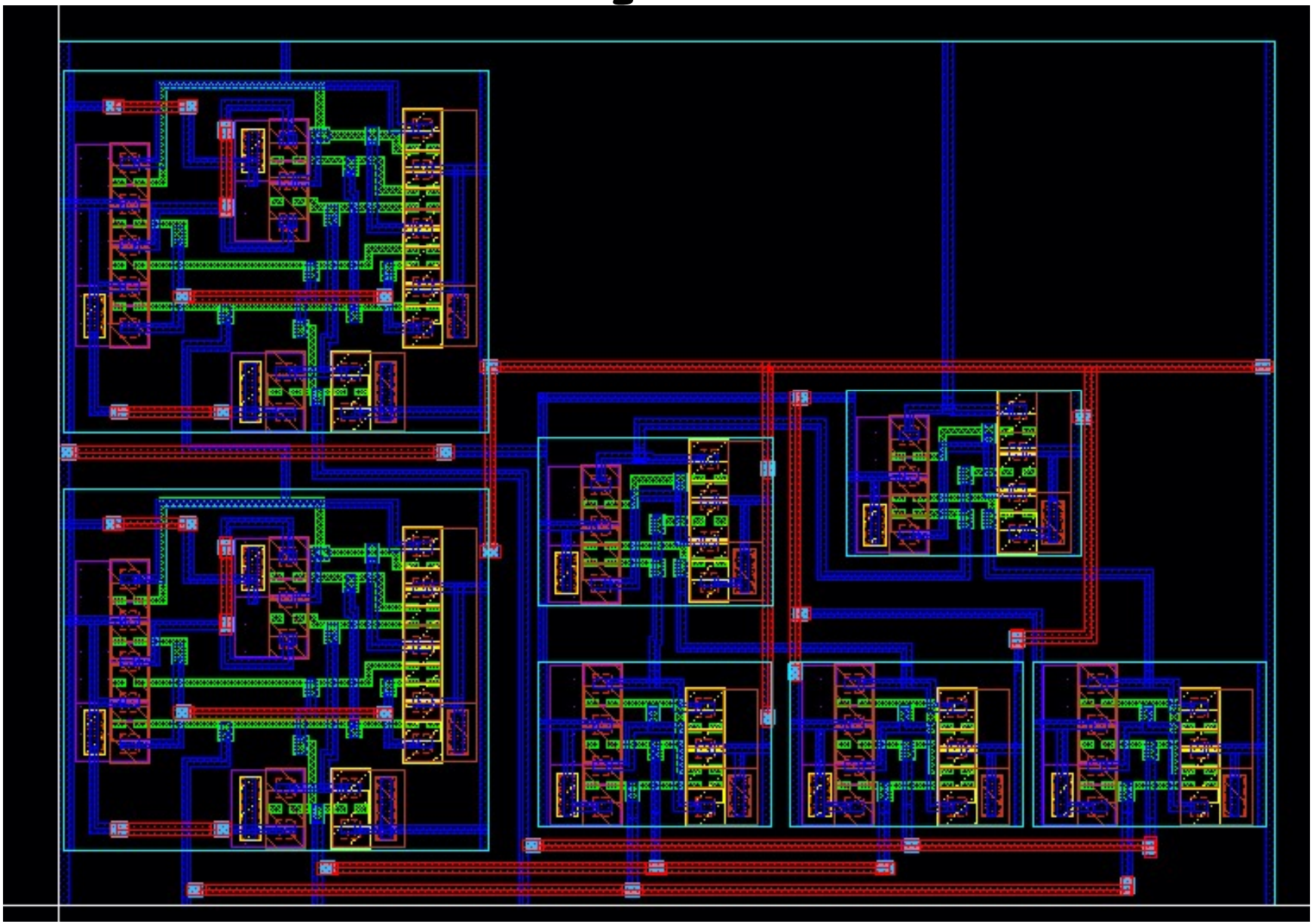
Transient Waveform



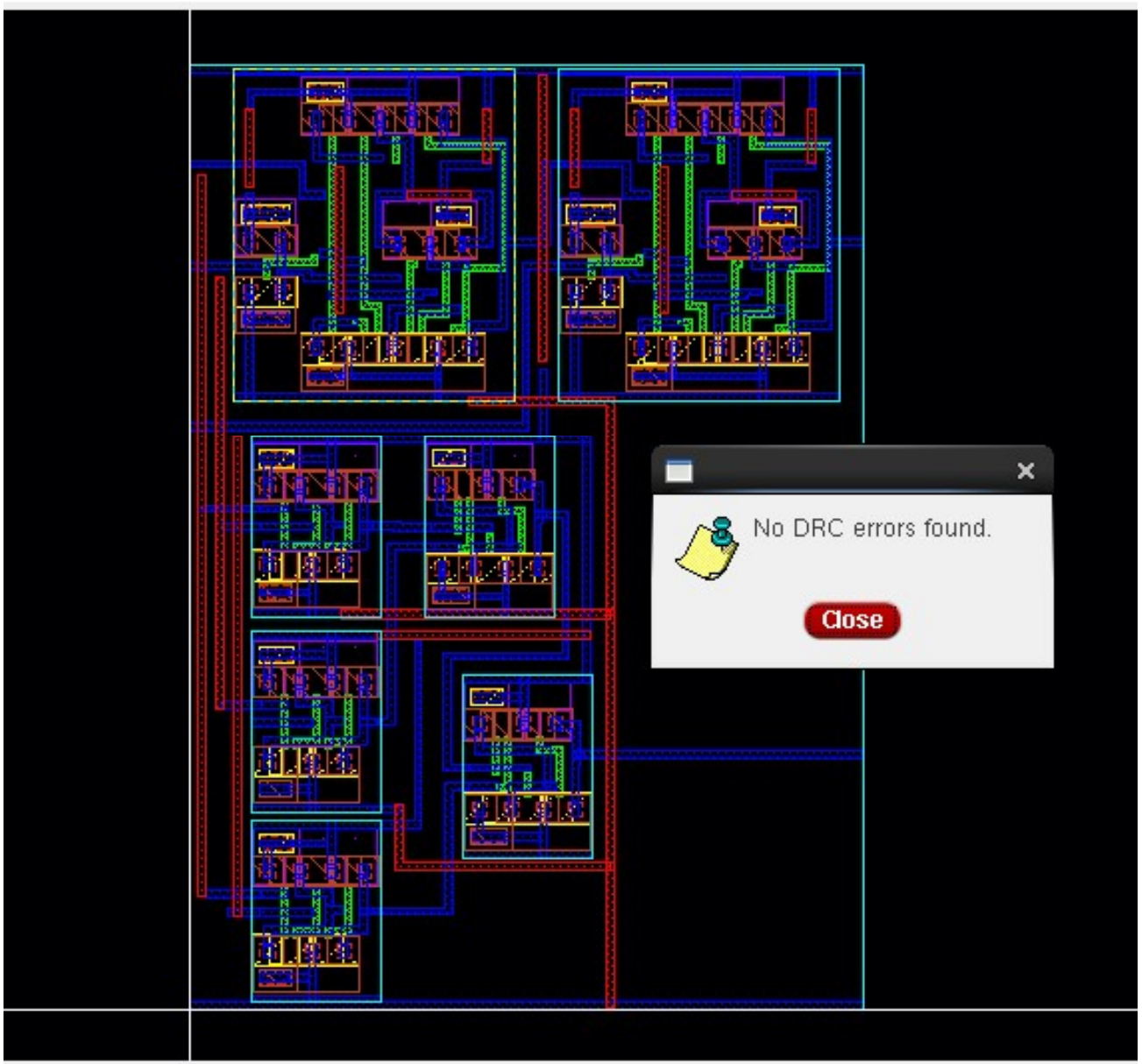
Power Consumption



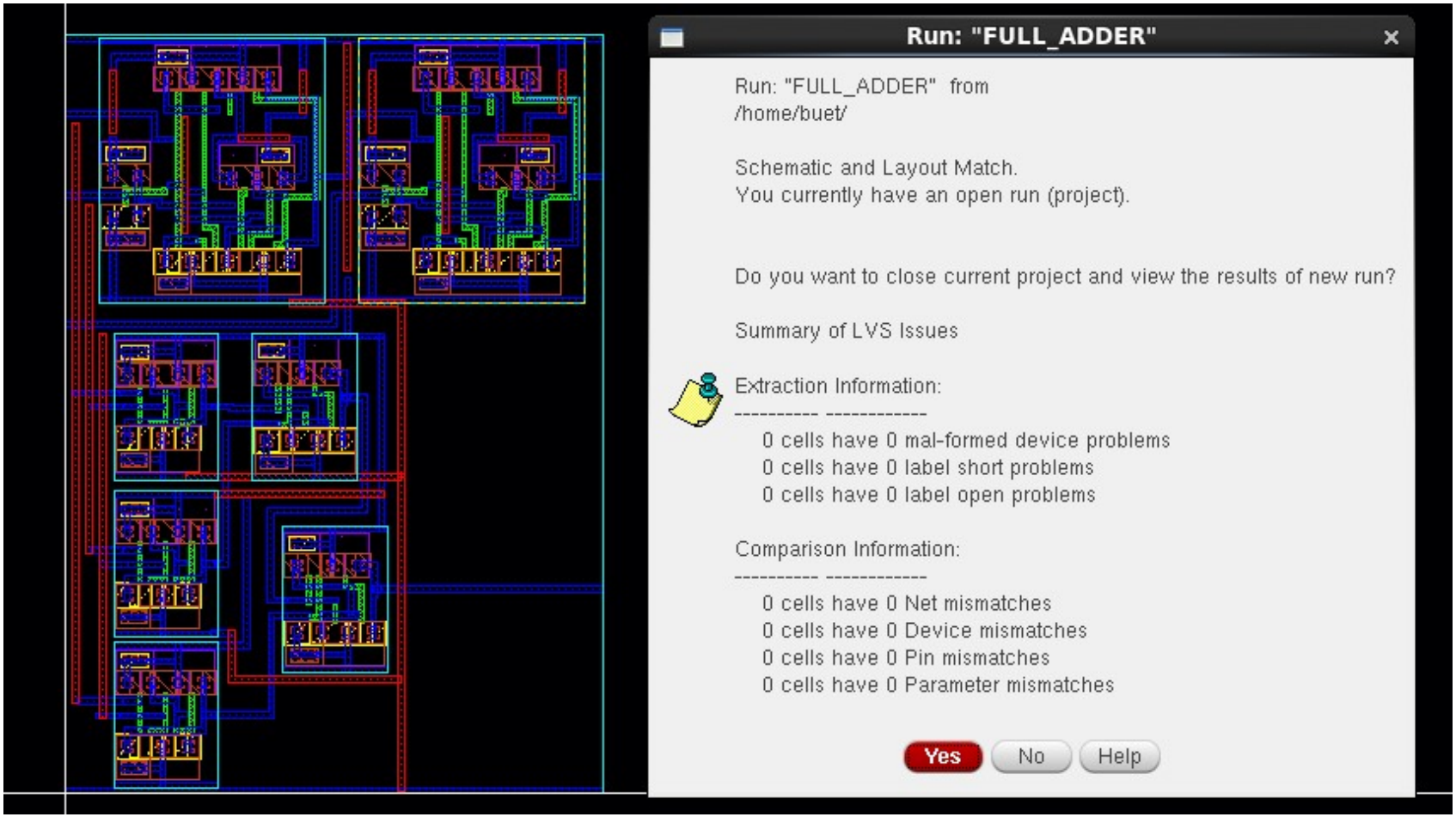
Layout



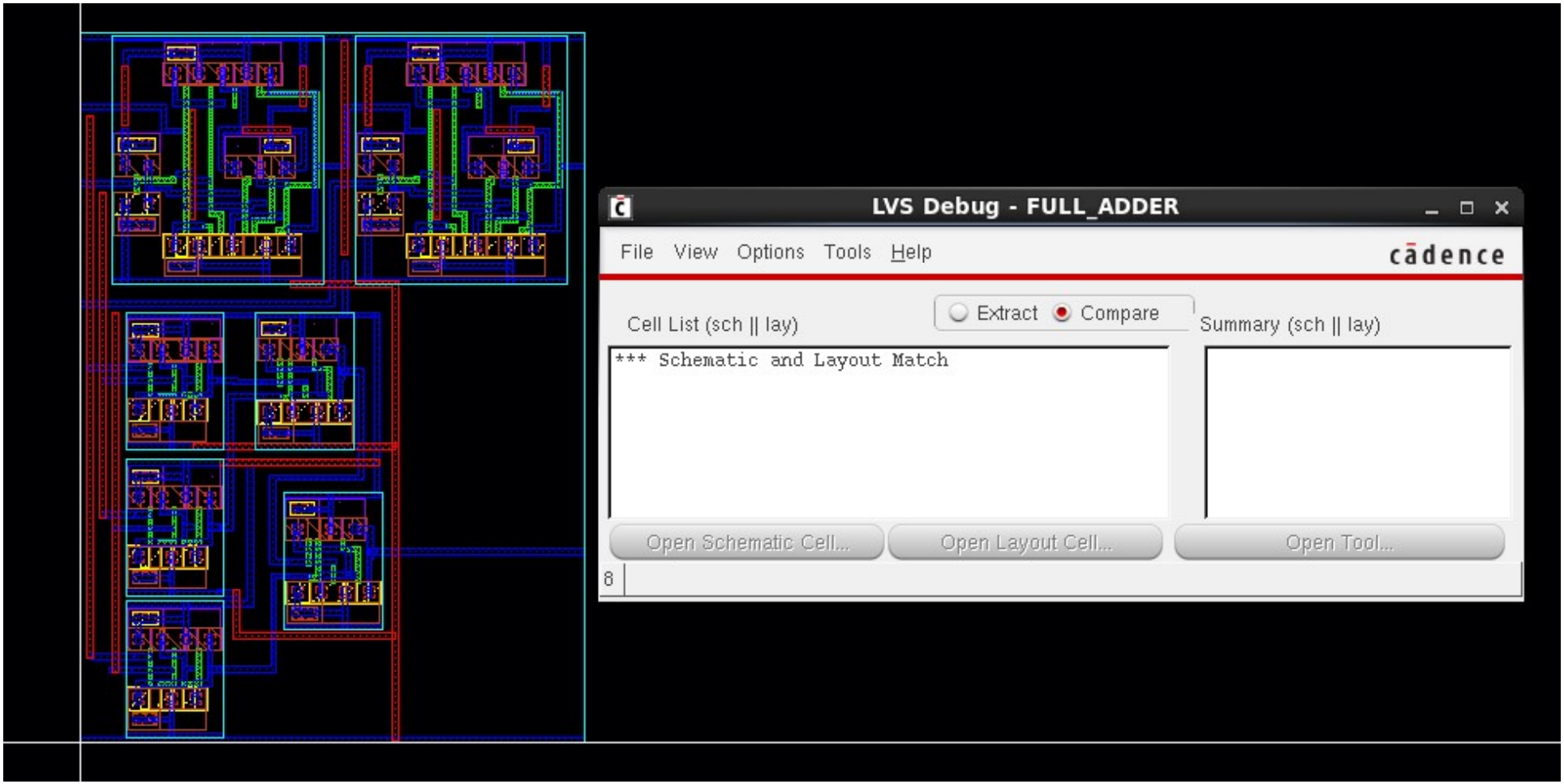
No DRC Error found



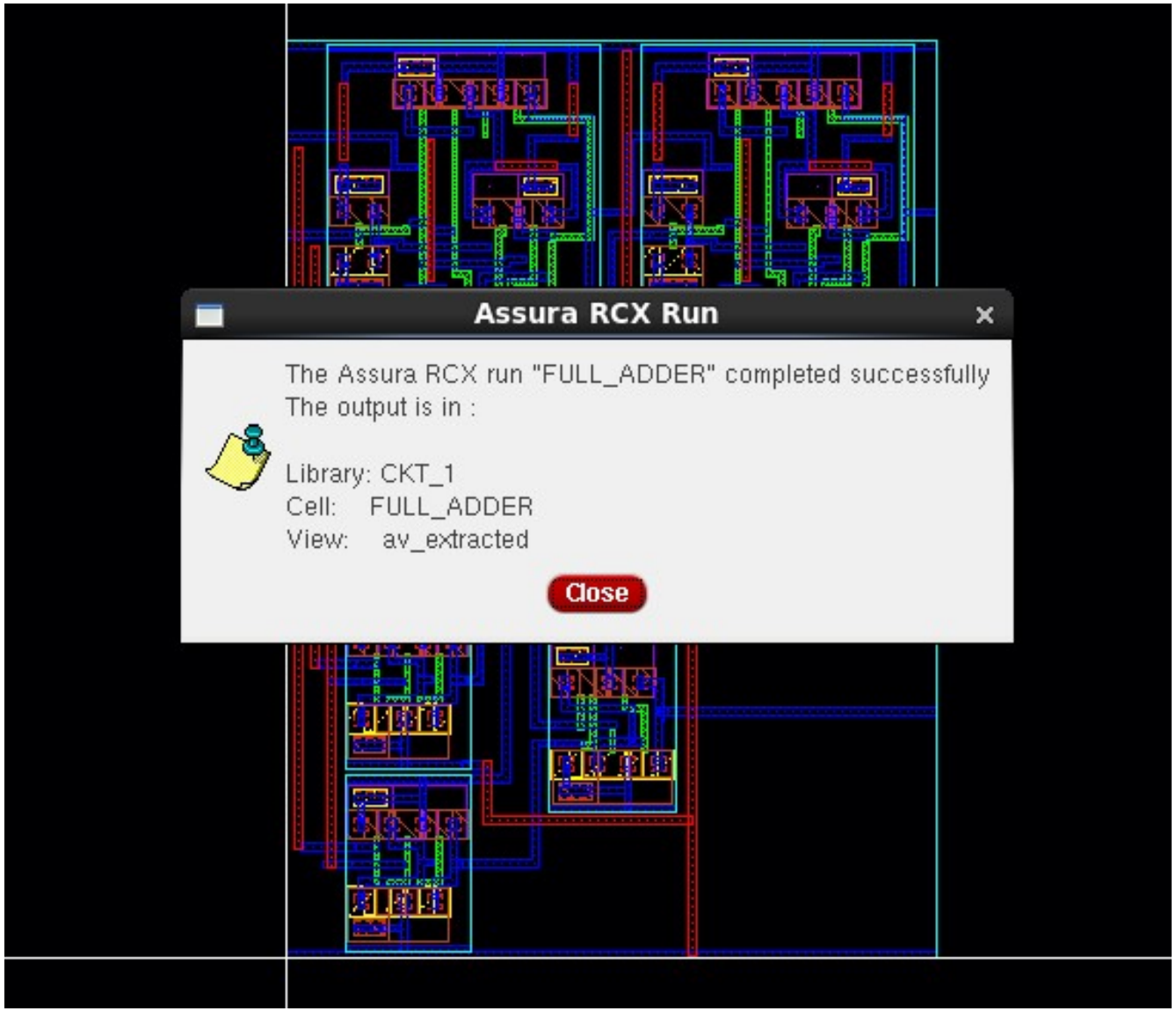
LVS with No mismatch



LVS Matched


LVS Debug - FULL_ADDER
File View Options Tools Help
cadence
Extract Compare
Cell List (sch || lay)
Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...
8

RCX Run


Assura RCX Run
The Assura RCX run "FULL_ADDER" completed successfully
The output is in :
Library: CKT_1
Cell: FULL_ADDER
View: av_extracted
Close

AV Extraction View