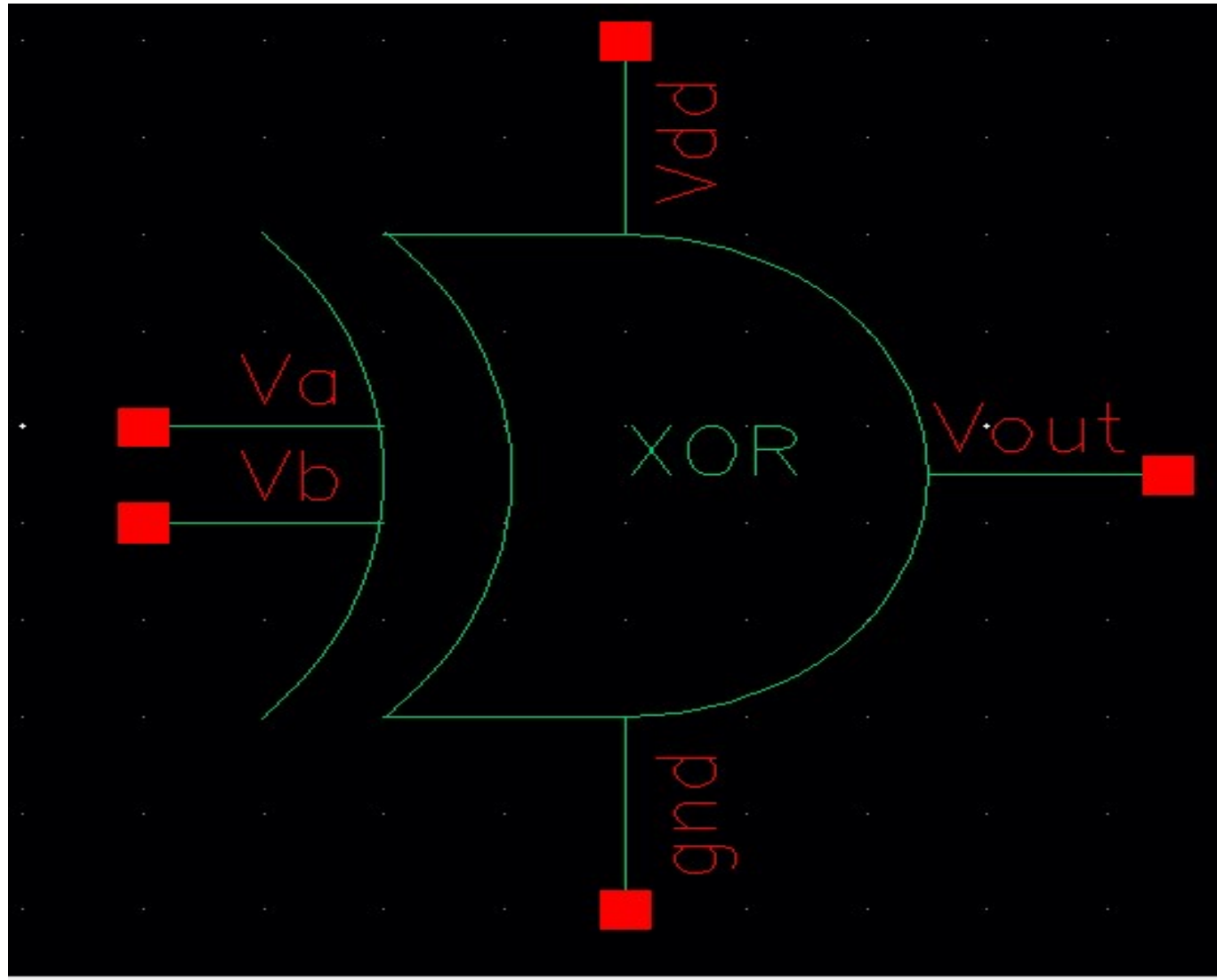
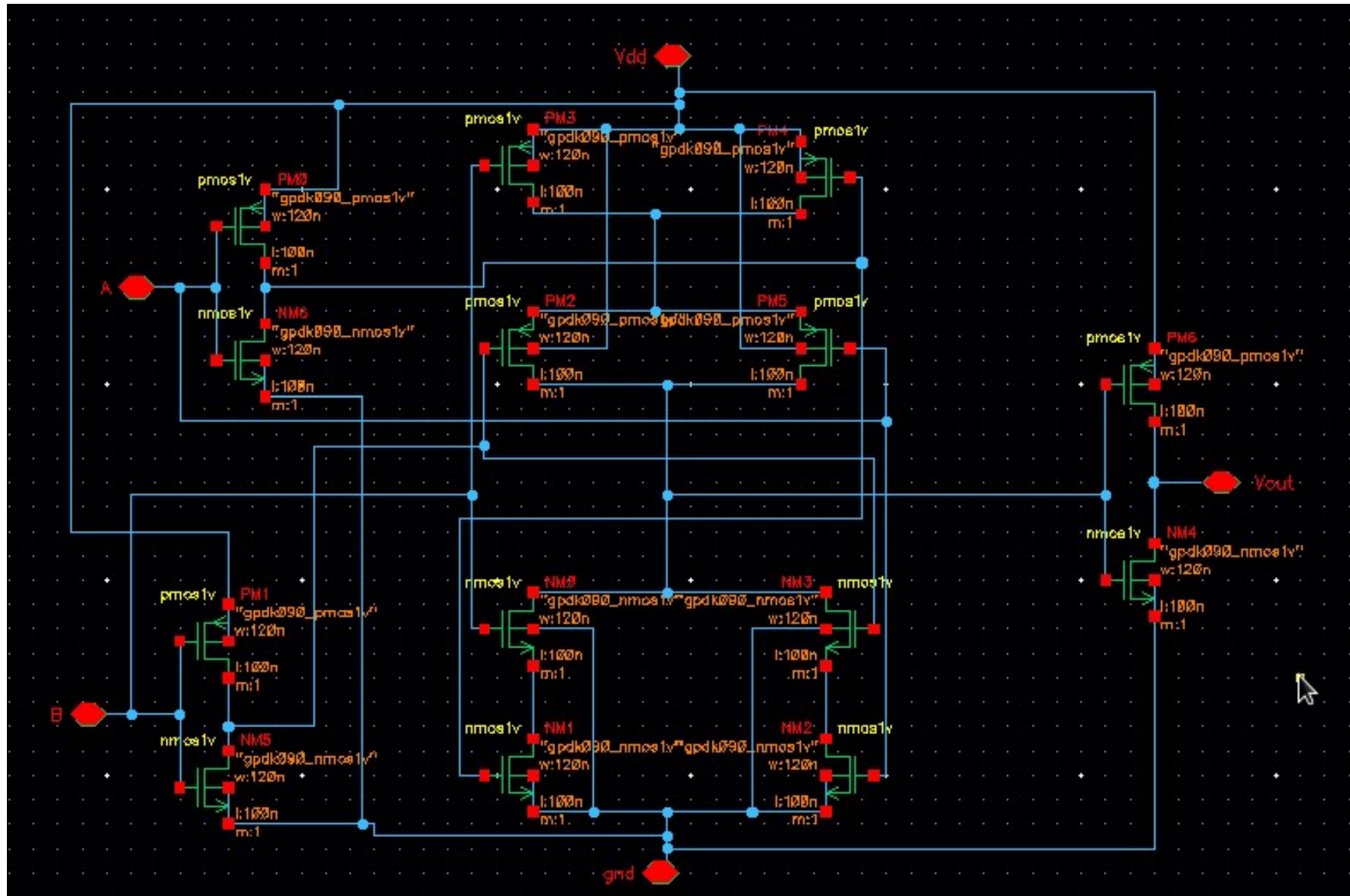


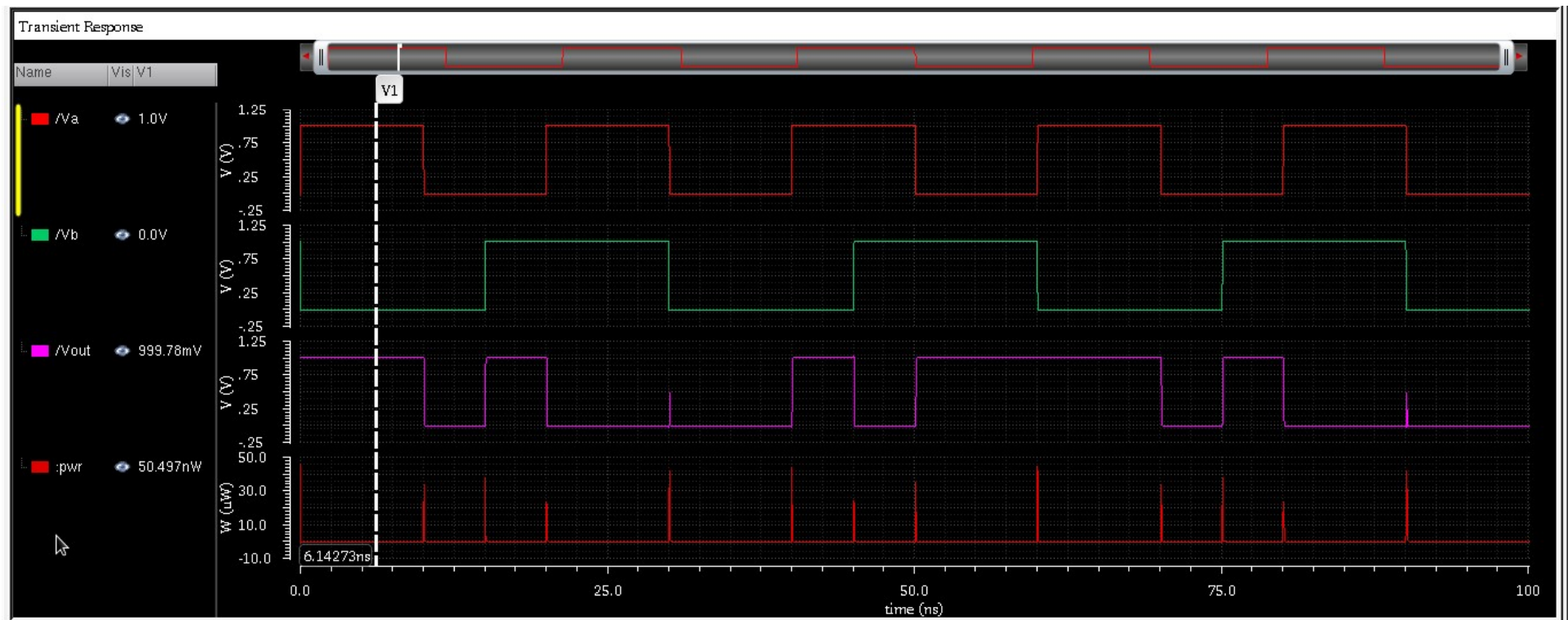
# Symbolic Representation



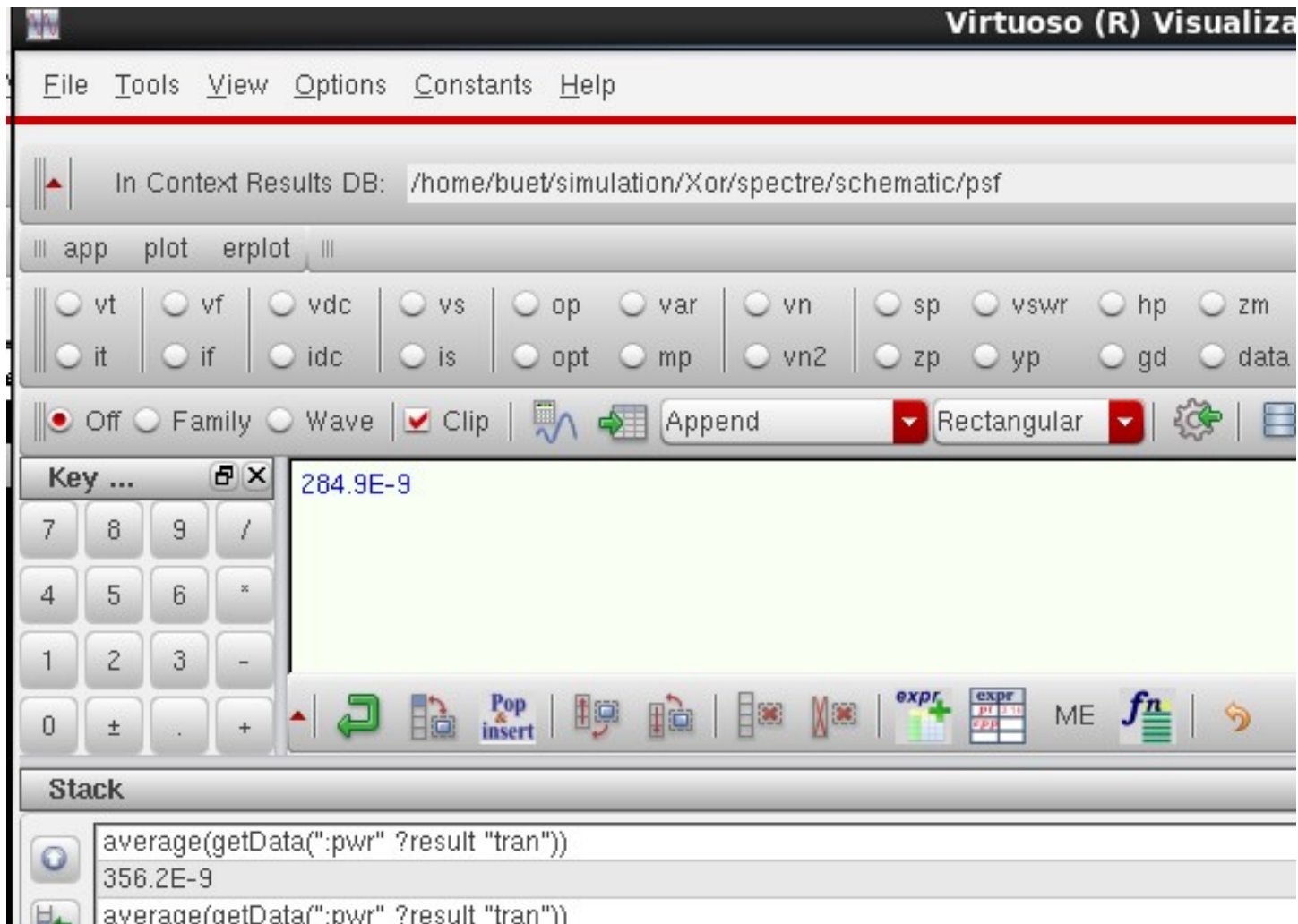
# Schematic Representation



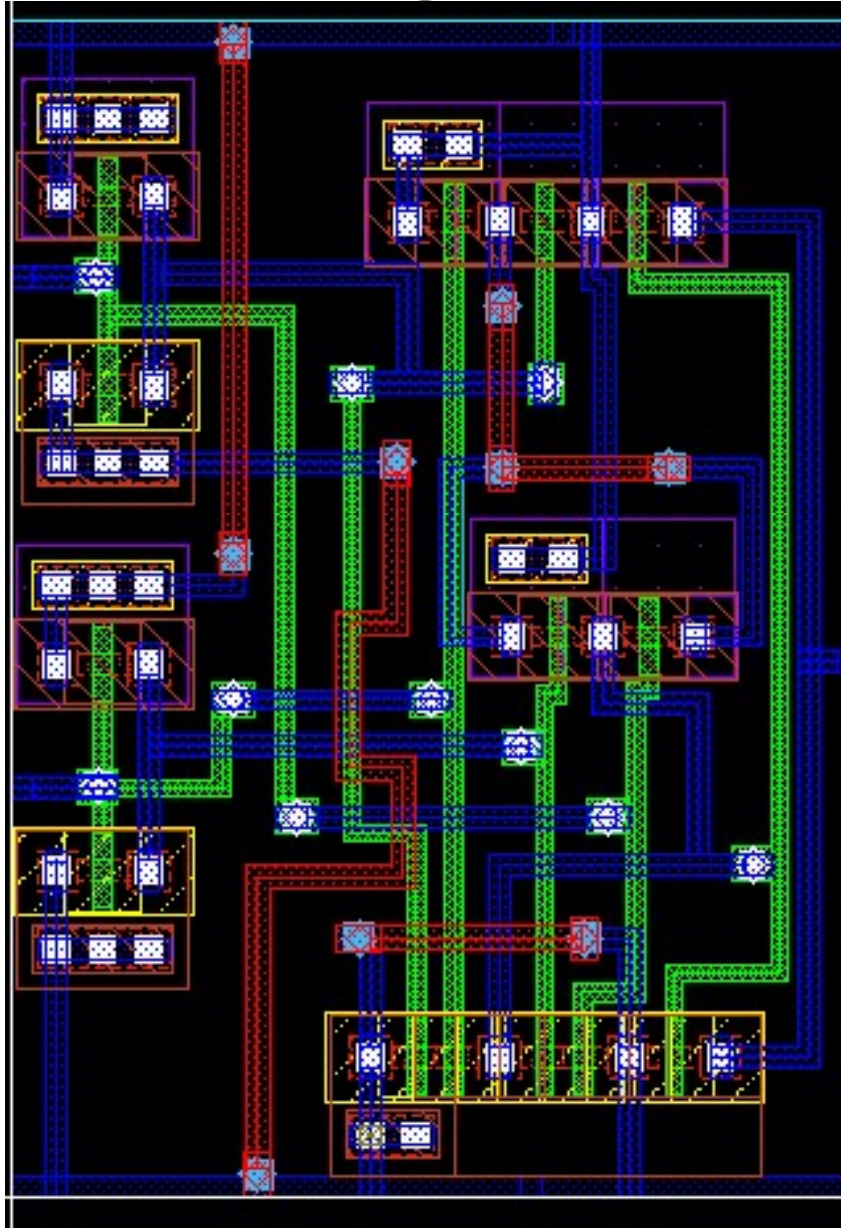
# Transient Waveform



# Power Consumption

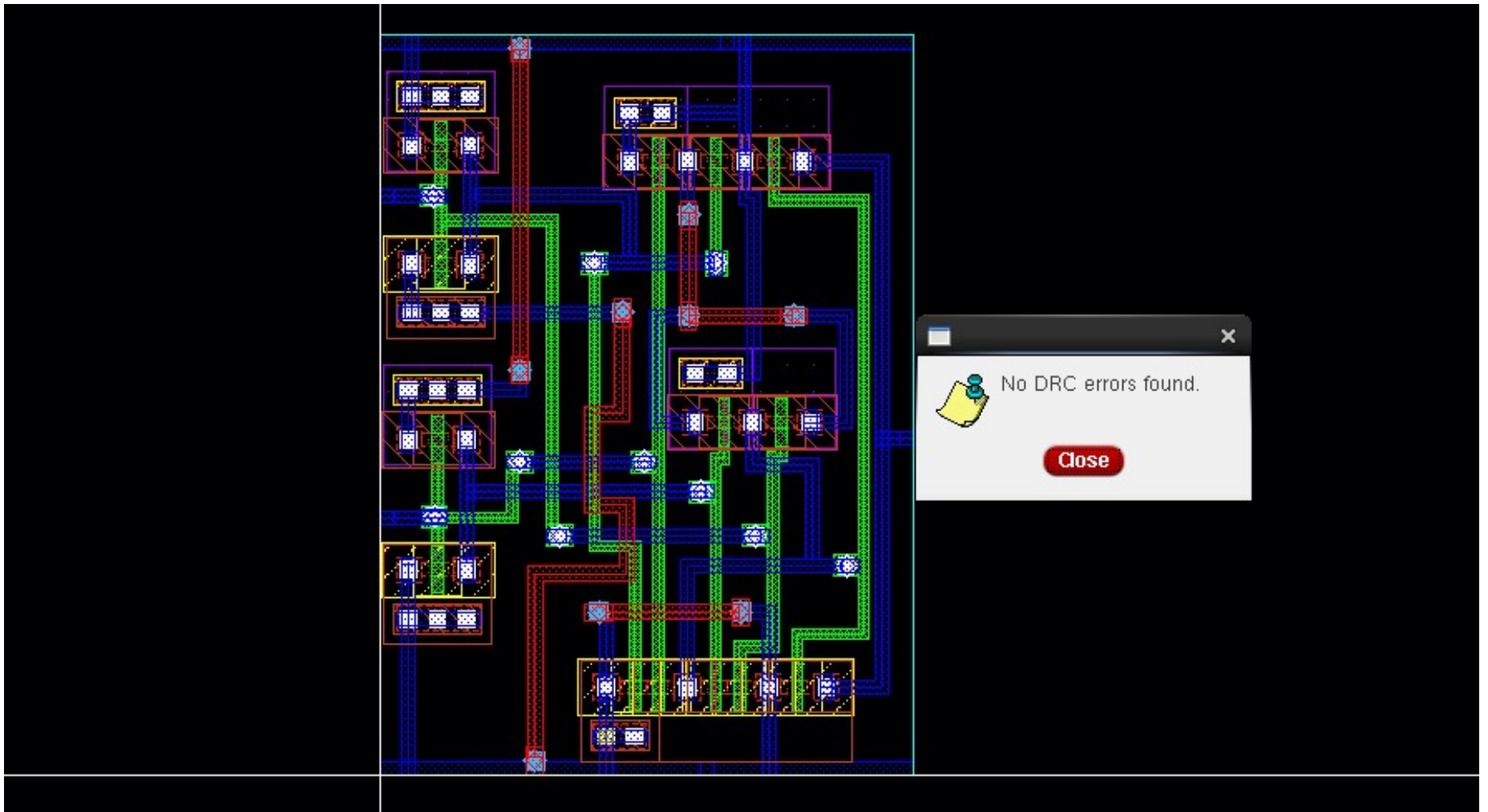


# Layout

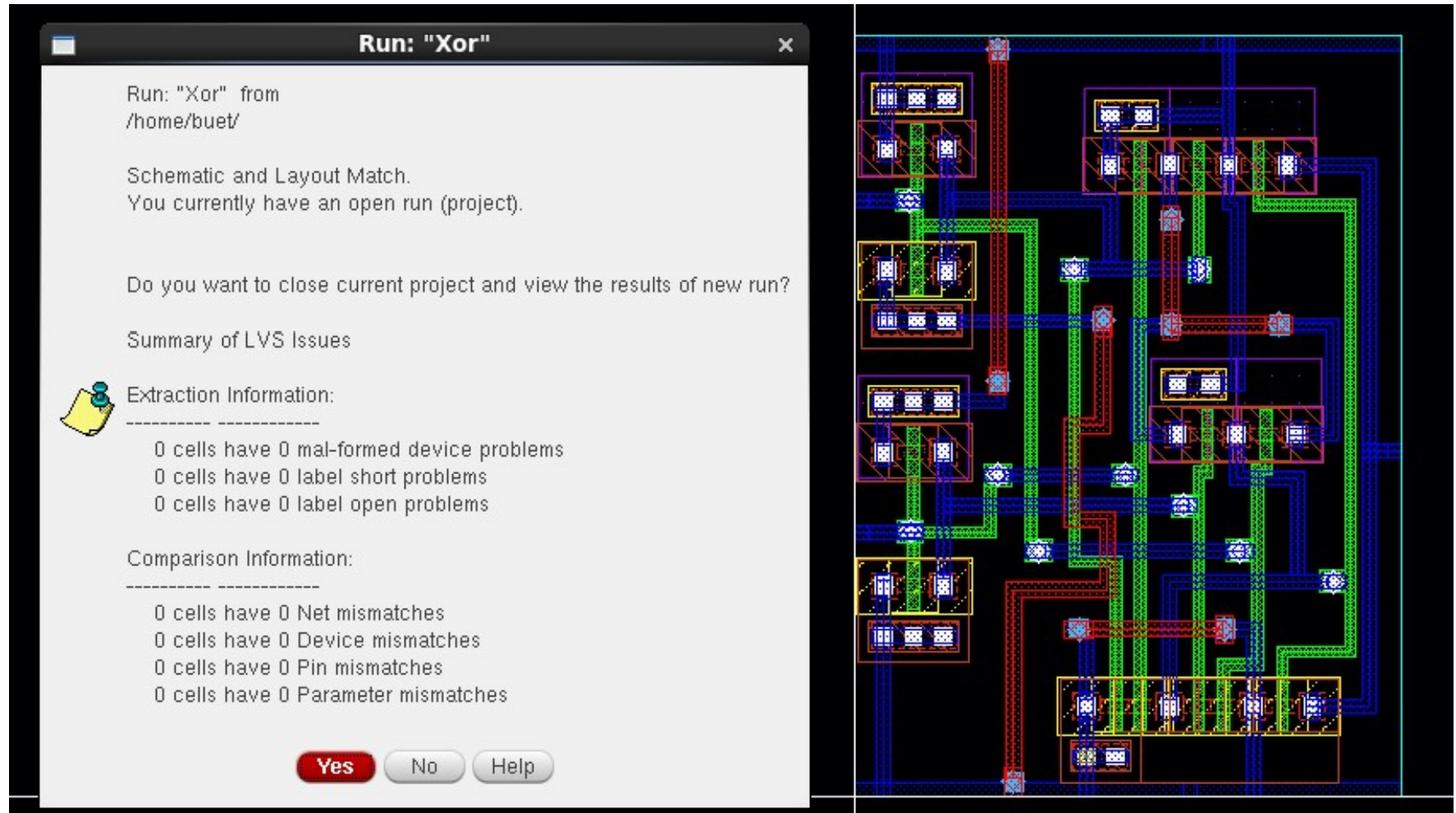




# No DRC Error found



# LVS with No mismatch




The image displays a software window titled "Run: 'Xor'" with a close button (X) in the top right corner. The window contains the following text:

Run: "Xor" from  
/home/buet/

Schematic and Layout Match.  
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

 Extraction Information:

-----

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

Comparison Information:

-----

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

At the bottom of the window are three buttons: "Yes" (highlighted in red), "No", and "Help".

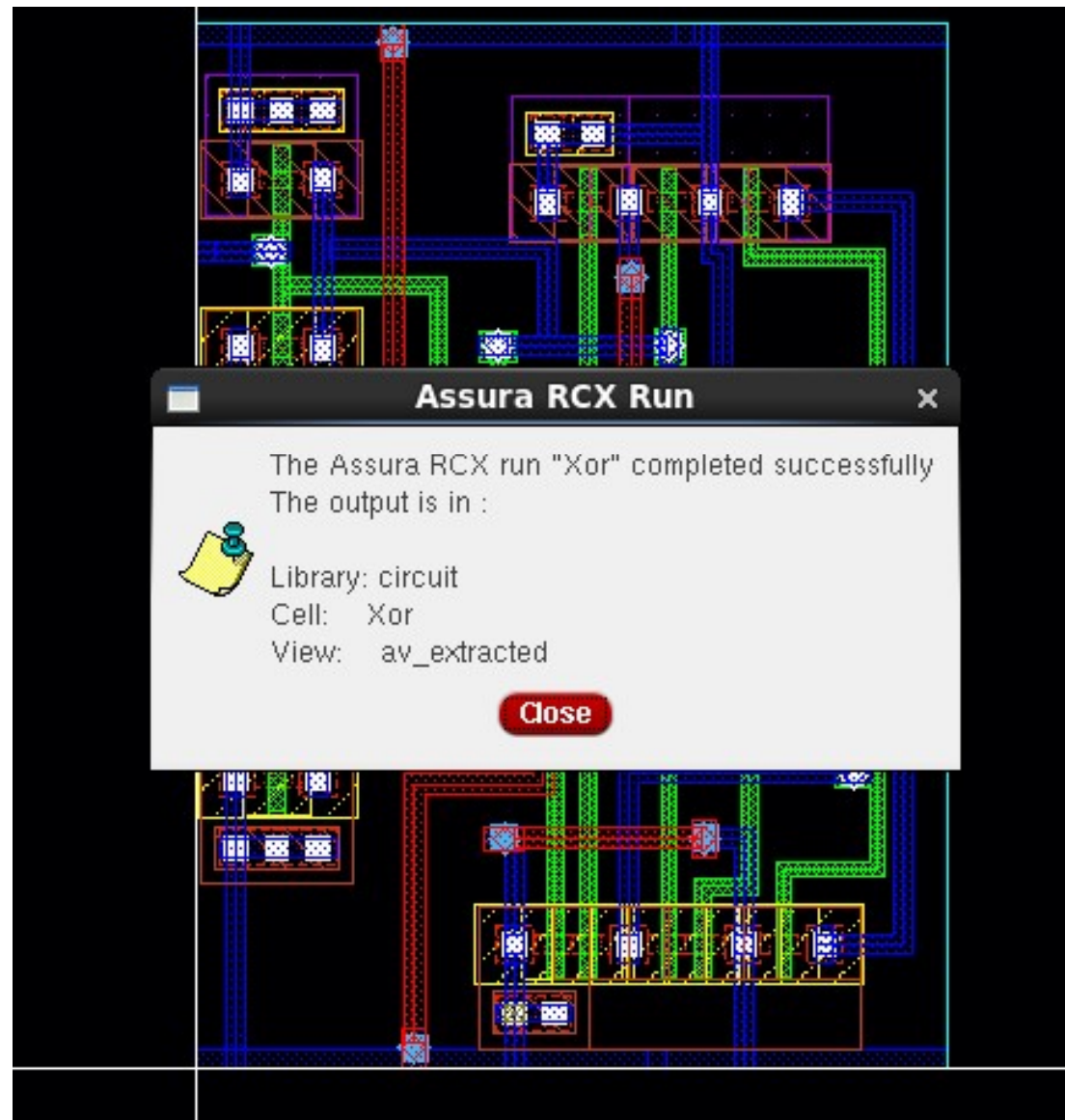
To the right of the window is a circuit layout diagram. It features a grid of components, including logic gates and multiplexers, interconnected by a dense network of colored lines (red, green, blue, and yellow) representing signal traces. The components are arranged in a structured, hierarchical manner, typical of a digital circuit design.

# LVS Matched





# RCX Run



# AV Extraction View

