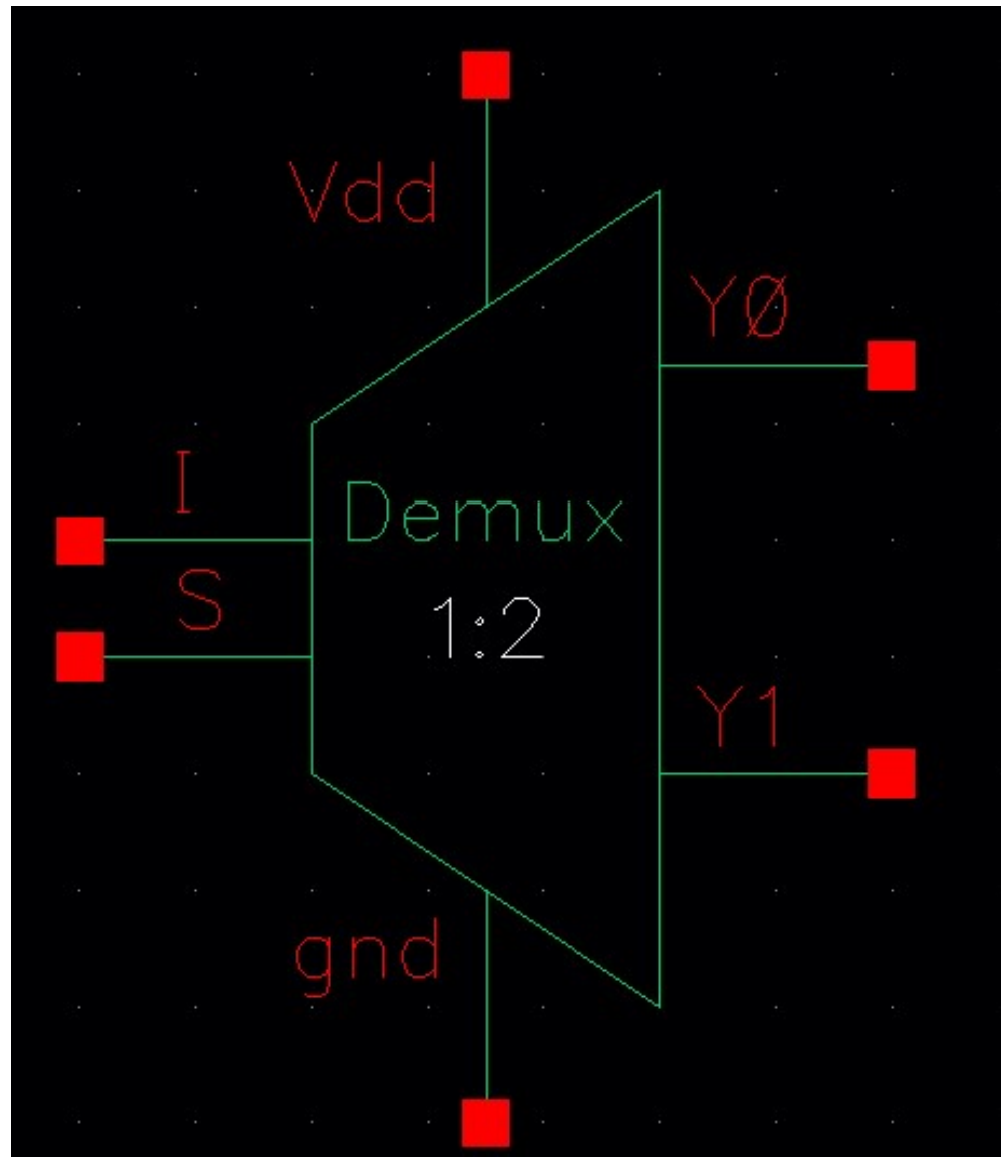
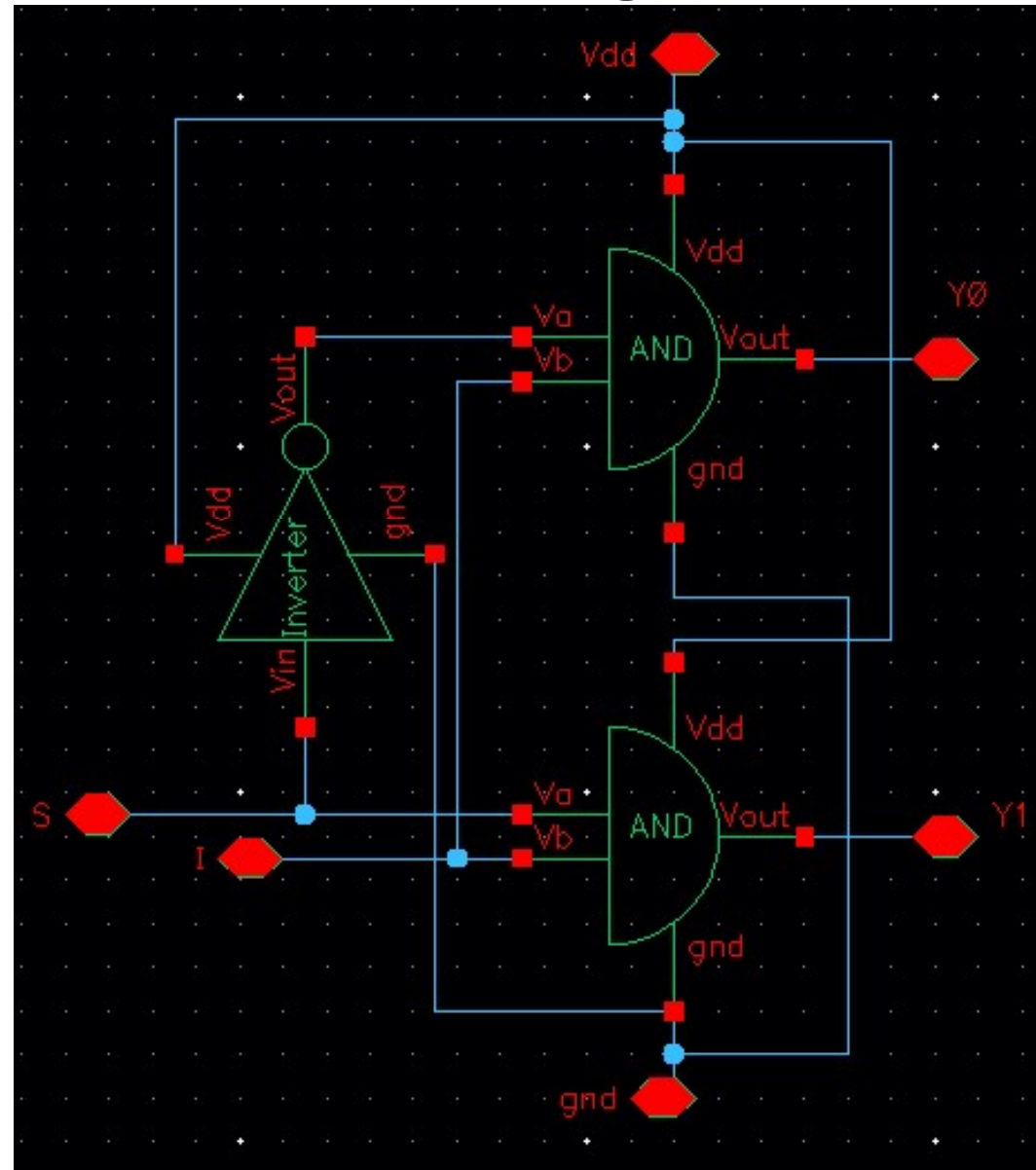


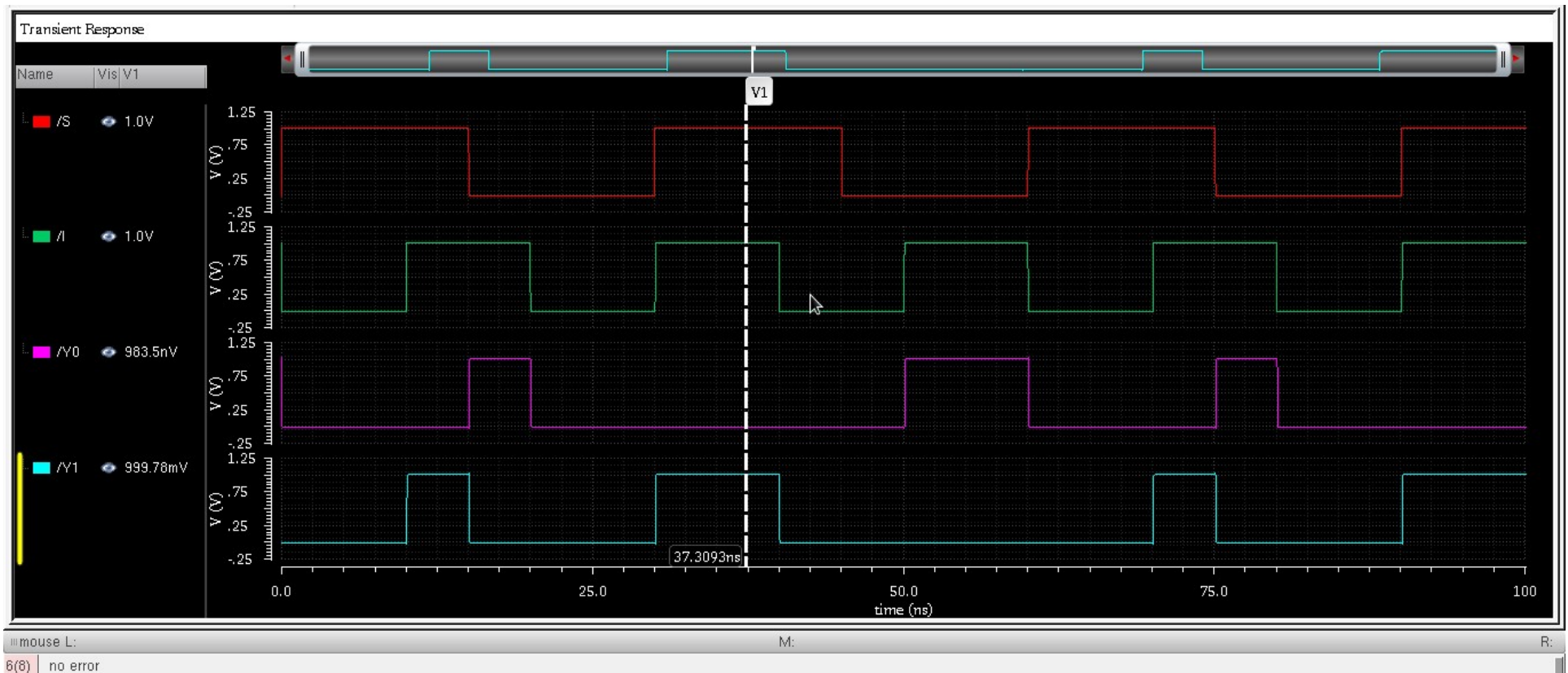
Symbolic Representation



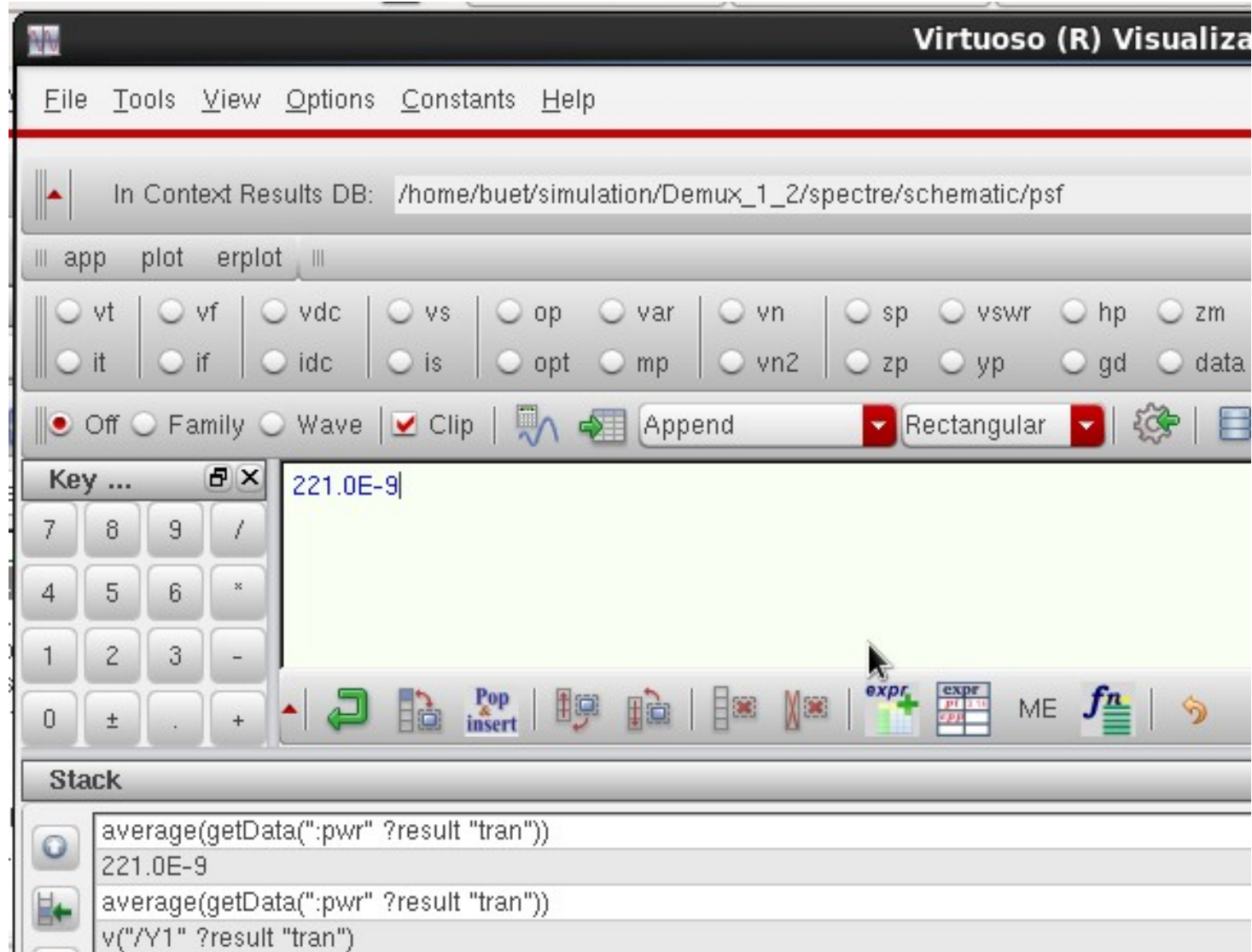
Schematic Representation



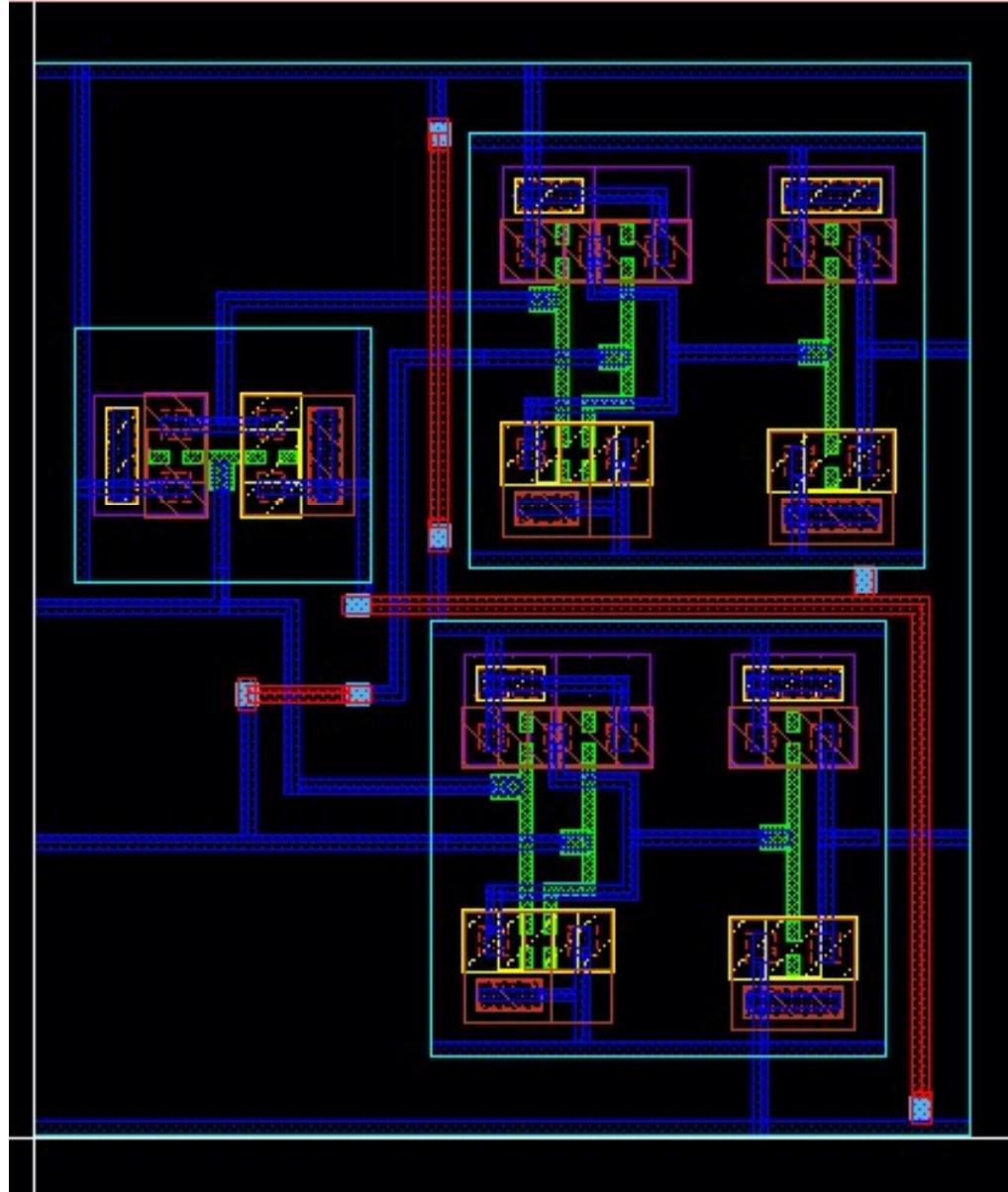
Transient Waveform



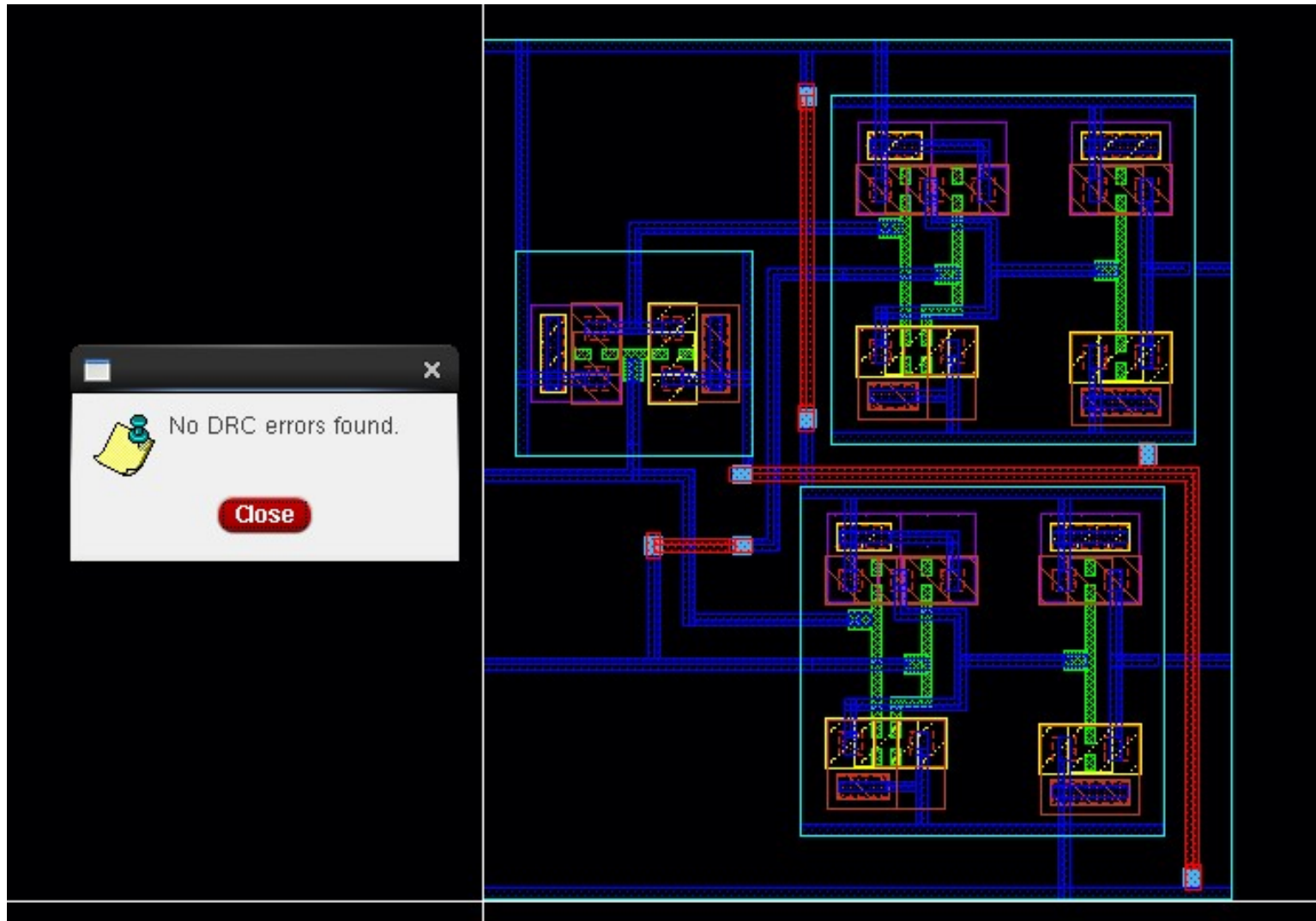
Power Consumption



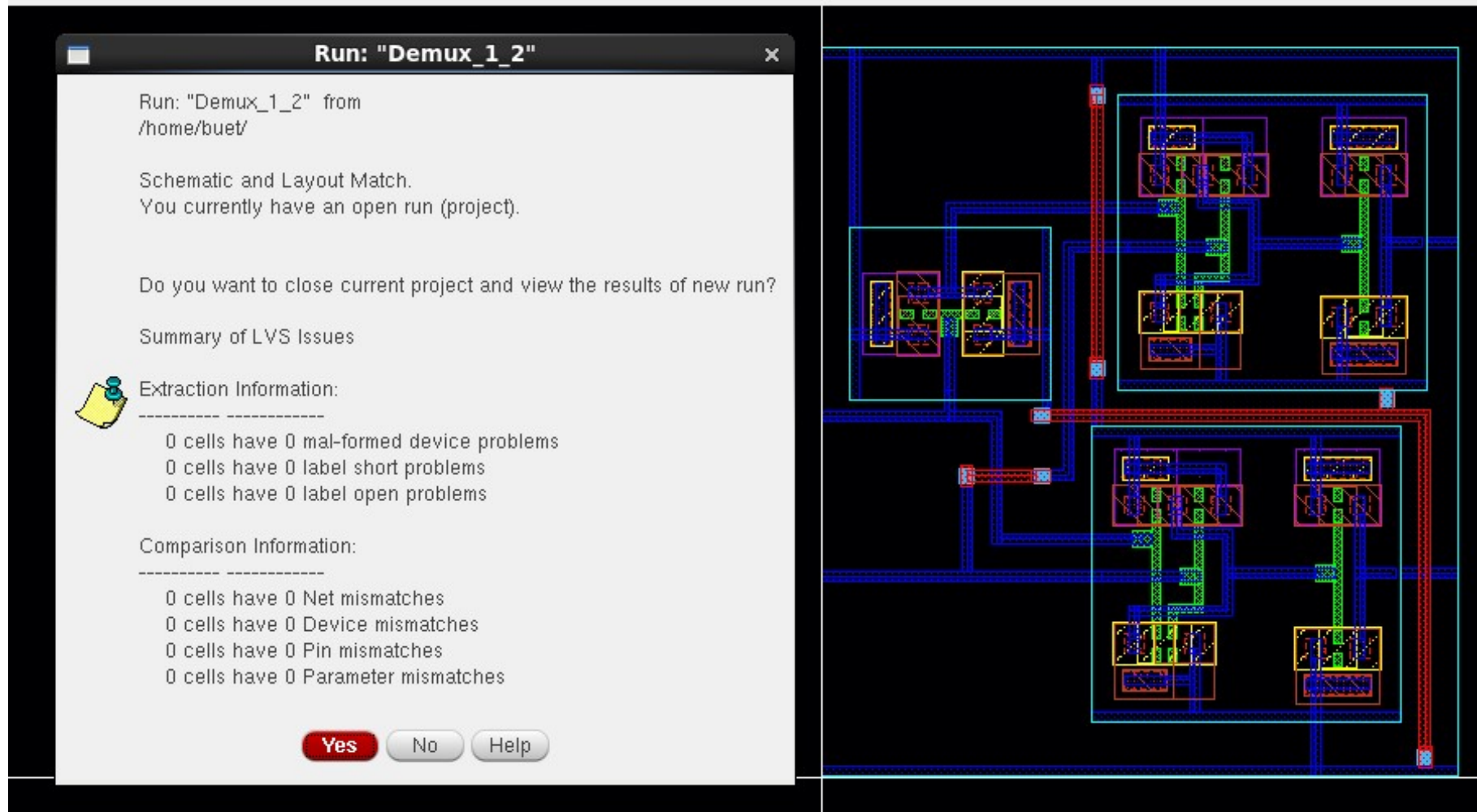
Layout



No DRC Error found



LVS with No mismatch




Run: "Demux_1_2"

Run: "Demux_1_2" from
/home/buet/

Schematic and Layout Match.
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

 Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

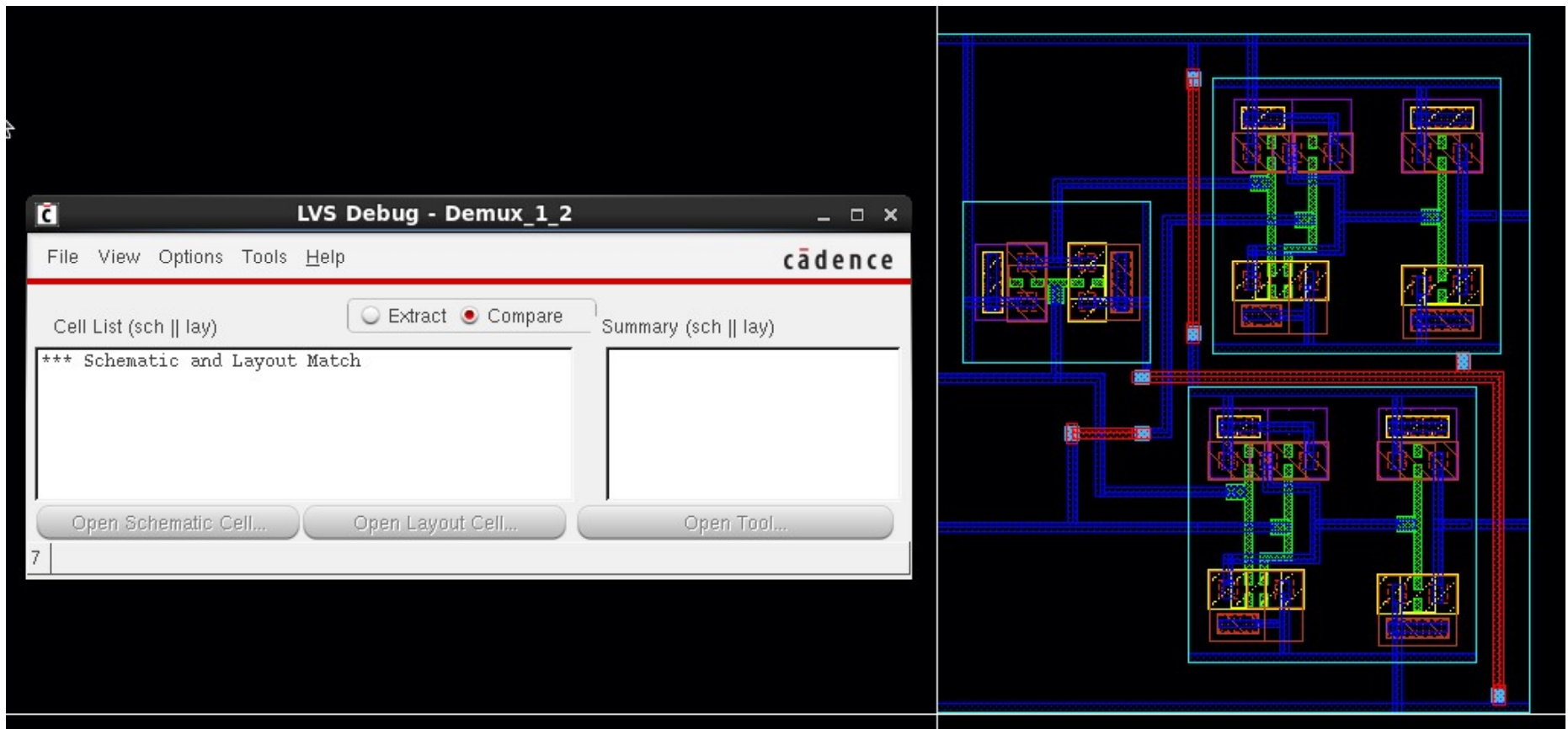
Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

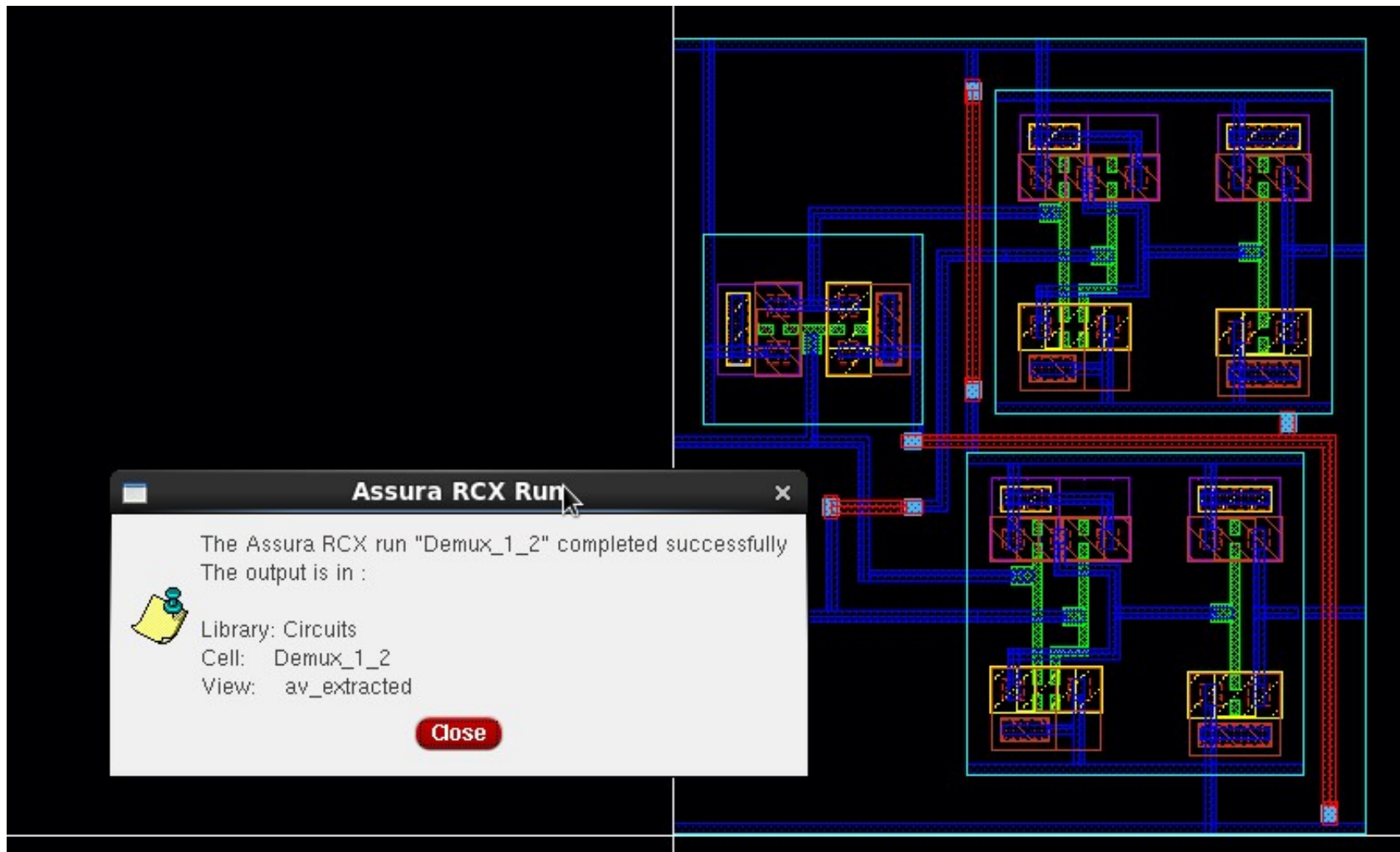
Yes No Help

The right side of the image shows a circuit layout diagram. It features several rectangular components, some with internal patterns, interconnected by a network of blue and red lines representing signal traces. The layout is organized into a grid-like structure with various connection points and junctions.

LVS Matched



RCX Run



AV Extraction View

