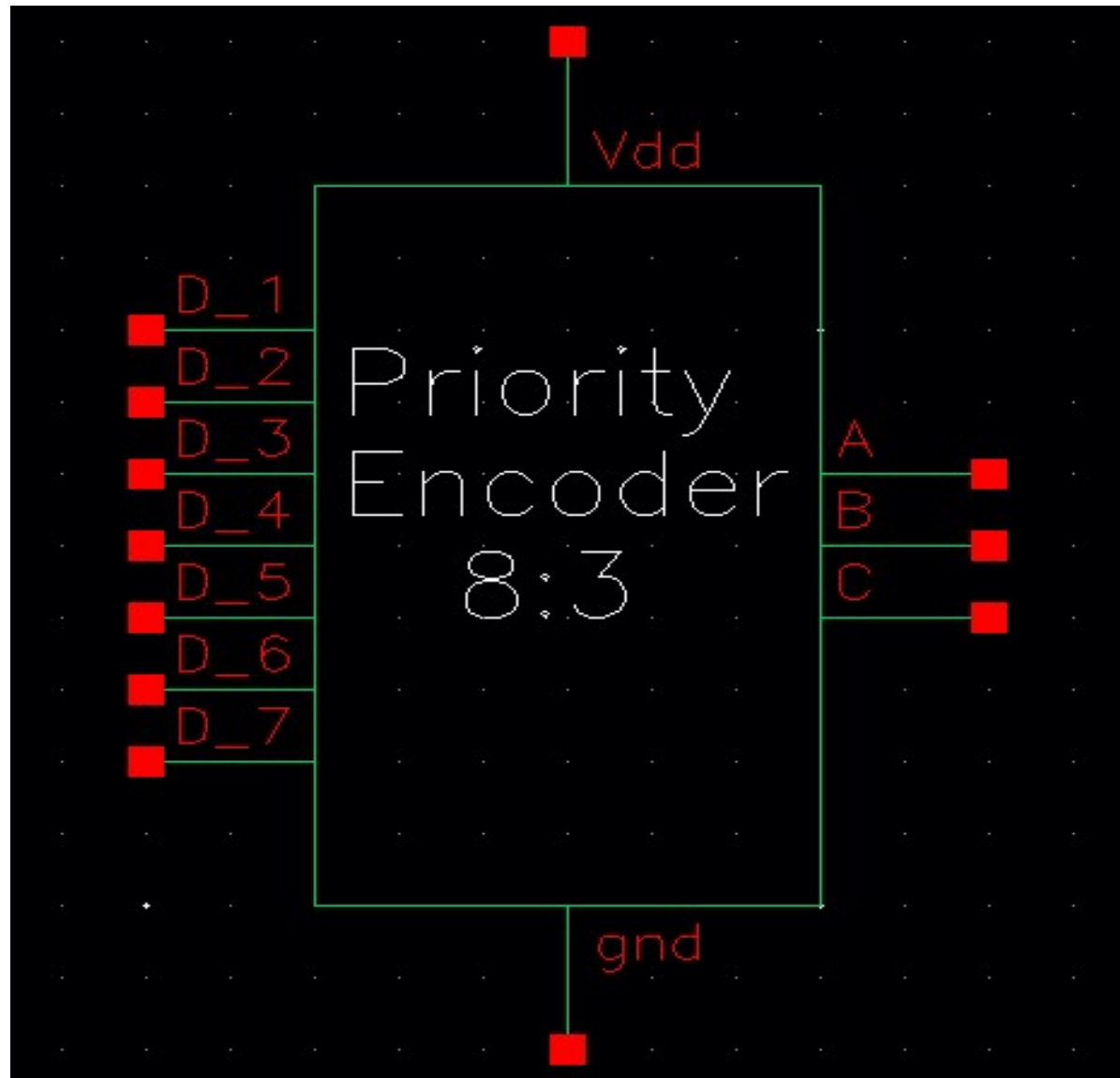
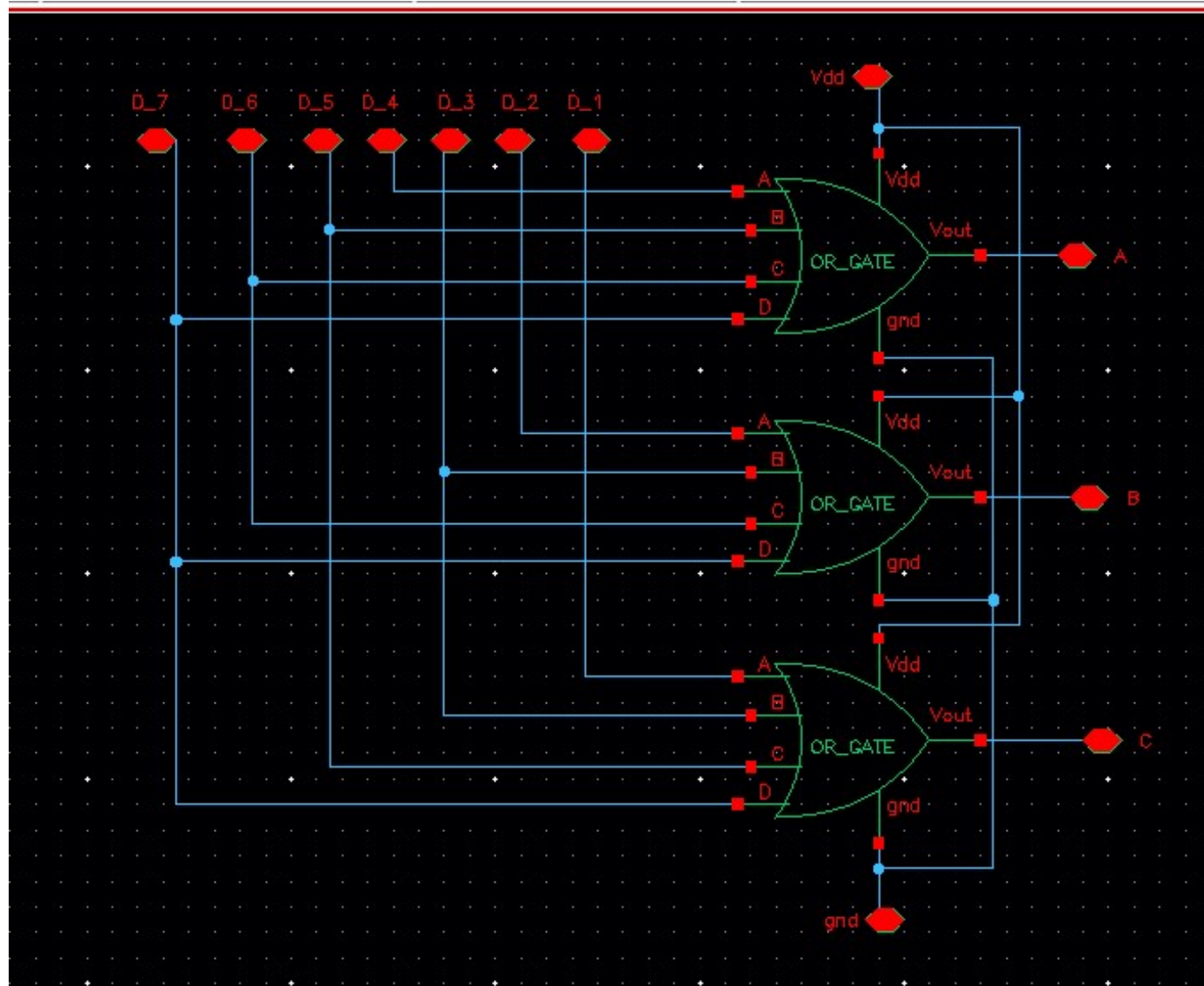


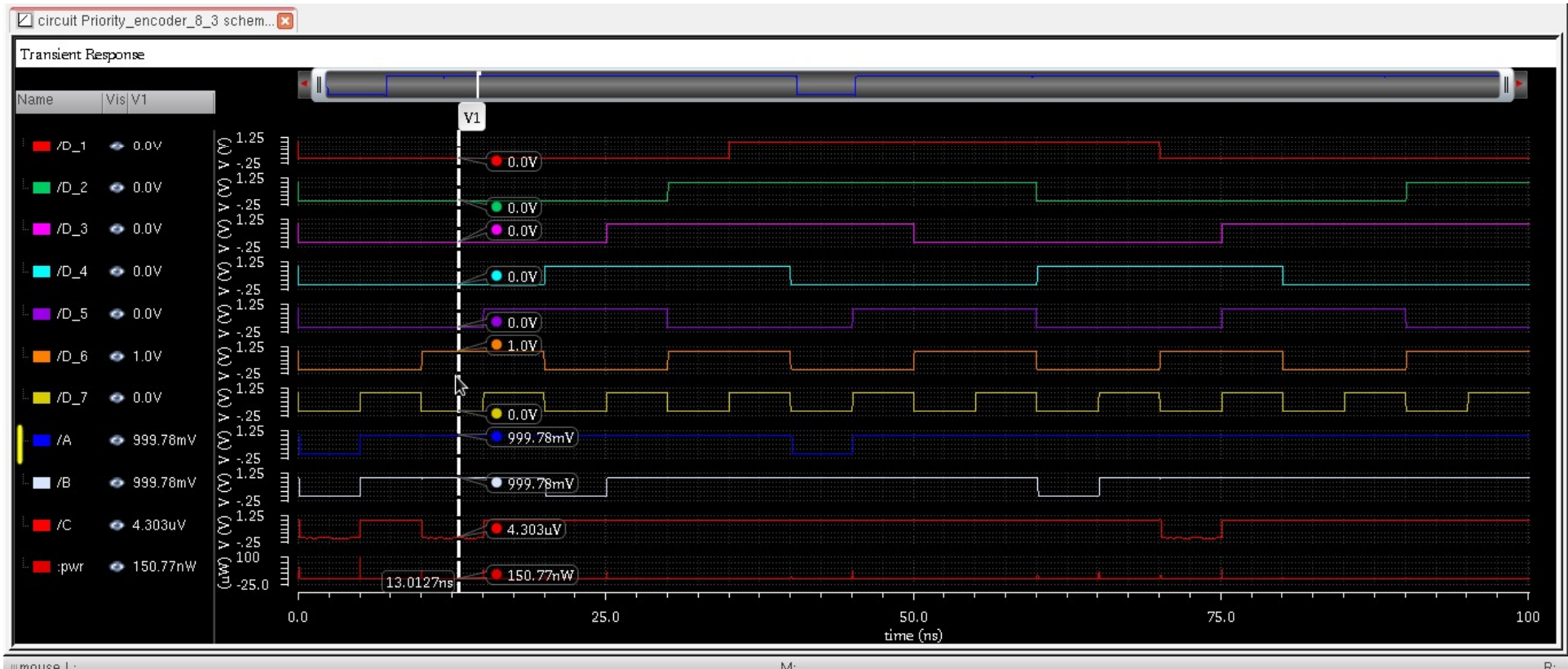
# Symbolic Representation



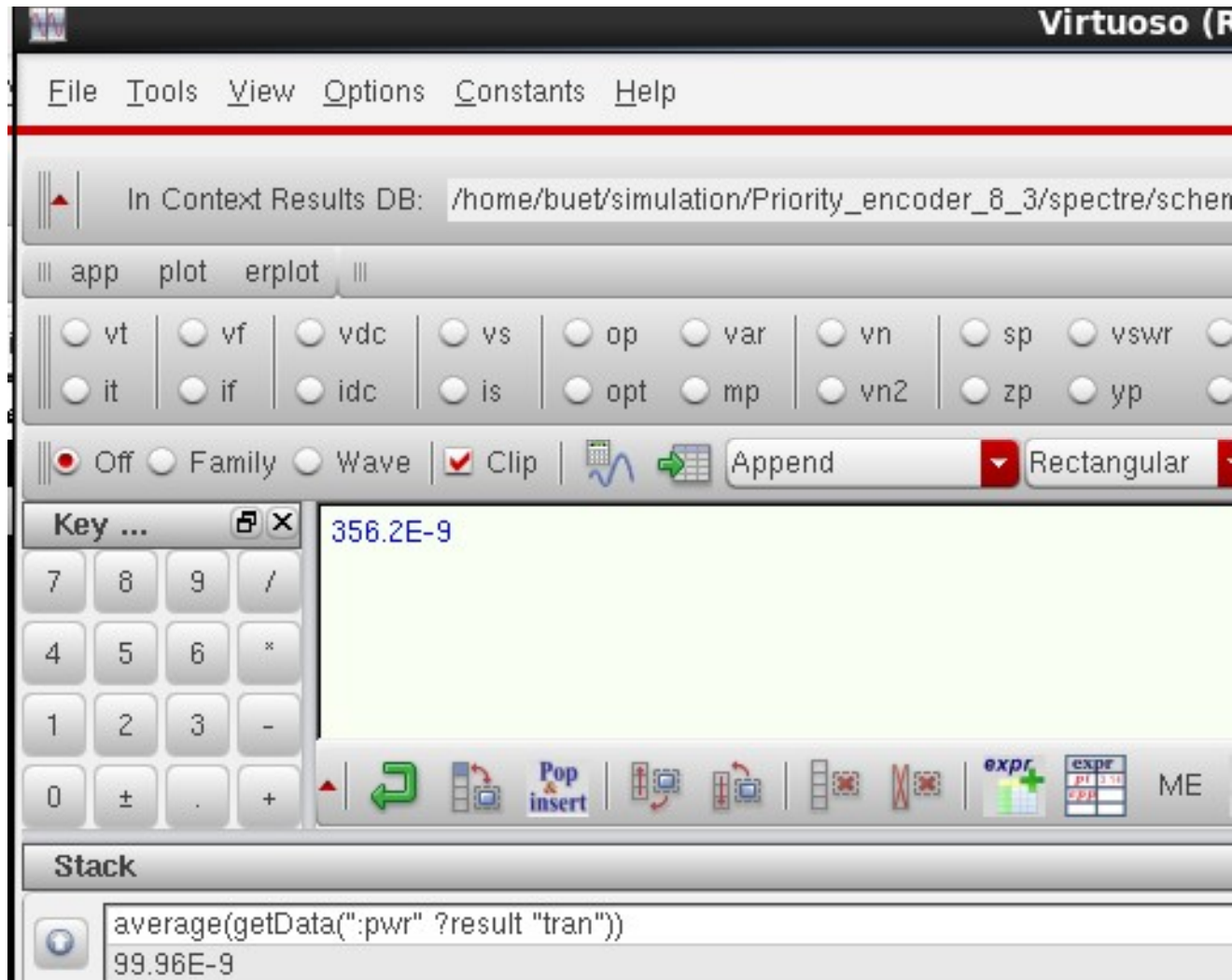
# Schematic Representation



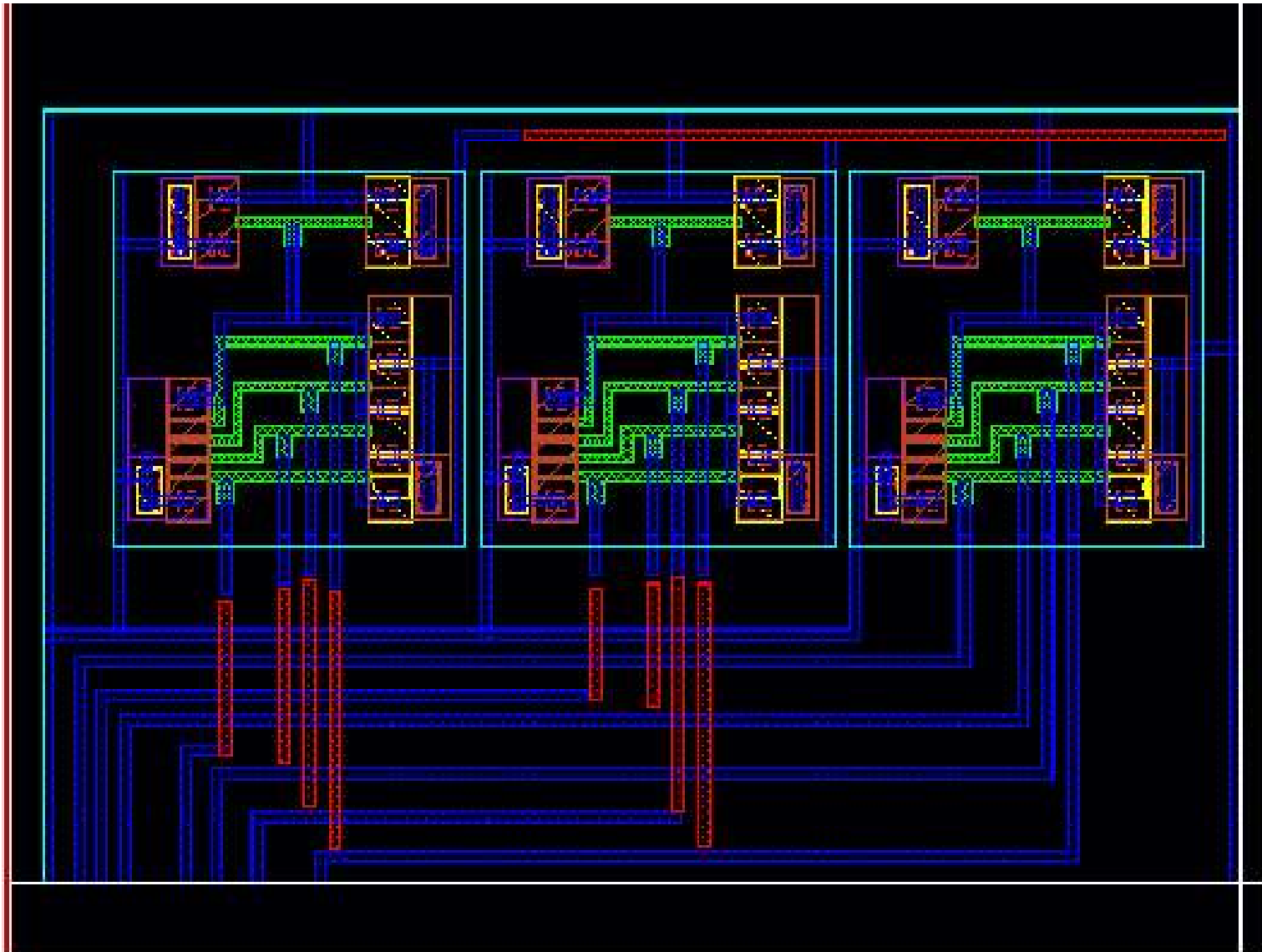
# Transient Waveform



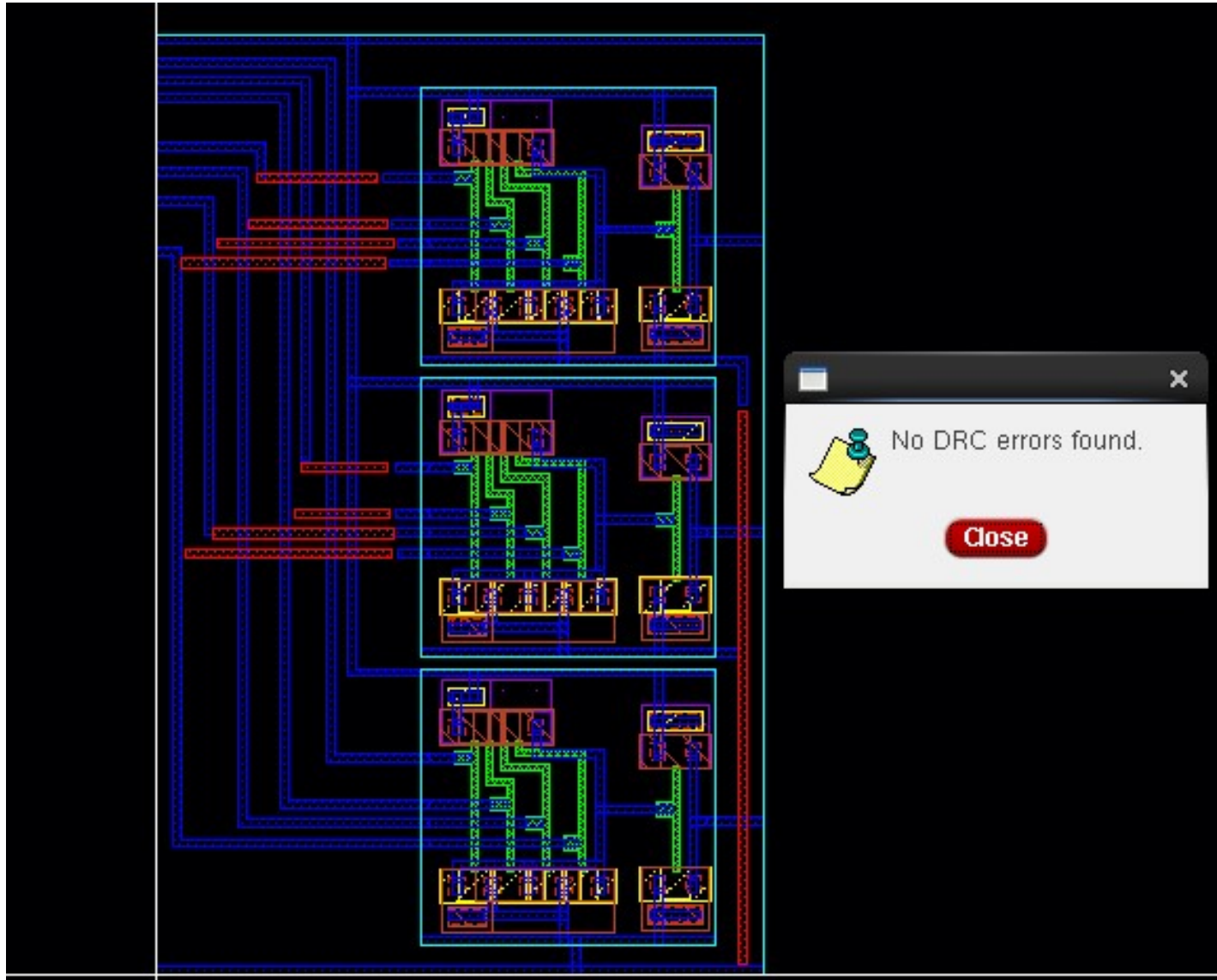
# Power Consumption



# Layout

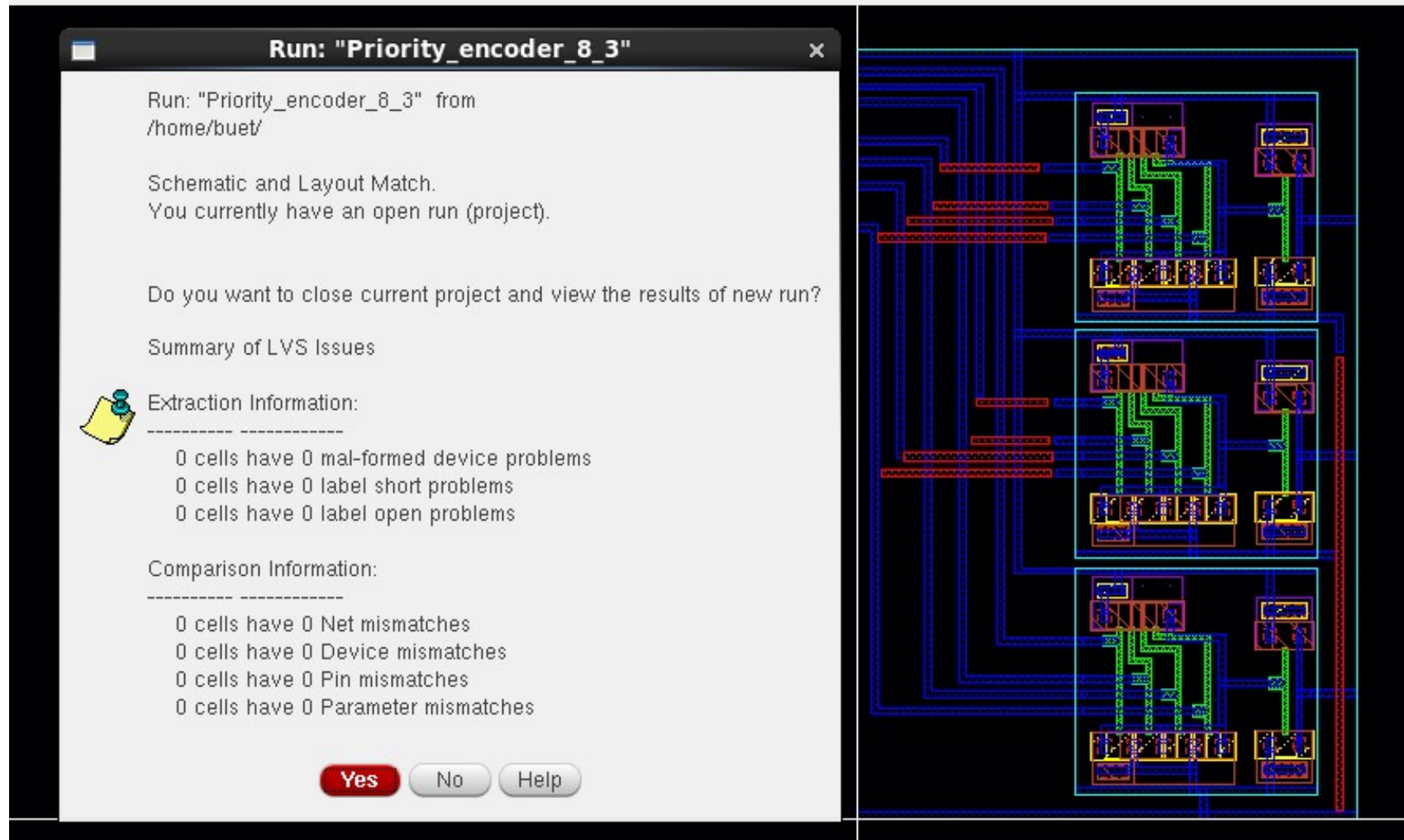


# No DRC Error found





# LVS with No mismatch



Run: "Priority\_encoder\_8\_3"

Run: "Priority\_encoder\_8\_3" from  
/home/buet/

Schematic and Layout Match.  
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

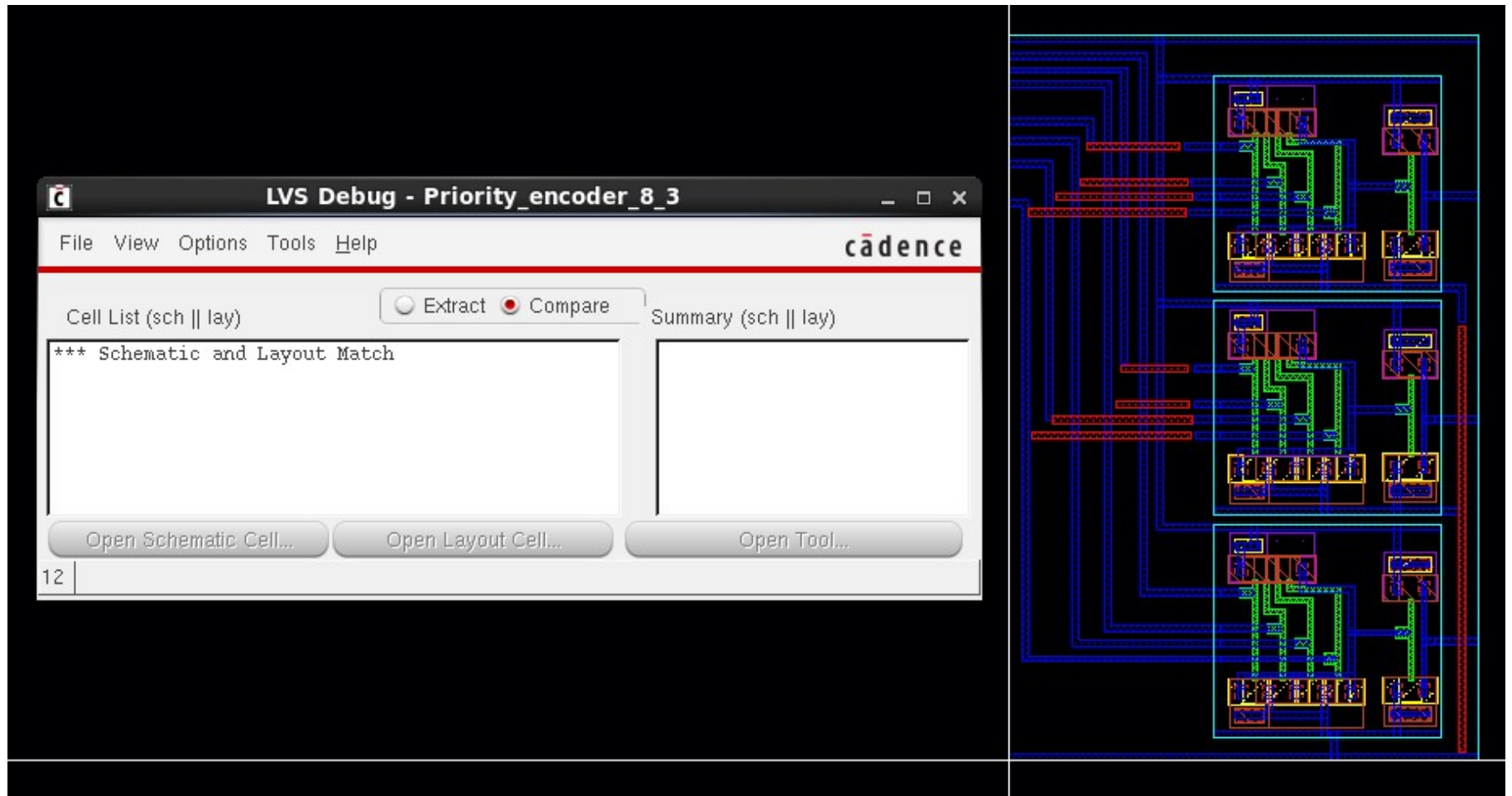
Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

Yes No Help

The right side of the image shows a detailed circuit layout diagram. It features a grid of blue lines representing routing channels. Various components, represented by colored rectangles (yellow, red, green, and blue), are placed within this grid. These components are interconnected by a network of colored lines (red, green, blue, and yellow) that trace the paths of the circuit signals across the layout.

# LVS Matched





# RCX Run



# AV Extraction View

