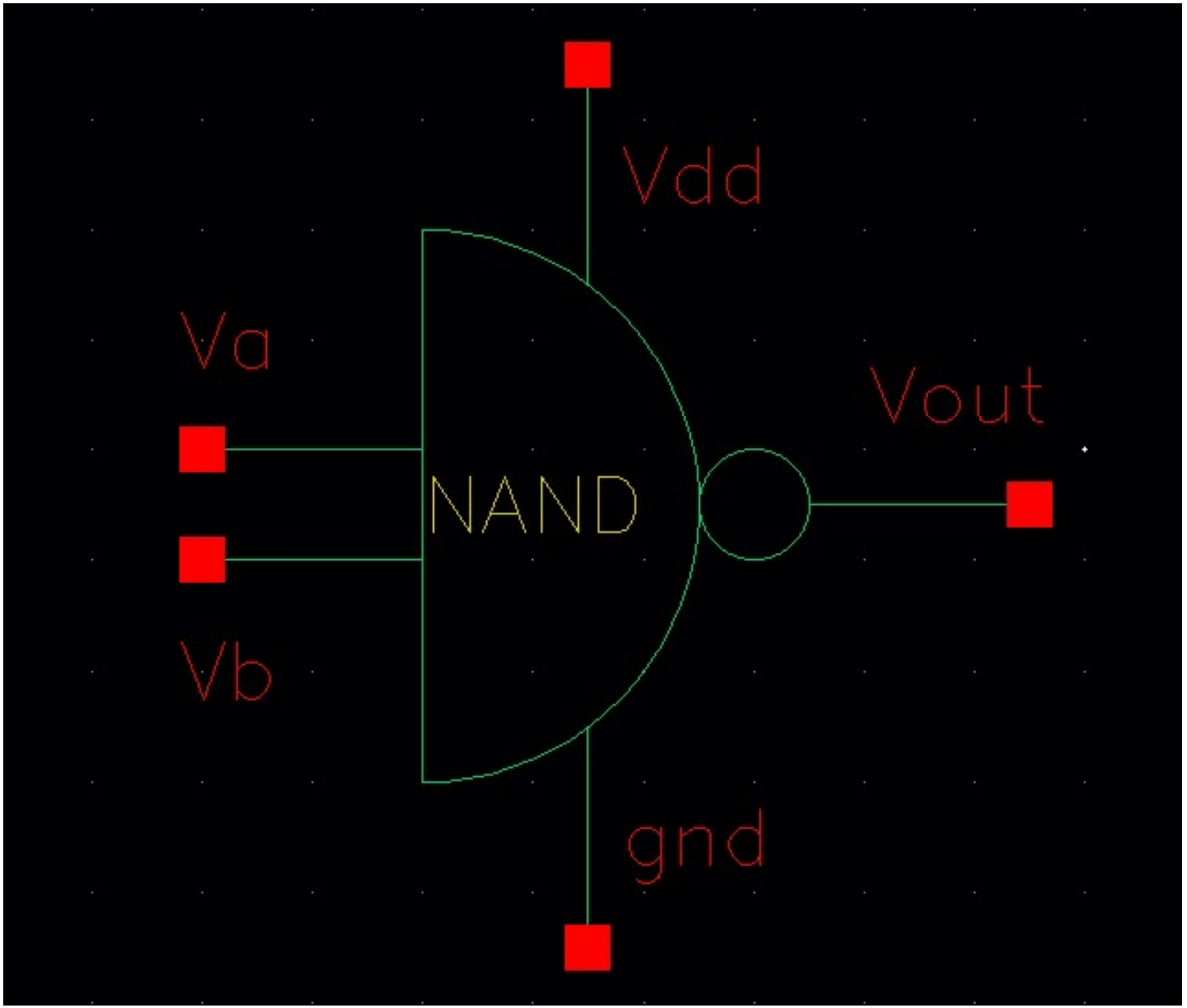
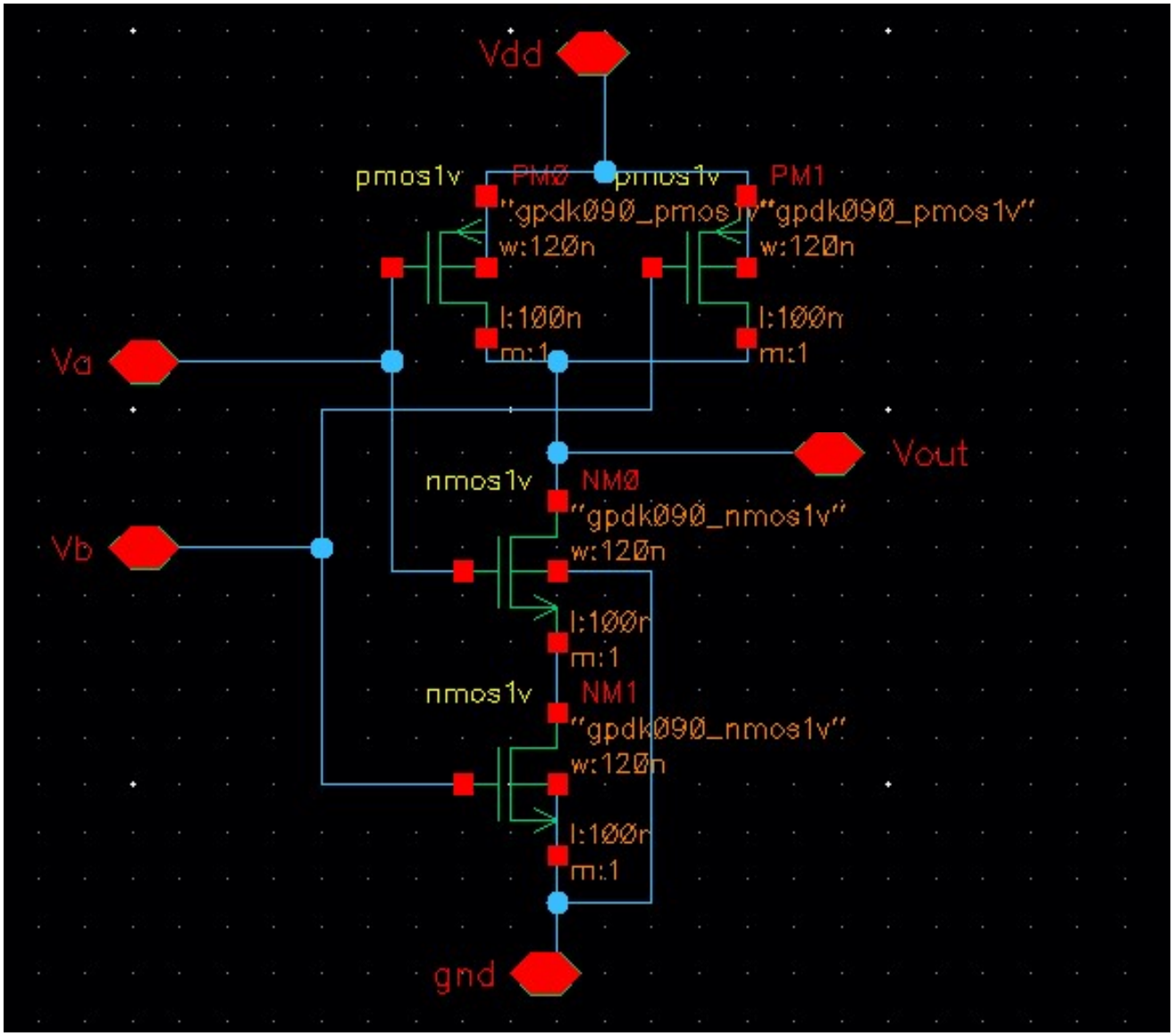
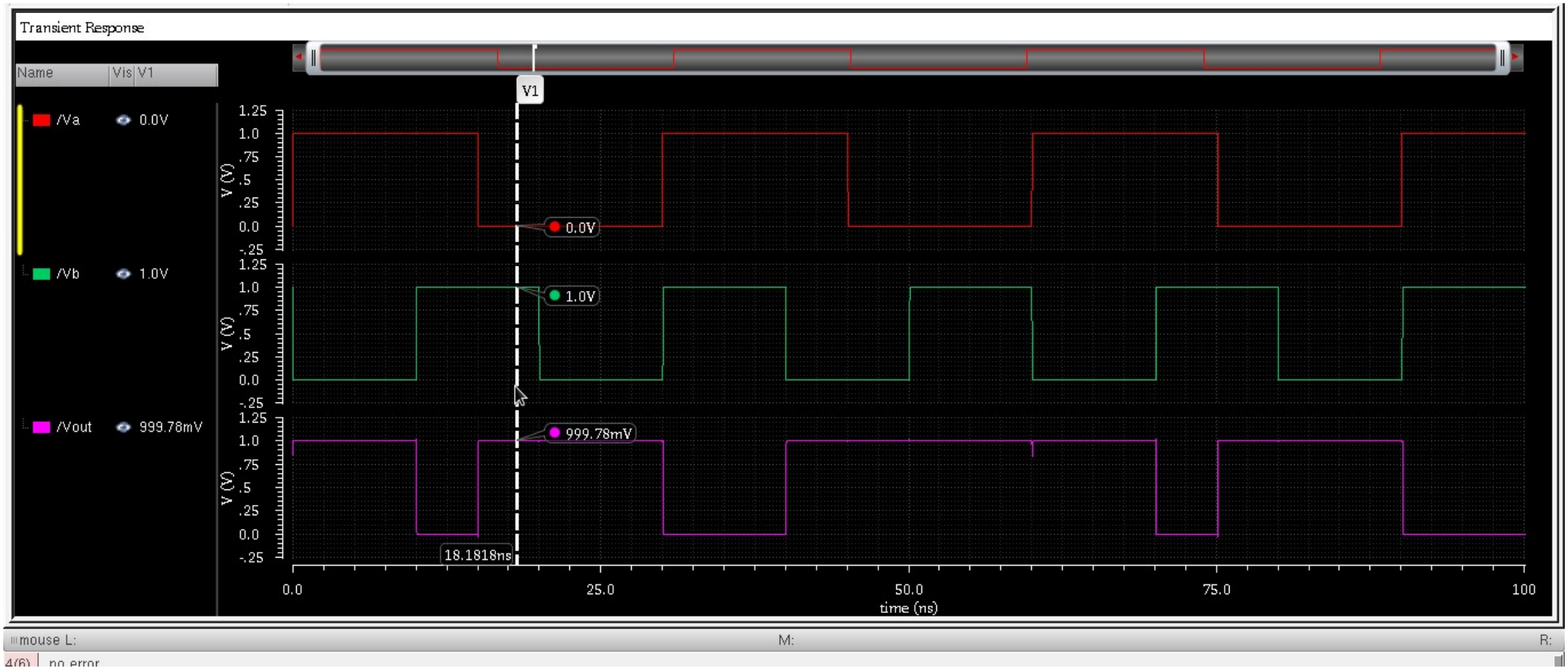
Symbolic Representation



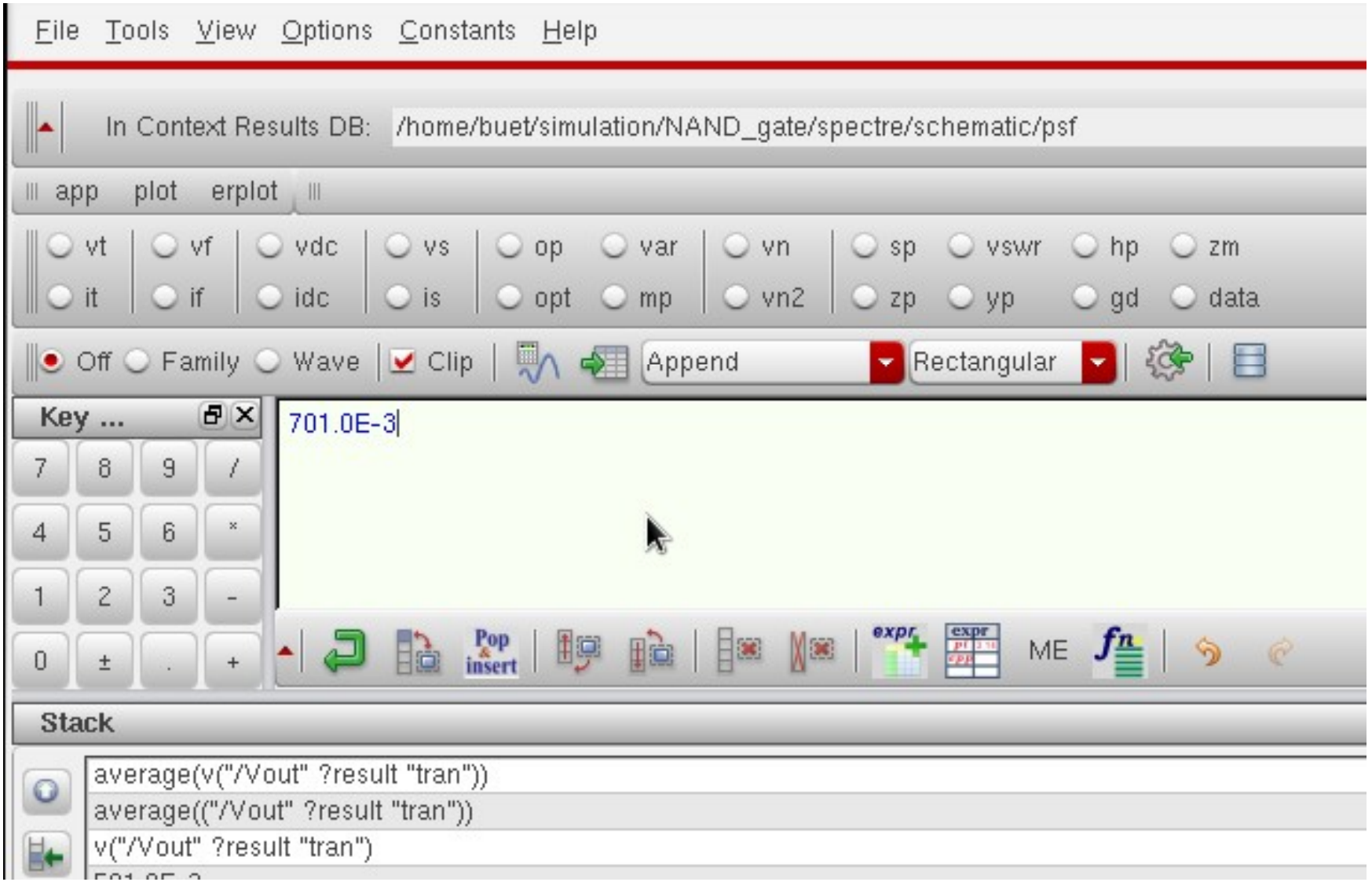
Schematic Representation



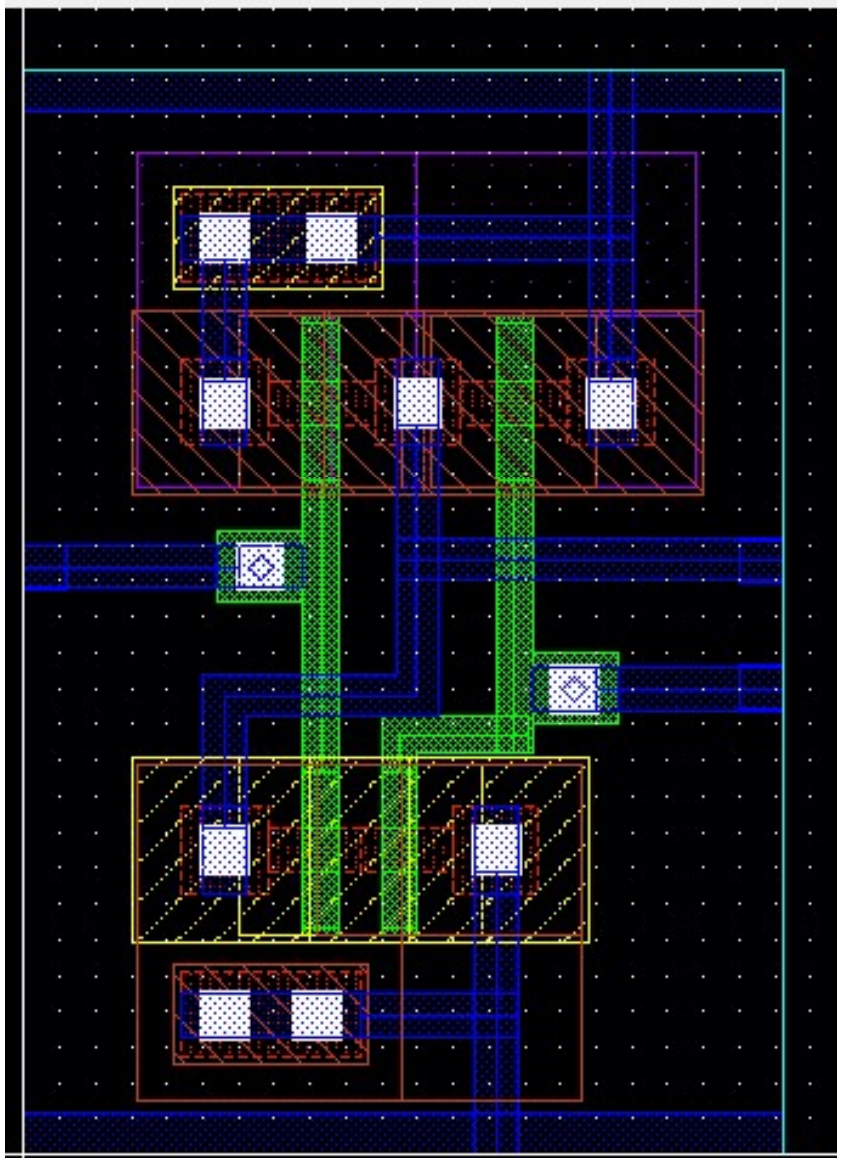
Transient Waveform



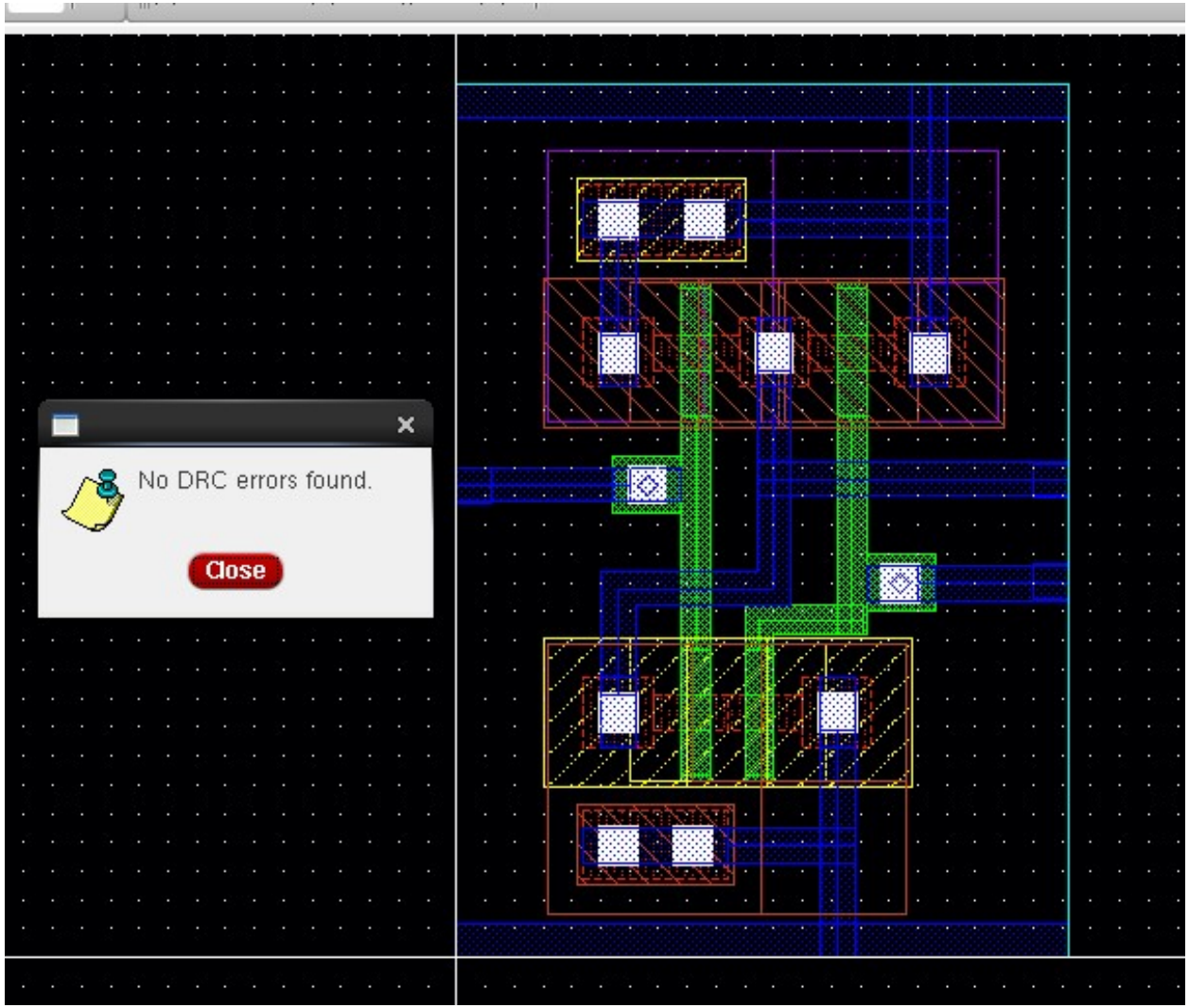
Power Consumption



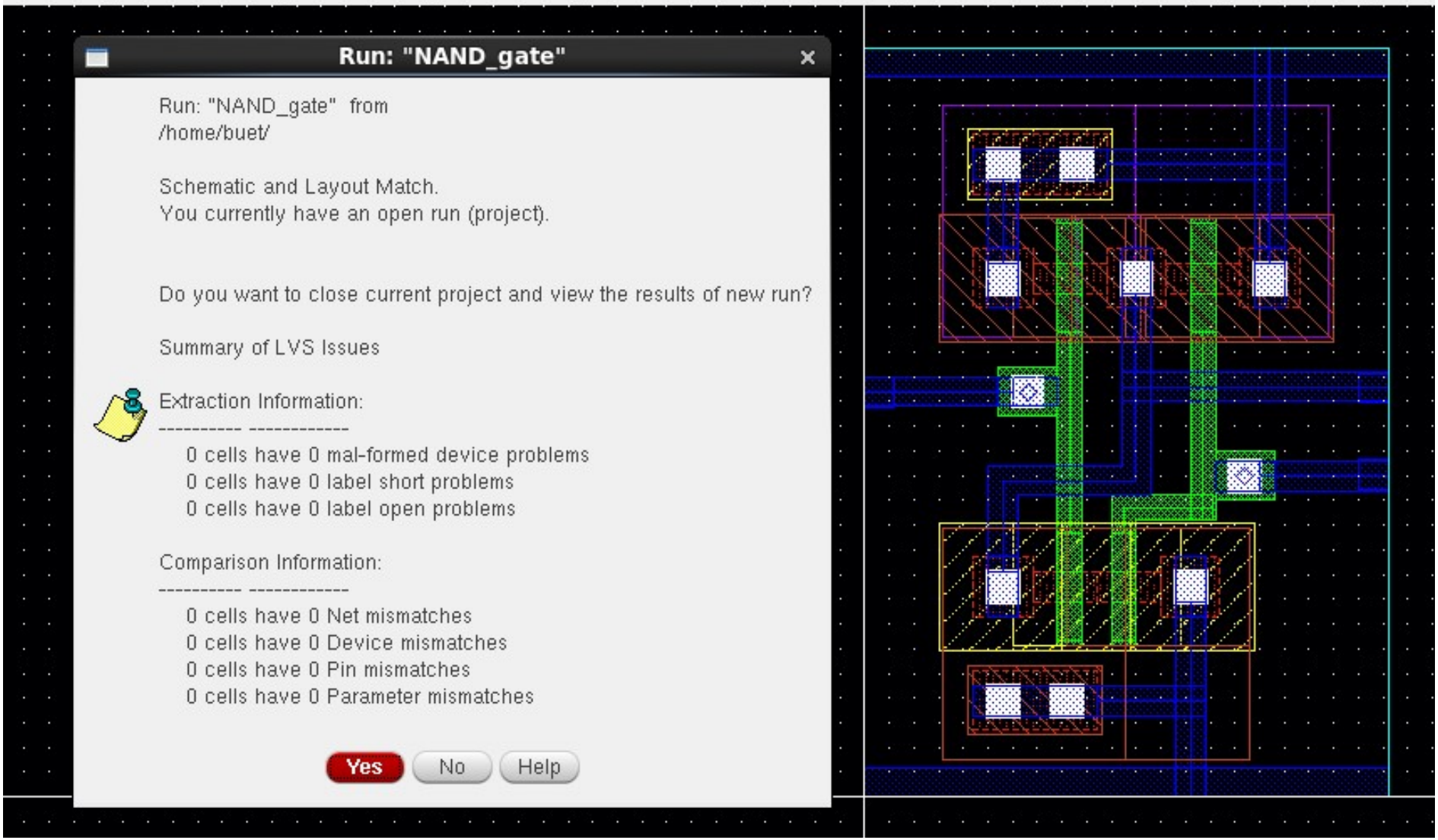
Layout



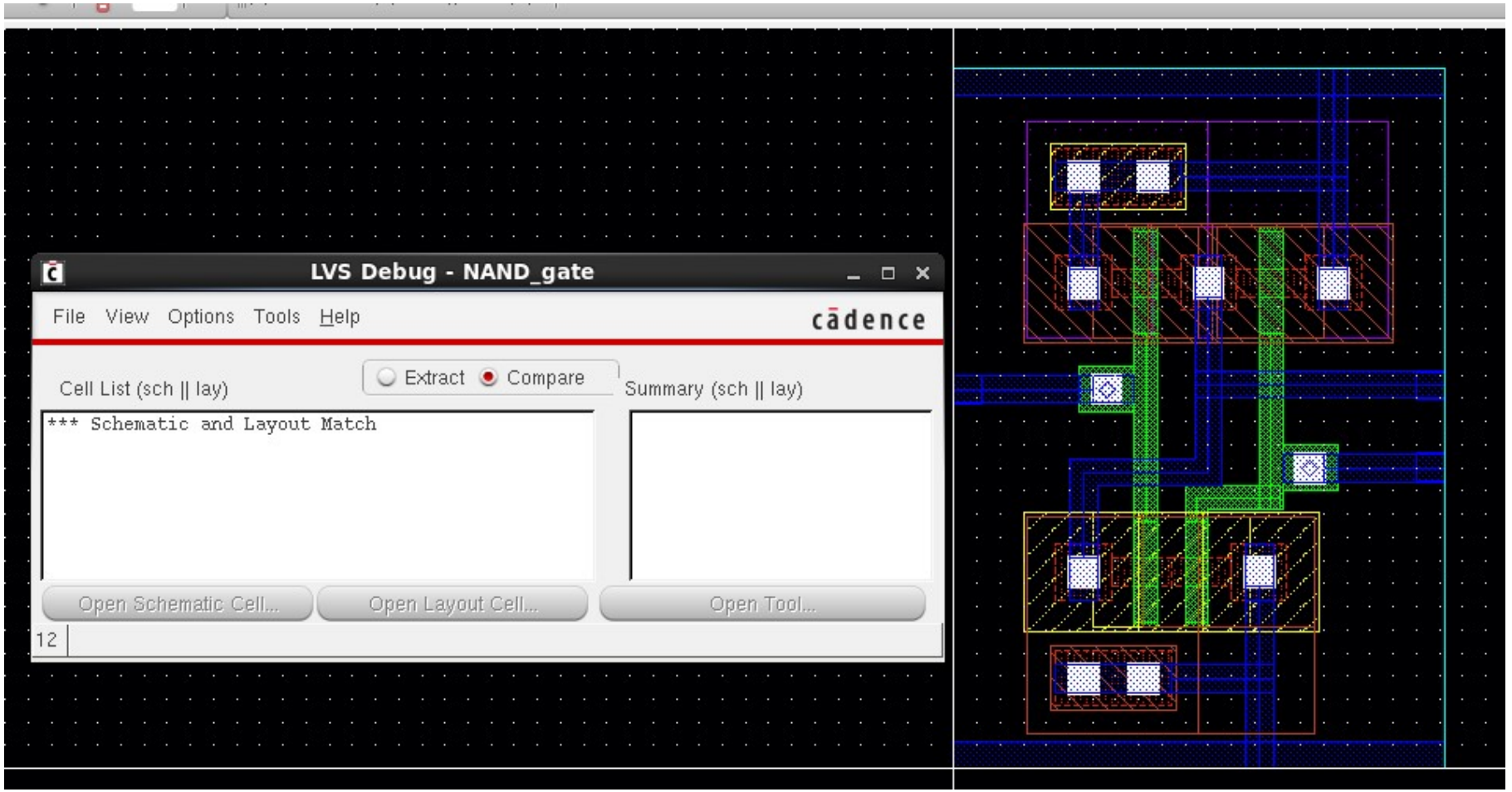
No DRC Error found



LVS with No mismatch



LVS Matched


LVS Debug - NAND_gate
File View Options Tools Help
cadence
Extract Compare
Cell List (sch || lay)
Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...
12

RCX Run


Assura RCX Run
The Assura RCX run "NAND_gate" completed successfully
The output is in :
Library: Circuit
Cell: NAND_gate
View: av_extracted
Close

AV Extraction View