Assignment #3 - Report

Verilog Design of Combinational and Sequential Unsigned Multipliers

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Combinational Unsigned Binary Multiplier(Array Multiplier):

1. Hardware Requirements: 16 Half Adders, 10 Full Adders, 36 AND Gates, 24 I/O Ports, 84 nets

2. Maximum Speed of Operation: infinity

Sequential Unsigned Binary Multiplier (Left-Shift Version):

1. Hardware Requirements: 37 cells, 27 I/O Ports, 112 nets

2. Maximum Speed of Operation: infinity

Sequential Unsigned Binary Multiplier (Right-Shift Version):

1. Hardware Requirements: 53 cells, 27 I/O Ports, 170 nets

2. Maximum Speed of Operation: infinity