# **Assignment #2 - Report**

## **Verilog Design of Binary Adders**

#### Group-51

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## **Ripple Carry Binary Adder:**

- 1. Hardware Requirements: 8 Full Adders, 26 I/O, 7 Wires
- 2. Critical Path Delay:

❖ Total Delay: 7.012 ns
 ❖ Logic Delay: 4.012 ns
 ❖ Net Delay: 3.000 ns

### **Hybrid Binary Adder:**

- 1. Hardware Requirements: 2 Carry Lookahead Adders, 26 I/O, 25 Wires
- 2. Critical Path Delay:

❖ Total Delay: 7.012 ns
 ❖ Logic Delay: 4.012 ns
 ❖ Net Delay: 3.000 ns

### **Bit-Serial Binary Adder:**

- Hardware Requirements: 1 D-Flip-Flop, 1 Full Adder, 27 I/O, 17 Wires
- 2. Critical Path Delay:

❖ Total Delay: 4.037 ns
❖ Logic Delay: 3.237 ns
❖ Net Delay: 0.800 ns
❖ Clock Time Period: 5 ns