

ELECTRICAL & COMPUTER ENGINEERING

ENCS2380 – Computer Organization and Microprocessors- Spring 2023 Course Project (I)

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Section : 3

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**Computer design and implementation:**

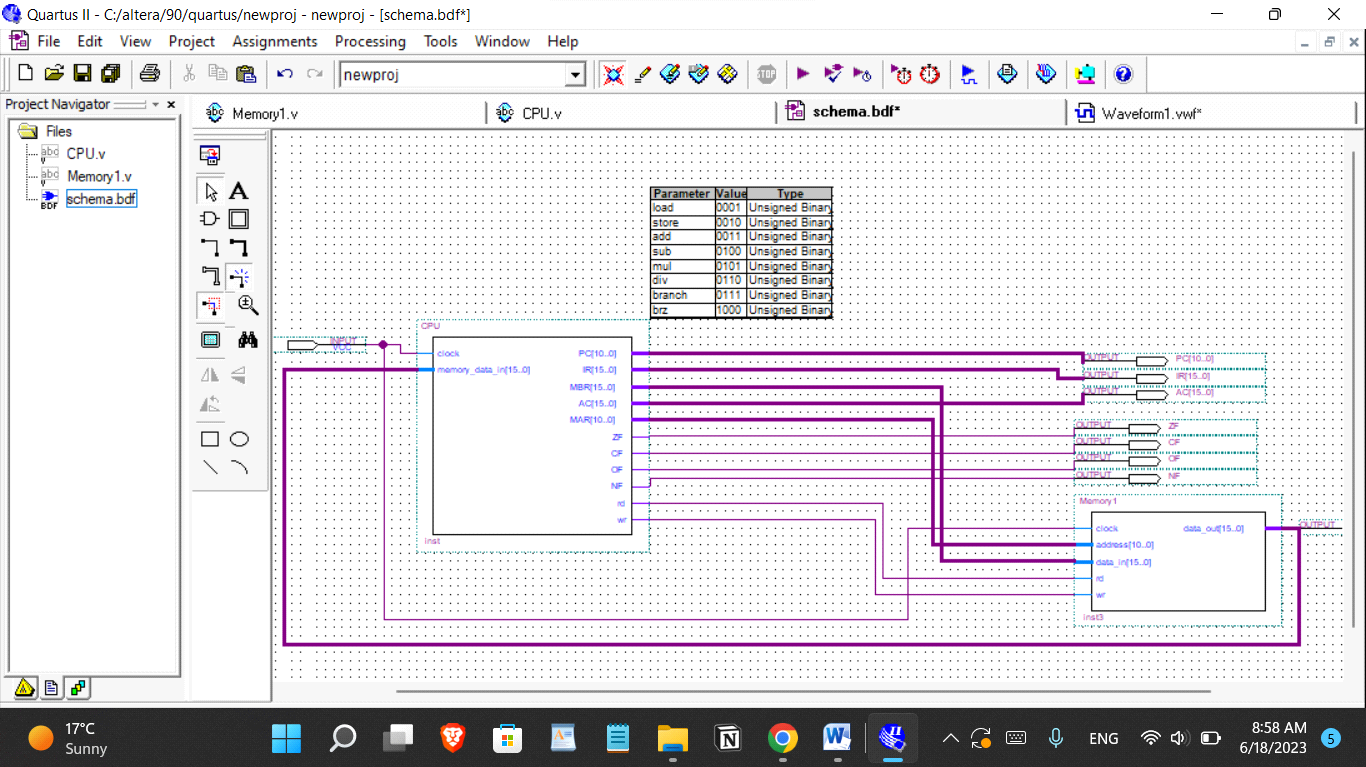
* Design and implement main memory as a Verilog module:

Attached as a Verilog file

2) Design and implement CPU as a Verilog module:

Attached as a Verilog file

3) a snapshot of Design and implement the whole computer:



**Simulation:**

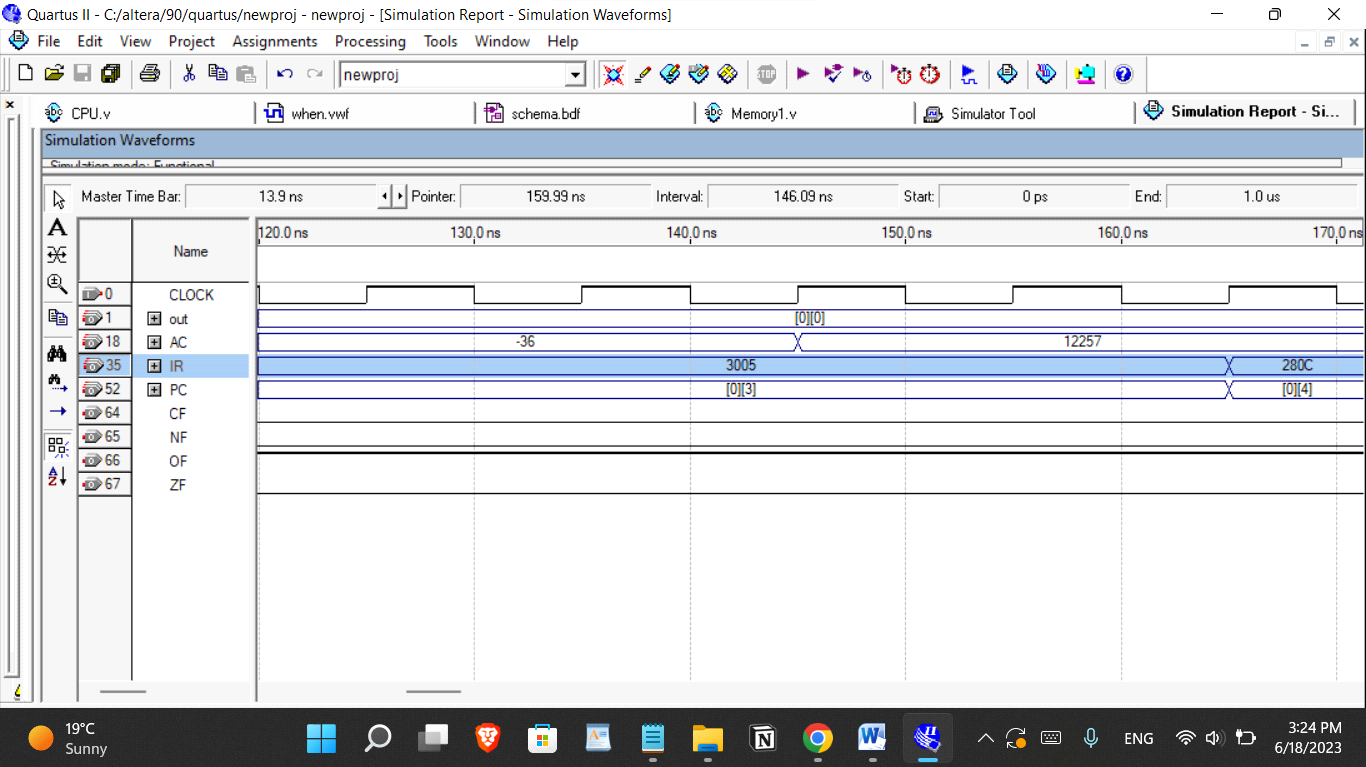
**1)** Initialize the memory with the following four instructions at memory address 0-3, and data at memory address 10-12, as shown in the following table.

**A)**Interpret each instruction into assembly instruction and add it to its corresponding instruction in the table. Also, interpret the integer’s data into decimal and add them into the table.

|  |  |  |
| --- | --- | --- |
| **Memory address** | **Content** | **Content in assembly** |
| **0** | **0x180A** | **LOAD [10]** |
| **1** | **0x580B** | **MUL [11]** |
| **2** | **0x3005** | **ADD 5** |
| **3** | **0x280C** | **STORE[12]** |
|  |  |  |
|  |  |  |
|  |  |  |
| **10** | **0x0009** | **9** |
| **11** | **0xFFFC** | **-4** |
| **12** | **0x0000** | **0** |

b) Simulate the four instructions at address 0 by initializing PC =0. Provide a snapshot of your resulted waveform. Verify that it works correctly and the also verify that the result stored at address 12 is correct.

Attach of simulation waveform:



**note:**in the semulations it executes all instructions correctly when the data is from a memory but when its an immediate there is a problem

**2)** Assume A,B,C,D,E and Y are memory cells with addresses 20,21,22,23,24, and 25, respectively.

Given , 𝑌 = 𝐴+𝐵∗𝐶−5/ 𝐷+𝐸+1 ,

a) Write assembly code for implementing the above arithmetic expression?

LOAD [23]

ADD [24]

ADD 1

STORE [25]

LOAD [21]

MUL [22]

SUB 5

ADD [20]

DIV [25]

STORE [25]

b) Convert the above assembly instructions into machine code and store them in the memory starting at address 0.

|  |  |
| --- | --- |
| **ADDRESS** | **CONTENT** |
| **0** | **0001 1 000 0001 0111** |
| **1** | **0011 1 000 0001 1000** |
| **2** | **0011 0 000 0001 0001** |
| **3** | **0010 1 000 0001 1001** |
| **4** | **0001 1 000 0001 0101** |
| **5** | **0101 1 000 0001 0110** |
| **6** | **0100 0 000 0000 0101** |
| **7** | **0011 1 000 0001 0100** |
| **8** | **0110 1 000 0001 1001** |
| **9** | **0010 1 000 0001 1001** |
| **10** |  |

c) Set PC=0 and simulate the above program. Verify that it works correctly and the result stored at memory variable Y is correct. Attach simulation waveform and the Verilog source file. Assume A, B, C, D and E have the values 2, 3, 5, 8, and -5, respectively.

it should equal 3

