Department of Electrical and Computer Engineering

First Semester,2023

Digital Systems - ENCS234

Verilog Project

Student Name : Asmaa abed AL-Rahman Fares

Student Number : 1210084

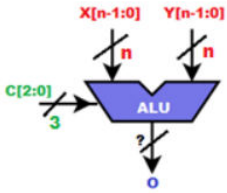
section 7

instructor : Dr.Ali

Problem: Modeling a Multifunction ALU

Design and implement a multifunction arithmetic and logic unit (ALU) based on the following specifications:

1. **X** and **Y** are the inputs of the unit and they are n-bit signed numbers represented in 2's complement.
2. **C** is a 3-bit unsigned number and used to select the operation of the unit (i.e. arithmetic or logical operation).
3. **O** is the signed ALU output and represented in 2's complement. Note that, you are required to define the minimum number of bits needed for **O** that will make the overflow never occurs in this design.
4. ALU symbol and the supported functions are represented as follow:

ALU Function Code (C)	ALU Output (O)	ALU Symbol
000	(**X**+**Y**)/2	
001	2*(**X**+**Y**)	
010	(**X**/2)+**Y**	
011	**X**-(**Y**/2)	
100	**X** NAND **Y**	
101	NOT(**X**)	
110	**X** NOR **Y**	
111	**X** XOR **Y**	

QUESTIONS AND ANSWERS:

a) Specify the size of the output (O) in bits so the overflow can never occur.

The size of the output (O) in bits so the overflow can never occur is n+2 bits, where n is the size of the inputs X and Y.

i concluded the max size from calculating the second operation which required me to add mor bits i explaind why in part b .

b)Show the ALU implementation using medium-scale integration (MSI) components and minimum number of gates (i.e. in blocks with their sizes). Note that, you mightuse some kind of extension (sign-

or zero-extension).

in the screenshots below im declaring that i connected the given order of blocks using a 8*1 mux that execute the requierd arithmetic and logical operations in the given table as follows

(x+y)/2 is xpy2 block

2*(x+y) is twoxy block

(x/2)+y is x2y block

x-(y/2) is xy2 block

xnandy block

not x block

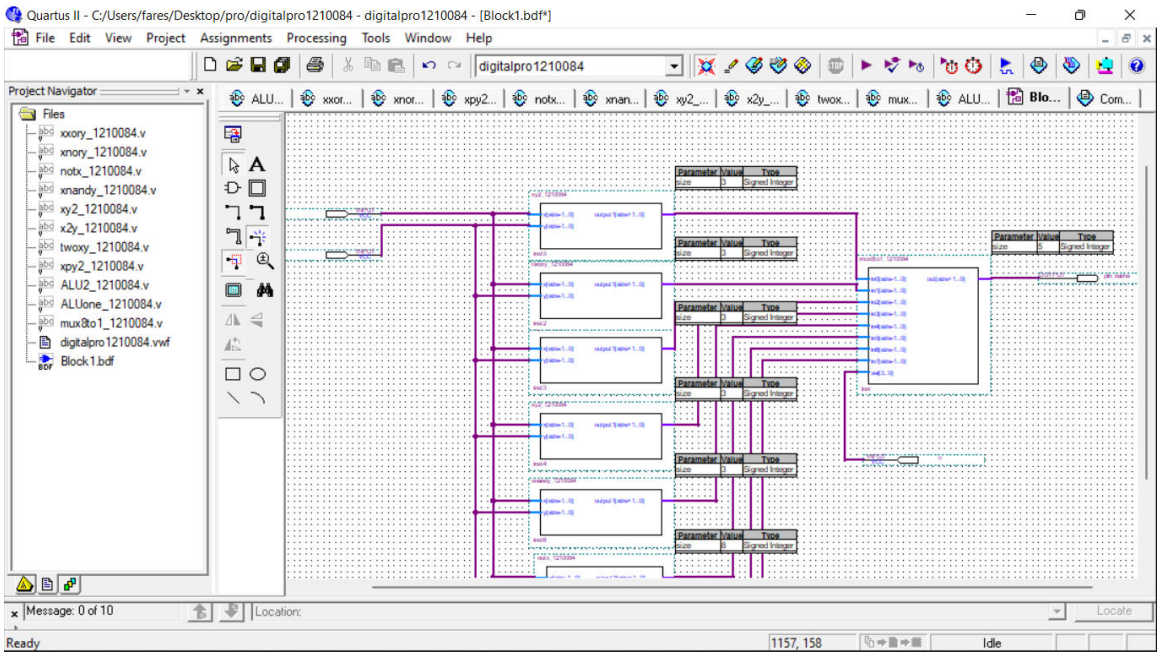
xnory block

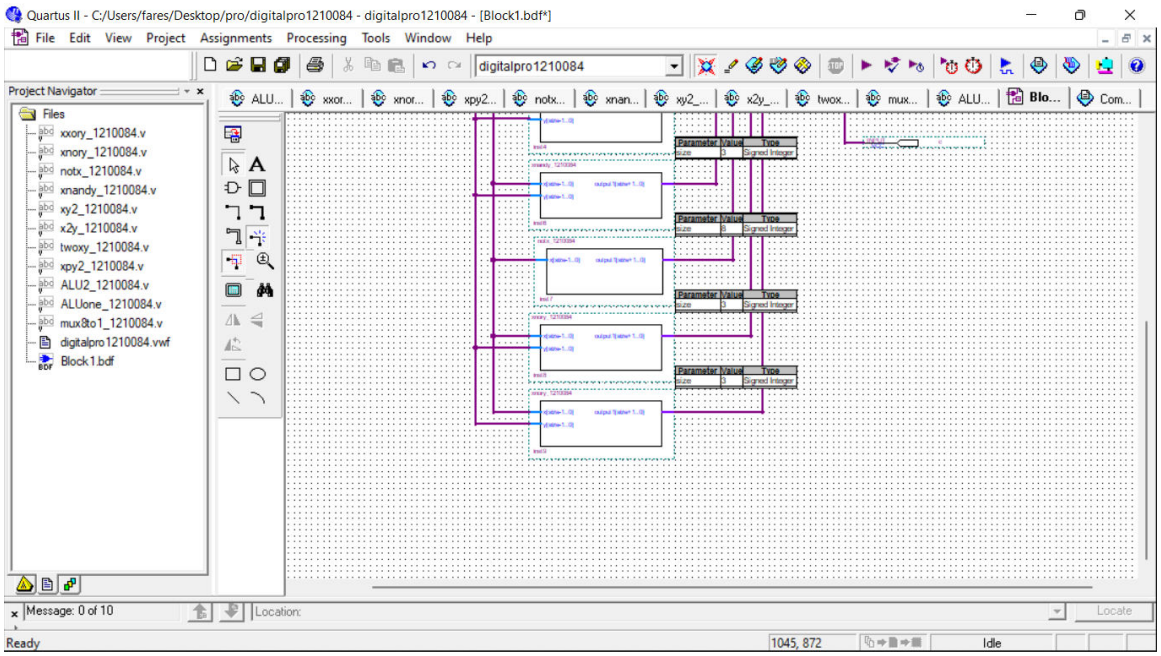
xxory block

x and y in these blocks have this range n-1to 0 and the output for each is n+1to0 because more bits for the output wont affect the result

i concluded the maximum size after calculating the second operation that requiers more 2 bits than the input after shifting and adding .

note : zoom in to see the components more clearly





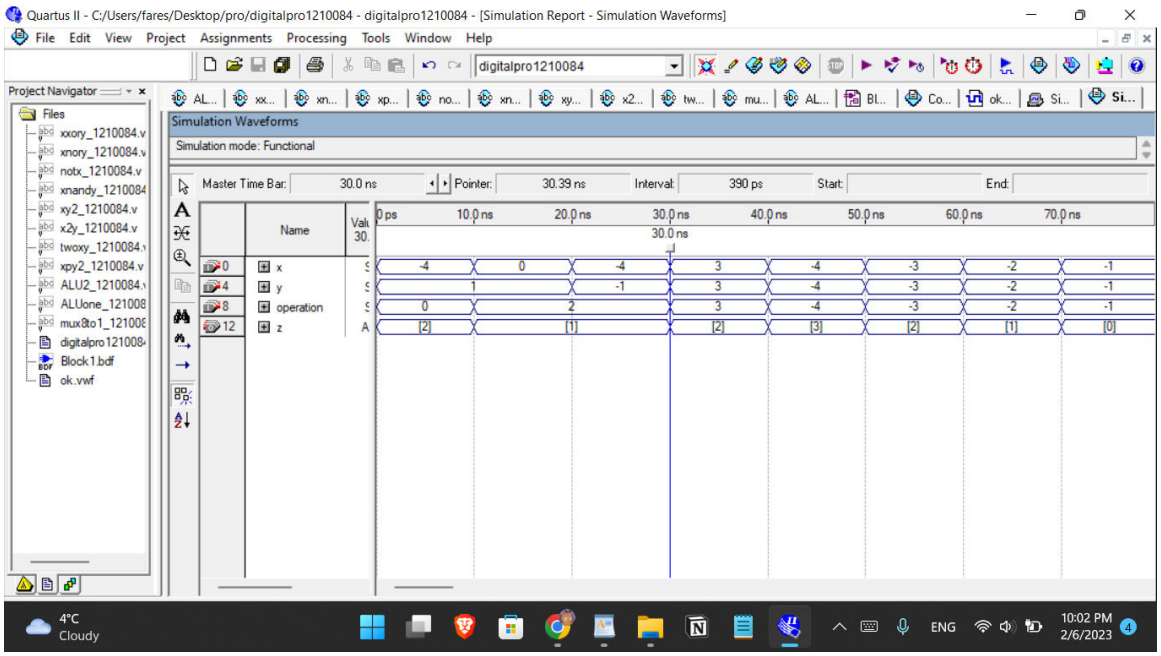
c) Write behavioral Verilog modules for your elements you defined in Part (b). Be noted that the size of every element you define should be parameterized, so that you can vary the design during the testing phase.

attached in the file

d) Write a structural Verilog model for your ALU designed in Part (b) using the elements you defined in Part (c).

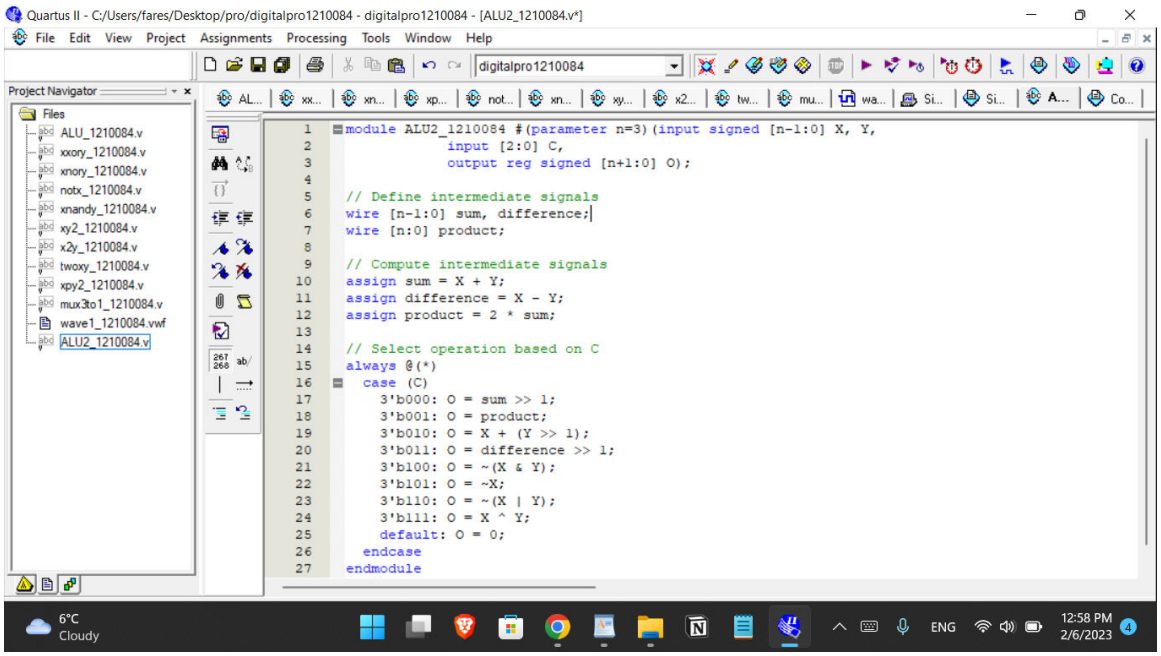
attached in the file

e) Generate the waveforms of the ALU defined in Part (d), assumes that X and Y are 4-bits and their values based on my student ID .



ps:while i was entering the values to the wave the first value in the wave for x keeps changing to negative value in both of my waveforms

f) Write a single behavioral Verilog module that models the designed ALU.



g) Generate the waveforms of the behavioral ALU defined in Part (f), assumes that

X and Y are 4-bits and their values based on your student ID should be set as follows:

The general representation of the student ID is 1C2Y2X2C1Y1X1.