Digital Clock

Designed by:

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Components Used:

- AND Gates
- OR Gates
- XOR Gates
- NOT Gates
- 0-9 Counters
- 0-5 Counters
- 0-2 Counter
- T Flip Flop
- J-K Flip Flop
- Clock Pulse (Hertz)

Overview:

This documentation gives a brief overview of the 24 hour digital clock designed using the concepts of Flip Flops, Counters and some Logic Gates. The digital Clock displays Seconds, Minutes and Hours. The clock has some push buttons to reset the clock. Some more push buttons have been used for setting up the clock manually. A clock pulse has been used which is fed into the counters used in the circuit. The clock resets to initial condition after twenty four hours. The circuit of the clock is simulated using the Logicly software (https://logic.ly/download/).

Basic Logic of the Clock:

The working of clock is such that six display blocks have been used for displaying Hours, Minutes and Seconds in the format HH/MM/SS. Now in the SS (seconds') block S0 counts from 0 to 9. On 9 S1 becomes 1 and S0 starts counting again. S1 counts till 5 only, because when SS becomes 59 so the SS block is set back to 00. Each time when SS completes 60 seconds so the M0 in MM(minutes) block increases by 1. The working of

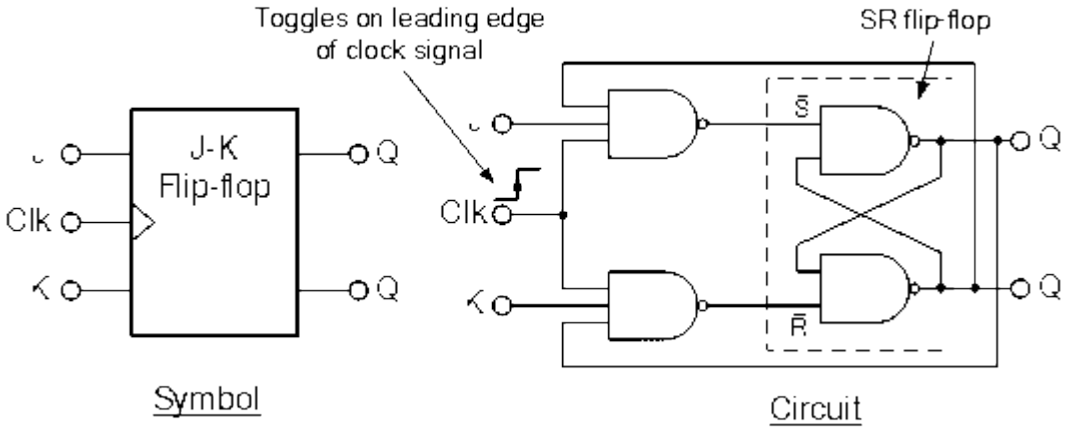
the MM block is same as that of the SS block so once we reach 59 in the MM block it increments the HH(hour) block by 1 and this whole process continues until we get 23 in the HH block. After that the clock resets to 00/00/00(initial state).

Now for the implementation of this Logic we have used a decade counter for S0, M0 and H0 because they count from zero to nine whereas for S1 and M1 a 0-5 counter has been used. For H1 a 0-2 counter has been used because H1 counts till 2 only (HH=24).

Mechanisms:

J-K Flip Flop:

J-K Flip Flops has two inputs J and K and it is connected to a clock pulse (positive triggered). If J and K are different then output has the same value as that of J but if J and K are same then it represents a toggle state.

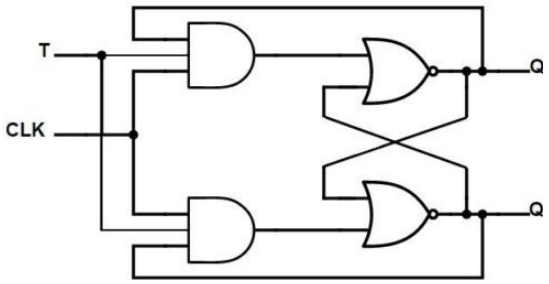


Truth Table:

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\bar{Q}_0$ (toggles)

T Flip Flop:

A T Flip Flop or a Toggle Flip Flop changes (toggles) its output whenever the input T is high. If T is low so the flip flop remains in its previous state and there is no change on the output Q.

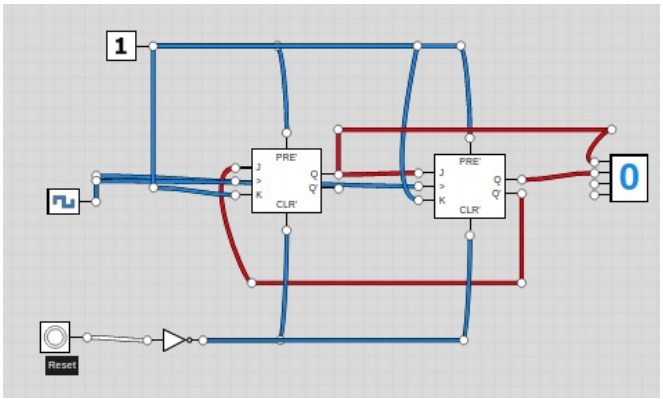


Truth Table:

T	Present state	CLK	Next State
0	0	↑	0
0	1	↑	1
1	0	↑	1(toggles)
1	1	↑	0(toggles)

0-2 Counter using J-K Flip Flop:

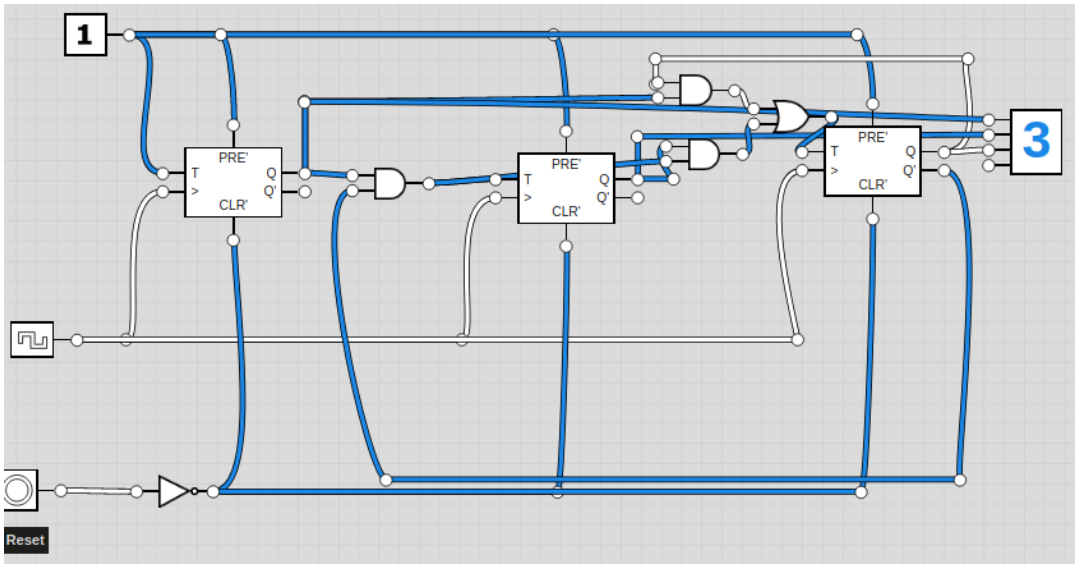
Two J-K Flip Flops have been used to implement a sequential circuit for a 0 to 2 counter. The purpose of this counter in the Digital Clock is to count from zero to two for the H1 of Hour Block. Initially, it has a zero stored in it. When it gets a 9 from the H0 so it increments by one. Once it reaches to two, it then resets to 00 on the next count.



0-5 Counter Using T Flip-Flop:

Combination of three T flip flops have been used to design a 0-5 counter. Two 0-5 counters have been used in the whole circuit. These counters count from zero to five. One of it is connected to the M1 of MM block and the other is connected to the S1 of SS block.

The purpose of this counter is to display digits from zero to five in the display blocks of Minutes and Seconds. These counters are further connected to another T flip flop which stores the value. Initially it has zero stored in it. When it gets a 9 from the decade counter so it increments by 1 and this process continues until it reaches 5. Once it reaches five and the decade counter reaches nine so we get 59 in SS block and as a result the M1 of MM block increments by one. Both, 0-5 counters used, have the same working mechanism.



0-9 Counter Using T Flip Flops:

A combination of four T Flip Flops have been used to implement a decade counter. Since it is a 0-9 counter so we need 4 bits and hence four flip flops are used. The purpose of this counter is same as that of a 0-5 counter but it counts from zero to nine. Once the S0 of SS block reaches to 9 so the decade counter sends signals to the 0-5 counter and increments it by 1. Three 0-9 counters have been used in the whole circuit. One for the S0 of SS block, another one for the M0 of MM block and the last one is used for the H0 of HH block. A clock pulse is given to the first decade counter and the rest are

triggered by the previous one. An XOR Gate is connected to the output of each 0-9 counter which helps in setting up the time manualy.