# Assignment 5

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## 1 Task 1

For task 1 we were required to implement all five parts of datapath for addi instruction.

The five datapaths are:-

- Instruction Fetch (IF)
- Instruction Decode (ID)
- Execute (EX)
- Memory (MEM)
- Write Back (WB)

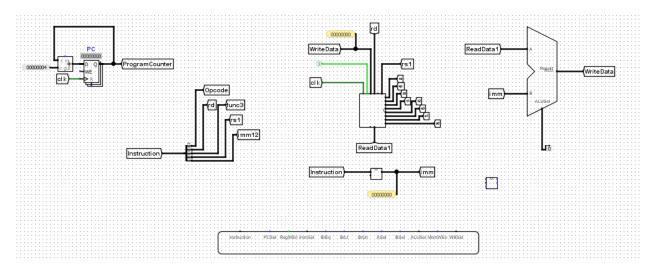


Figure 1: Datapath for addi instruction

#### **Additional Points:**

- Since we are not using control signals, we have hardwired some of the control signals.
- Splitter has been used to split the different fields for instruction.
- Various parts of instruction has been given input to register file and the ALU.

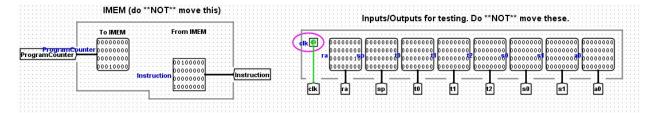


Figure 2: Result for addi instruction imm = 512 rd = 1(ra)

## 2 Task 2

## 2.1 Task 2.1

In Task 2, we will have to add ALUsel tunnnel and RegWEn tunnel instead of hardcoded control signal.

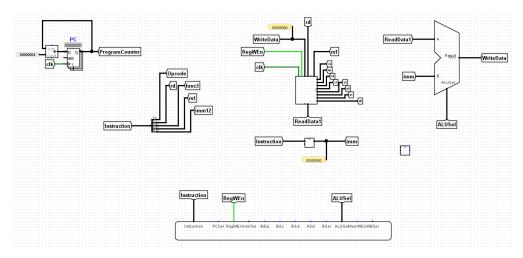


Figure 3: CPU for task 2

### 2.2 Task 2.2

In this subproblem, we need to we need to implement control signal for the immediate instruction. For this subproblem we make an observation that the func3 field is the same as the ALUsel in alu.circ, hence we can directly map the func3 to ALUsel and use it in our main file(cpu.circ).

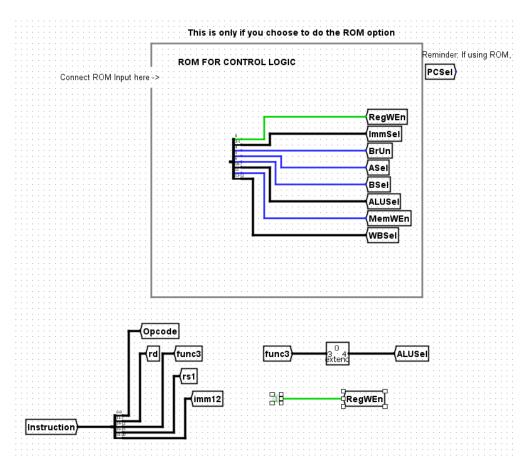


Figure 4: Control Logic for Task 2.2

## 3 Task 3

In Task 3, we are required to implement the R-type instruction.

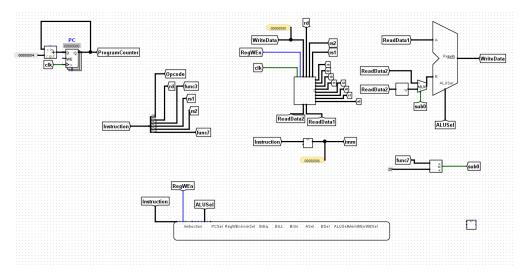


Figure 5: CPU for R-type instructions

Control Logic for R-type instructions.

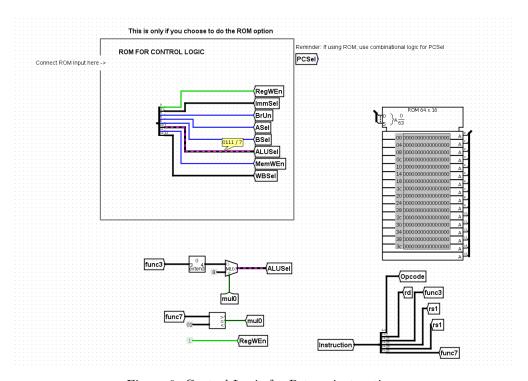


Figure 6: Control Logic for R-type instructions