Computer Architecture HW2

B07303024 李品樺

```
Inferred memory devices in process
        in routine ALU line 198 in file
                '/home/raid7_2/userb07/b7303024/111-1_CA_HW2/HW2.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     alu_in_reg      | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
|       rdy_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|      state_reg      | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N  |
|     counter_reg     | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|      shreg_reg      | Flip-flop |  64   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb07/b7303024/111-1_CA_HW2/ALU.db:ALU'
Loaded 1 design.
Current design is 'ALU'.
ALU
```