# Results of the project implementation for the Reconfigurable Systems course

#### Amin Daemdoost

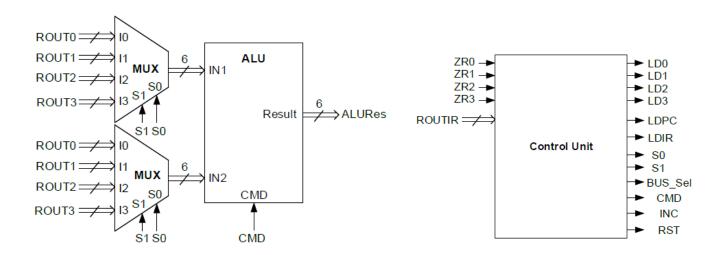
Course Instructor: Mehdi Aminian

Consider the following components: the Arithmetic Logic Unit (ALU) and the Control Unit. Write a test bench for their attached code using the VHDL language via Vivado software, then determine the consumed LUTs, power, delay, and utilization.

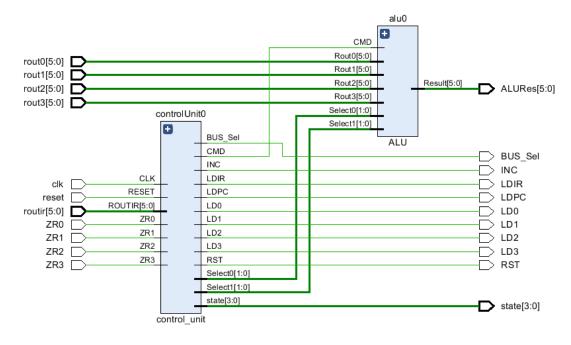
Note: For the test bench inputs ROUTIR, ROUT3, ROUT2, ROUT1, ROUT0, write the last two digits of your student number in 8-bit binary format, and take the least significant 6 bits as the first input. Then, assign subsequent inputs as 2 times, 4 times, 6 times, and so on, based on the initial value.

**Example:** If the last two digits of your student number are **02**, the least significant **6-bit binary** representation would be **000001**. Thus, the sequence of multiple inputs would be:

000010, 000100, 001000, 001100, ...



#### 1. Final Schematic in vivado



# ۲. خروجی simulation



# 3. Number of each cell type used

N main

| Primitive type<br>FLOP_LATCH | Count<br>9 |
|------------------------------|------------|
| LUT                          | 83         |
| CARRY                        | 4          |
| Ю                            | 55         |
| CLK                          | 1          |

## 4. Power consumption

#### Settings Summary (11.523 W, Margir

Power Supply

V Utilization Details

Hierarchical (10.483 W)

✓ Signals (0.733 W)

ignale (on oo ii)

Data (0.733 W)

Set/Reset (0 W)

Logic (0.361 W)

I/O (9.389 W)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 11.523 W (Junction temp exceeded!)

Design Power Budget: Not Specified

Power Budget Margin: N/A

Junction Temperature: 125.0°C

Thermal Margin: -72.9°C (-5.6 W)

Effective  $\vartheta$ JA: 11.5°C/W Power supplied to off-chip devices: 0 W

Confidence level: Low

Launch Power Constraint Advisor to find and fix

invalid switching activity

|      |                | 10.483 W    | (91% | o) —  |
|------|----------------|-------------|------|-------|
| 040/ | s              | ignals: 0.7 | 33 W | (7%)  |
| 91%  | 90% L          | ogic: 0.3   | 61 W | (3%)  |
|      |                | O: 9.3      | 89 W | (90%) |
| 9%   | Device Static: | 1.039 W     | (9%  | n)    |

| Summary (11.523 W, Margin: N/A |
|--------------------------------|
| Power Supply                   |

Utilization Details

Settings

#### Hierarchical (10.483 W)

∨ Signals (0.733 W)

Data (0.733 W)

Set/Reset (0 W)

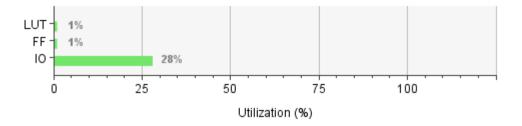
Logic (0.361 W)

I/O (9.389 W)

| Utilization               | Name                          | Signals (W) | Data (W) | Logic (W) | I/O (W) |
|---------------------------|-------------------------------|-------------|----------|-----------|---------|
| V 10.483 W (91% of total) | N main                        |             |          |           |         |
| 9.6 W (83% of total)      | Leaf Cells (56)               |             |          |           |         |
| > 0.831 W (7% of total)   | ■ controlUnit0 (control_unit) | 0.491       | 0.491    | 0.339     | <0.001  |
| > 0.053 W (1% of total)   | I alu0 (ALU)                  | 0.036       | 0.036    | 0.016     | <0.001  |

### 5. Utilization

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT      | 72          | 53200     | 0.14          |
| FF       | 9           | 106400    | 0.01          |
| IO       | 55          | 200       | 27.50         |



# 6. Delay



| General Information    | Timing Check                     | Count ~ | 1 Worst Severity |
|------------------------|----------------------------------|---------|------------------|
| Timer Settings         | no_output_delay                  | 19      | 9 High           |
| Design Timing Summary  | no_input_delay                   | 11      | l U High         |
| Clock Summary (1)      | no_clock                         | (       | )                |
| > 庙 Check Timing (30)  | constant_clock                   | (       | )                |
| > lntra-Clock Paths    | pulse_width_clock                | (       | )                |
| Inter-Clock Paths      | unconstrained_internal_endpoints | (       | )                |
| Other Path Groups      | multiple_clock                   | (       | )                |
| User Ignored Paths     | generated_clocks                 | (       | )                |
| >  Unconstrained Paths | loops                            | (       | )                |
| >  Datasheet           | partial_input_delay              | (       | )                |
|                        | partial_output_delay             | (       | )                |
|                        | latch_loops                      | (       | )                |
|                        |                                  |         |                  |

| General Information     | Name       | Slack ^1 | Levels | Routes | High Fanout | From      | То        | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock     |
|-------------------------|------------|----------|--------|--------|-------------|-----------|-----------|-------------|-------------|-----------|-------------|------------------|
| Timer Settings          | 3 Path 19  | ∞        | 7      | 5      | 21          | routir[3] | ALURes[2] | 15.871      | 5.007       | 10.864    | 00          | input port clock |
| Design Timing Summa     | → Path 20  | 00       | 7      | 5      | 21          | routir[2] | ALURes[4] | 15.684      | 4.866       | 10.819    | 00          | input port clock |
| Clock Summary (1)       | ¹→ Path 21 | 00       | 8      | 6      | 21          | routir[3] | ALURes[5] | 15.575      | 5.325       | 10.250    | 00          | input port clock |
| > 🙃 Check Timing (30)   | → Path 22  | 00       | 7      | 5      | 21          | routir[3] | ALURes[1] | 15.546      | 4.876       | 10.669    | 00          | input port clock |
| > intra-Clock Paths     | → Path 23  | 00       | 7      | 5      | 21          | routir[3] | ALURes[0] | 15.015      | 4.670       | 10.345    | 00          | input port clock |
| Inter-Clock Paths       | → Path 24  | 00       | 7      | 5      | 21          | routir[3] | ALURes[3] | 14.530      | 5.058       | 9.472     | 00          | input port clock |
| Other Path Groups       | → Path 25  | 00       | 3      | 2      | 21          | routir[3] | LD2       | 9.199       | 4.100       | 5.099     | 00          | input port clock |
| User Ignored Paths      | → Path 26  | 00       | 3      | 2      | 21          | routir[3] | LD1       | 8.964       | 3.868       | 5.096     | 00          | input port clock |
| ∨ □ Unconstrained Paths | → Path 27  | 00       | 3      | 2      | 21          | routir[3] | LD3       | 8.851       | 4.119       | 4.732     | 00          | input port clock |
| ✓ NONE to NONE          | → Path 28  | 00       | 3      | 2      | 21          | routir[3] | LD0       | 8.398       | 3.860       | 4.538     | 00          | input port clock |
| Setup (10)<br>Hold (10) |            |          |        |        |             |           |           |             |             |           |             |                  |

| General Information    | Name        | Slack | Levels | Routes | High Fanout | From      | То                       | Total ∨ 1 | Logic Delay | Net Delay | Requirement | Source   |
|------------------------|-------------|-------|--------|--------|-------------|-----------|--------------------------|-----------|-------------|-----------|-------------|----------|
| Timer Settings         | lup Path 39 | ∞     | 3      | 2      | 21          | routir[3] | controlUnit0p_s_reg[3]/D | 4.944     | 1.405       | 3.540     | ∞           | input po |
| Design Timing Sum      | lup Path 40 | ∞     | 3      | 2      | 21          | routir[2] | controlUnit0p_s_reg[6]/D | 4.575     | 1.350       | 3.225     | 00          | input po |
| Clock Summary (1)      | ↓ Path 41   | ∞     | 3      | 2      | 21          | routir[2] | controlUnit0p_s_reg[7]/D | 4.567     | 1.342       | 3.225     | 00          | input po |
| > 🙃 Check Timing (30)  | ↓ Path 42   | 00    | 3      | 2      | 21          | routir[3] | controlUnit0p_s_reg[0]/D | 4.446     | 1.405       | 3.042     | ∞           | input po |
| > Intra-Clock Paths    | ┡ Path 43   | 00    | 2      | 1      | 6           | routir[4] | controlUnit0p_s_reg[8]/D | 4.060     | 1.307       | 2.753     | 00          | input po |
| Inter-Clock Paths      | ┡ Path 44   | 00    | 2      | 1      | 6           | routir[4] | controlUnit0p_s_reg[2]/D | 4.038     | 1.285       | 2.753     | 00          | input po |
| Other Path Groups      | ┡ Path 45   | 00    | 1      | 1      | 9           | reset     | controlUnit0s_reg[1]/CLR | 3.515     | 0.984       | 2.531     | 00          | input po |
| User Ignored Paths     | ┡ Path 46   | 00    | 1      | 1      | 9           | reset     | controlUnit0s_reg[4]/PRE | 3.515     | 0.984       | 2.531     | 00          | input po |
| ∨ □ Unconstrained Path | ▶ Path 47   | 00    | 1      | 1      | 9           | reset     | controlUnit0s_reg[5]/CLR | 3.515     | 0.984       | 2.531     | 00          | input po |
| ∨ □ NONE to NONE       | ▶ Path 48   | 00    | 1      | 1      | 9           | reset     | controlUnit0s_reg[3]/CLR | 3.365     | 0.984       | 2.382     | 00          | input po |
| Setup (10)             |             |       |        |        |             |           |                          |           |             |           |             |          |
| Hold (10)              |             |       |        |        |             |           |                          |           |             |           |             |          |
| ✓ □ NONE to clk        |             |       |        |        |             |           |                          |           |             |           |             |          |

| General Information    | Name      | Slack ^1 | Levels | Routes | High Fanout | From                  | То        | Total Delay | Logic Delay | Net Delay | Requirement | Sou |
|------------------------|-----------|----------|--------|--------|-------------|-----------------------|-----------|-------------|-------------|-----------|-------------|-----|
| Timer Settings         | 3 Path 59 | 00       | 6      | 5      | 42          | controlUnits_reg[8]/C | ALURes[4] | 14.389      | 4.417       | 9.972     | 00          | clk |
| Design Timing Sum      | 3 Path 60 | ∞        | 6      | 5      | 42          | controlUnits_reg[8]/C | ALURes[2] | 14.259      | 4.762       | 9.497     | 00          | clk |
| Clock Summary (1)      | 3 Path 61 | ∞        | 6      | 5      | 42          | controlUnits_reg[8]/C | ALURes[5] | 14.211      | 4.611       | 9.600     | 00          | clk |
| > 庙 Check Timing (30)  | 3 Path 62 | 00       | 6      | 5      | 42          | controlUnits_reg[8]/C | ALURes[1] | 13.831      | 4.369       | 9.462     | 00          | clk |
| > 🔚 Intra-Clock Paths  | 3 Path 63 | ∞        | 6      | 5      | 42          | controlUnits_reg[8]/C | ALURes[0] | 13.301      | 4.163       | 9.138     | 00          | clk |
| Inter-Clock Paths      | 3 Path 64 | 00       | 6      | 5      | 42          | controlUnits_reg[8]/C | ALURes[3] | 12.920      | 4.814       | 8.105     | 00          | clk |
| Other Path Groups      | 3 Path 65 | 00       | 3      | 3      | 6           | controlUnits_reg[7]/C | state[0]  | 8.182       | 3.941       | 4.241     | 00          | clk |
| User Ignored Paths     | 3 Path 66 | 00       | 3      | 3      | 6           | controlUnits_reg[7]/C | state[2]  | 7.677       | 3.495       | 4.182     | 00          | clk |
| ✓ 🗀 Unconstrained Path | 3 Path 67 | 00       | 3      | 3      | 6           | controlUnits_reg[7]/C | state[3]  | 7.308       | 3.485       | 3.822     | 00          | clk |
| V ■ NONE to NONE       | → Path 68 | 00       | 3      | 3      | 11          | controlUnits_reg[4]/C | state[1]  | 6.779       | 3.302       | 3.476     | 00          | clk |
| Setup (10)             |           |          |        |        |             |                       |           |             |             |           |             |     |
| Hold (10)              |           |          |        |        |             |                       |           |             |             |           |             |     |

Hold (10)

Value clk to NONE

Setup (10)

Hold (10)

∨ NONE to clk
Setup (10)

Setup (10) Hold (10)