Results of the project implementation for the Reconfigurable Systems course

Amin Daemdoost

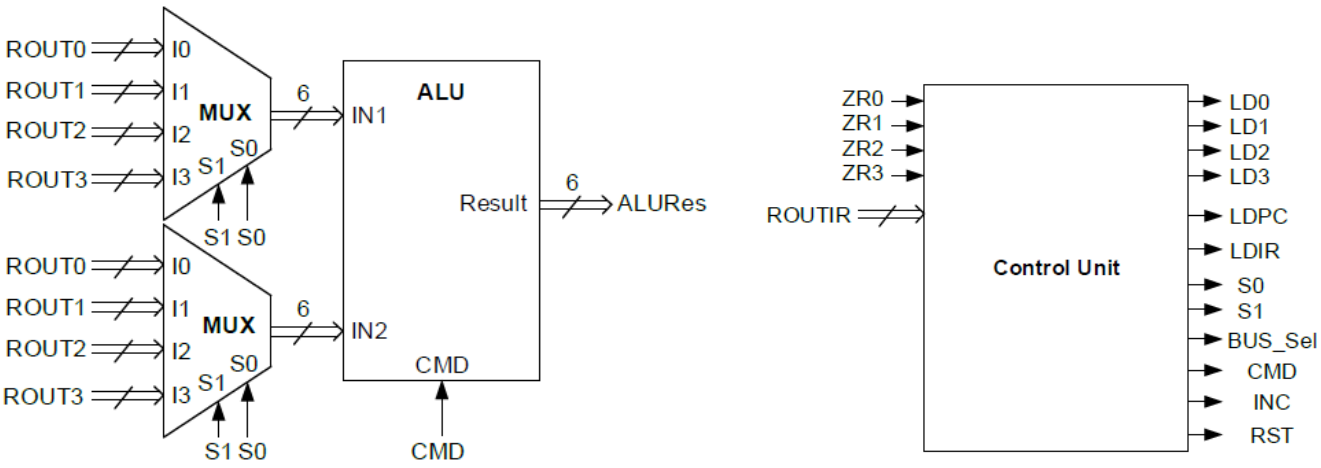
Course Instructor: Mehdi Aminian

Consider the following components: the Arithmetic Logic Unit (ALU) and the Control Unit. Write a test bench for their attached code using the VHDL language via Vivado software, then determine the consumed LUTs, power, delay, and utilization.

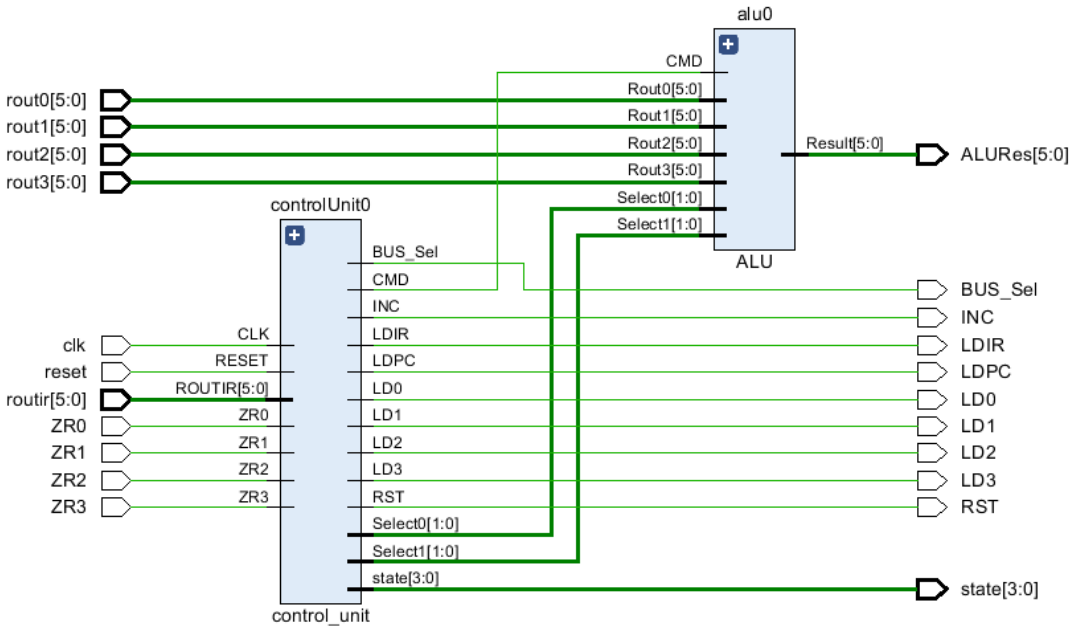
Note: For the test bench inputs **ROUTIR, ROUT3, ROUT2, ROUT1, ROUT0**, write the last two digits of your student number in **8-bit binary format**, and take the least significant **6 bits** as the first input. Then, assign subsequent inputs as **2 times, 4 times, 6 times**, and so on, based on the initial value.

Example: If the last two digits of your student number are **02**, the least significant **6-bit binary** representation would be **000001**. Thus, the sequence of multiple inputs would be:

000010, 000100, 001000, 001100, ...



1. Final Schematic in vivado



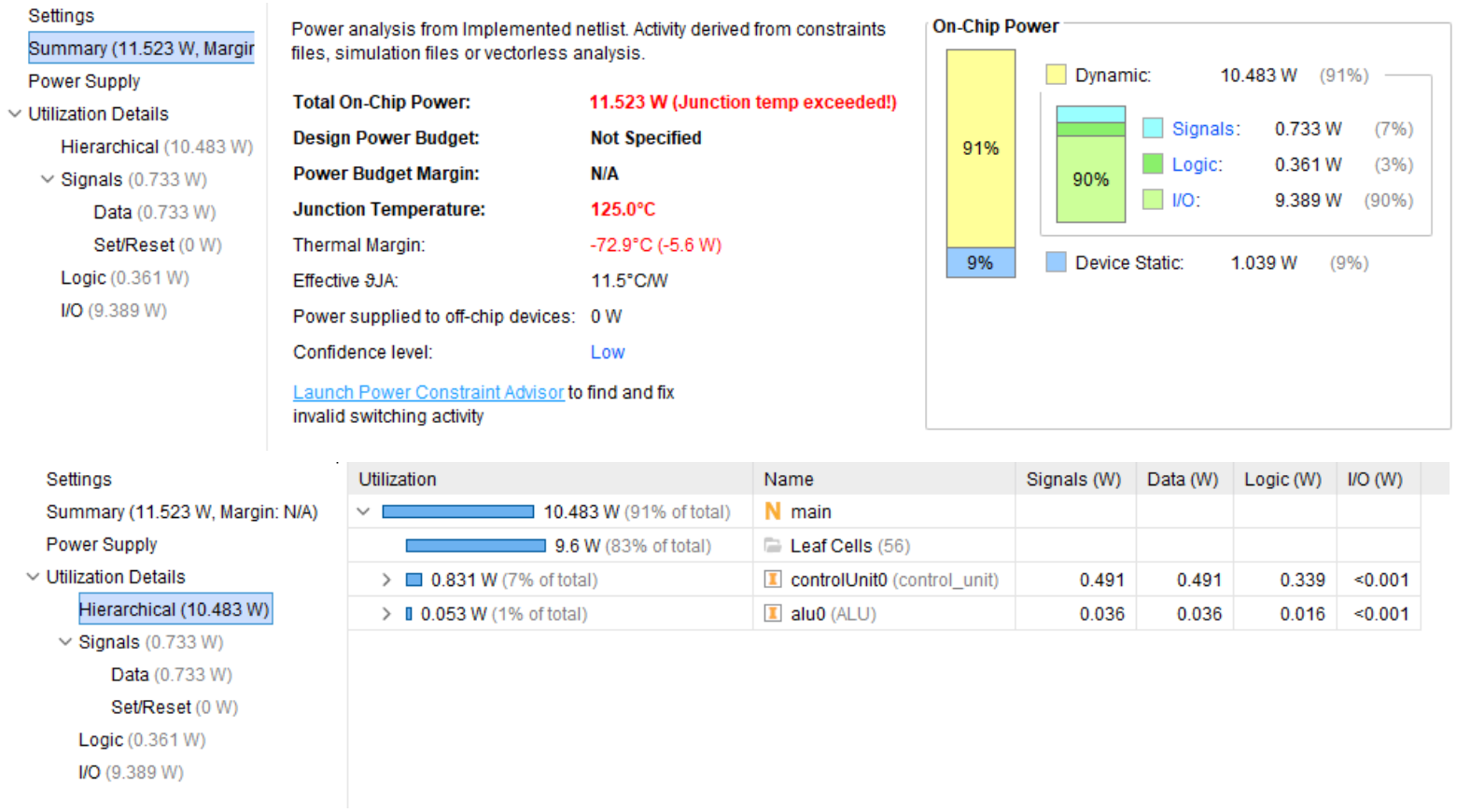
۲. خروجی simulation

3. Number of each cell type used

N main

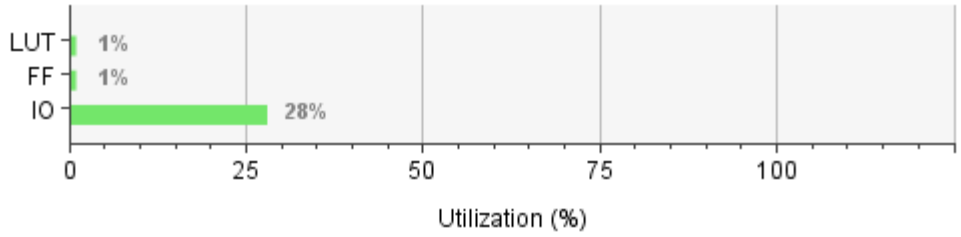
Primitive type	Count
FLOP_LATCH	9
LUT	83
CARRY	4
IO	55
CLK	1

4. Power consumption

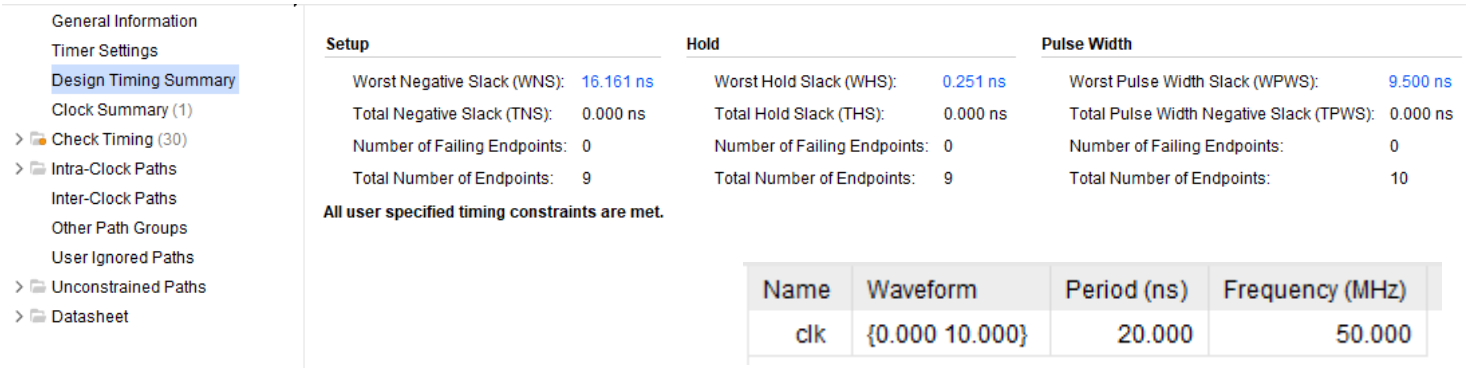


5. Utilization

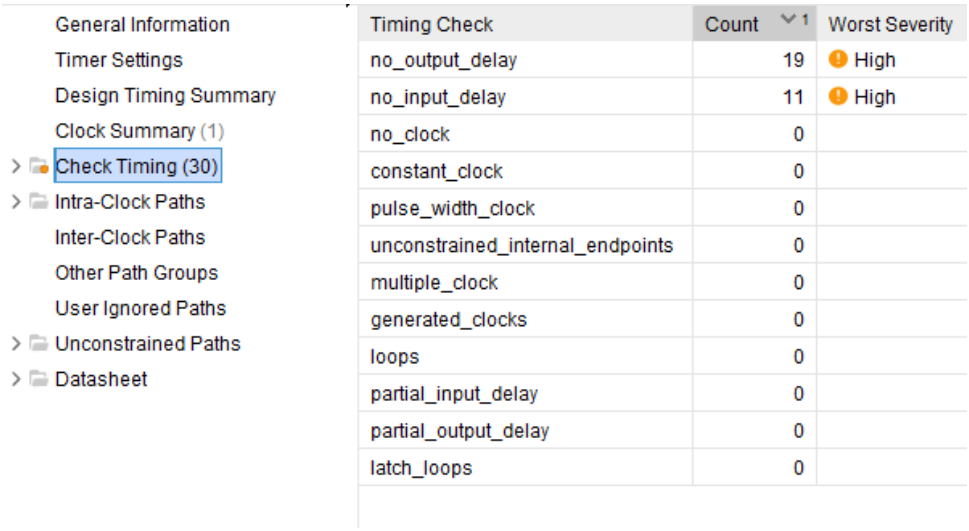
Resource	Utilization	Available	Utilization %
LUT	72	53200	0.14
FF	9	106400	0.01
IO	55	200	27.50



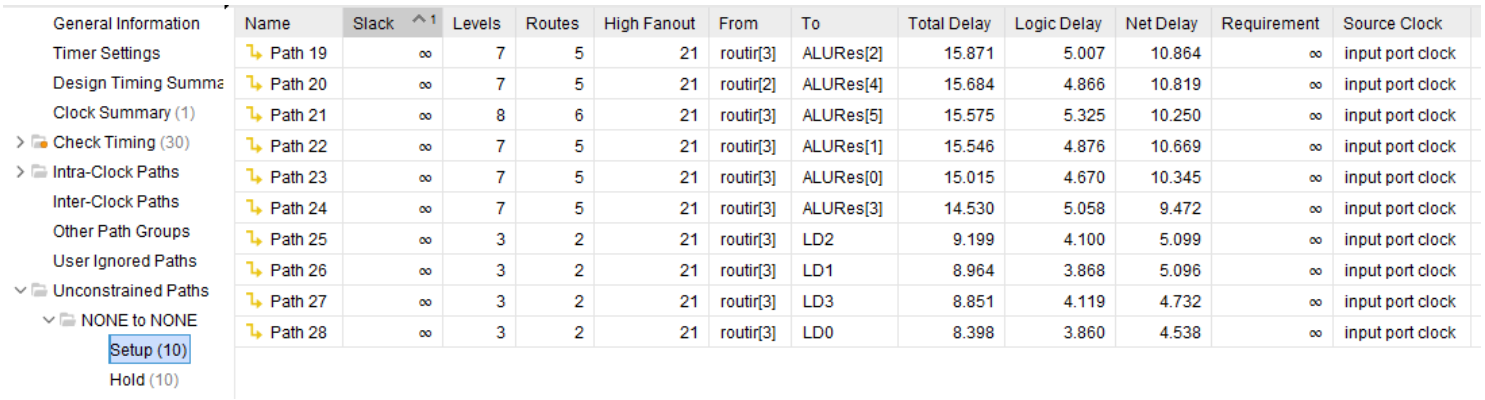
6. Delay



Name	Waveform	Period (ns)	Frequency (MHz)
clk	{0.000 10.000}	20.000	50.000

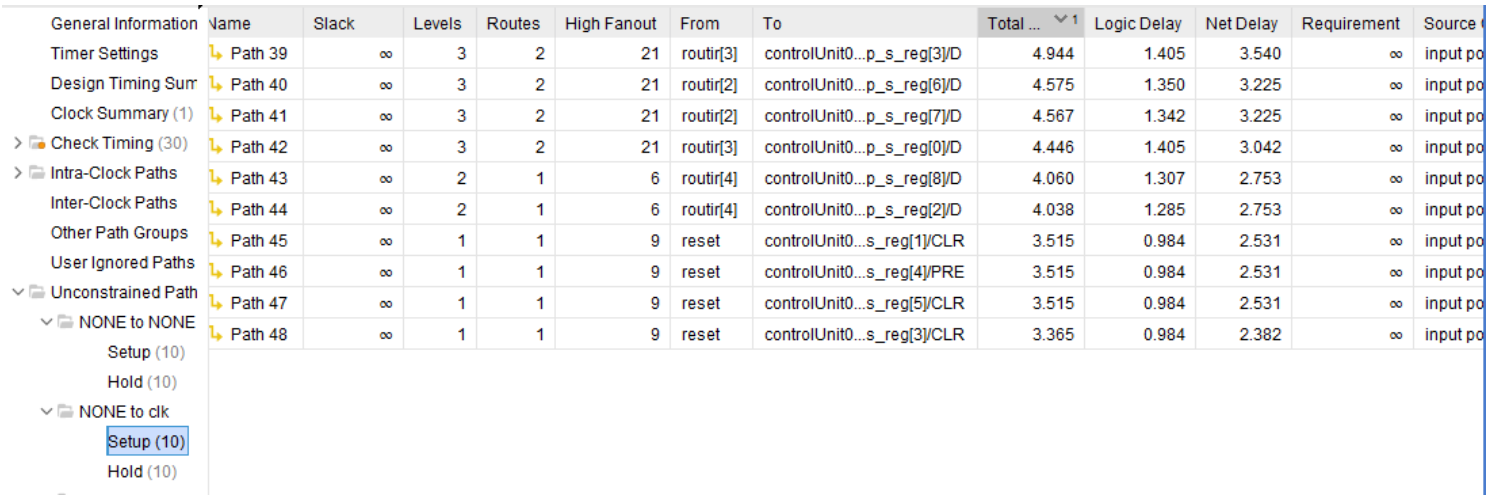


Timing Check	Count	Worst Severity
no_output_delay	19	High
no_input_delay	11	High
no_clock	0	
constant_clock	0	
pulse_width_clock	0	
unconstrained_internal_endpoints	0	
multiple_clock	0	
generated_clocks	0	
loops	0	
partial_input_delay	0	
partial_output_delay	0	
latch_loops	0	



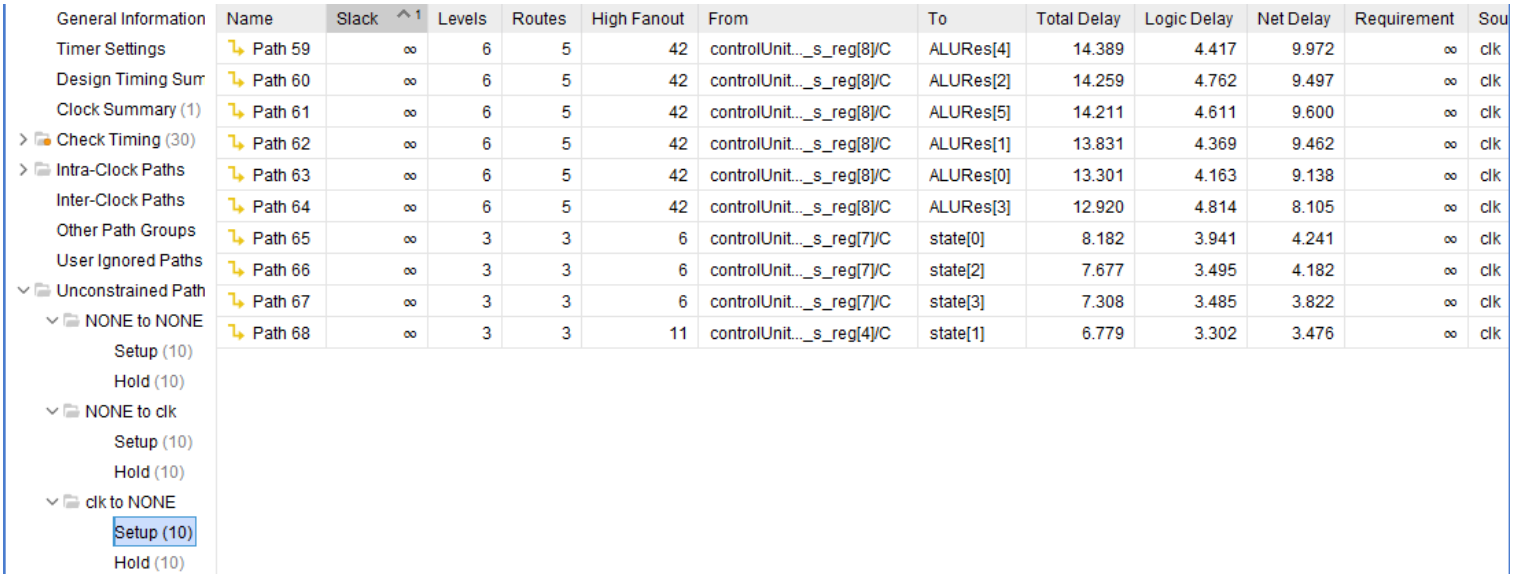
- General Information
- Timer Settings
- Design Timing Summa
- Clock Summary (1)
- Check Timing (30)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths
  - NONE to NONE
    - Setup (10)
    - Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 19	∞	7	5	21	routir[3]	ALURes[2]	15.871	5.007	10.864	∞	input port clock
Path 20	∞	7	5	21	routir[2]	ALURes[4]	15.684	4.866	10.819	∞	input port clock
Path 21	∞	8	6	21	routir[3]	ALURes[5]	15.575	5.325	10.250	∞	input port clock
Path 22	∞	7	5	21	routir[3]	ALURes[1]	15.546	4.876	10.669	∞	input port clock
Path 23	∞	7	5	21	routir[3]	ALURes[0]	15.015	4.670	10.345	∞	input port clock
Path 24	∞	7	5	21	routir[3]	ALURes[3]	14.530	5.058	9.472	∞	input port clock
Path 25	∞	3	2	21	routir[3]	LD2	9.199	4.100	5.099	∞	input port clock
Path 26	∞	3	2	21	routir[3]	LD1	8.964	3.868	5.096	∞	input port clock
Path 27	∞	3	2	21	routir[3]	LD3	8.851	4.119	4.732	∞	input port clock
Path 28	∞	3	2	21	routir[3]	LD0	8.398	3.860	4.538	∞	input port clock



- General Information
- Timer Settings
- Design Timing Sum
- Clock Summary (1)
- Check Timing (30)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Path
  - NONE to NONE
    - Setup (10)
    - Hold (10)
  - NONE to clk
    - Setup (10)
    - Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total ...	Logic Delay	Net Delay	Requirement	Source
Path 39	∞	3	2	21	routir[3]	controlUnit0...p_s_reg[3]/D	4.944	1.405	3.540	∞	input po
Path 40	∞	3	2	21	routir[2]	controlUnit0...p_s_reg[6]/D	4.575	1.350	3.225	∞	input po
Path 41	∞	3	2	21	routir[2]	controlUnit0...p_s_reg[7]/D	4.567	1.342	3.225	∞	input po
Path 42	∞	3	2	21	routir[3]	controlUnit0...p_s_reg[0]/D	4.446	1.405	3.042	∞	input po
Path 43	∞	2	1	6	routir[4]	controlUnit0...p_s_reg[8]/D	4.060	1.307	2.753	∞	input po
Path 44	∞	2	1	6	routir[4]	controlUnit0...p_s_reg[2]/D	4.038	1.285	2.753	∞	input po
Path 45	∞	1	1	9	reset	controlUnit0...s_reg[1]/CLR	3.515	0.984	2.531	∞	input po
Path 46	∞	1	1	9	reset	controlUnit0...s_reg[4]/PRE	3.515	0.984	2.531	∞	input po
Path 47	∞	1	1	9	reset	controlUnit0...s_reg[5]/CLR	3.515	0.984	2.531	∞	input po
Path 48	∞	1	1	9	reset	controlUnit0...s_reg[3]/CLR	3.365	0.984	2.382	∞	input po



- General Information
- Timer Settings
- Design Timing Sum
- Clock Summary (1)
- Check Timing (30)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Path
  - NONE to NONE
    - Setup (10)
    - Hold (10)
  - NONE to clk
    - Setup (10)
    - Hold (10)
  - clk to NONE
    - Setup (10)
    - Hold (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Sou
Path 59	∞	6	5	42	controlUnit..._s_reg[8]/C	ALURes[4]	14.389	4.417	9.972	∞	clk
Path 60	∞	6	5	42	controlUnit..._s_reg[8]/C	ALURes[2]	14.259	4.762	9.497	∞	clk
Path 61	∞	6	5	42	controlUnit..._s_reg[8]/C	ALURes[5]	14.211	4.611	9.600	∞	clk
Path 62	∞	6	5	42	controlUnit..._s_reg[8]/C	ALURes[1]	13.831	4.369	9.462	∞	clk
Path 63	∞	6	5	42	controlUnit..._s_reg[8]/C	ALURes[0]	13.301	4.163	9.138	∞	clk
Path 64	∞	6	5	42	controlUnit..._s_reg[8]/C	ALURes[3]	12.920	4.814	8.105	∞	clk
Path 65	∞	3	3	6	controlUnit..._s_reg[7]/C	state[0]	8.182	3.941	4.241	∞	clk
Path 66	∞	3	3	6	controlUnit..._s_reg[7]/C	state[2]	7.677	3.495	4.182	∞	clk
Path 67	∞	3	3	6	controlUnit..._s_reg[7]/C	state[3]	7.308	3.485	3.822	∞	clk
Path 68	∞	3	3	11	controlUnit..._s_reg[4]/C	state[1]	6.779	3.302	3.476	∞	clk