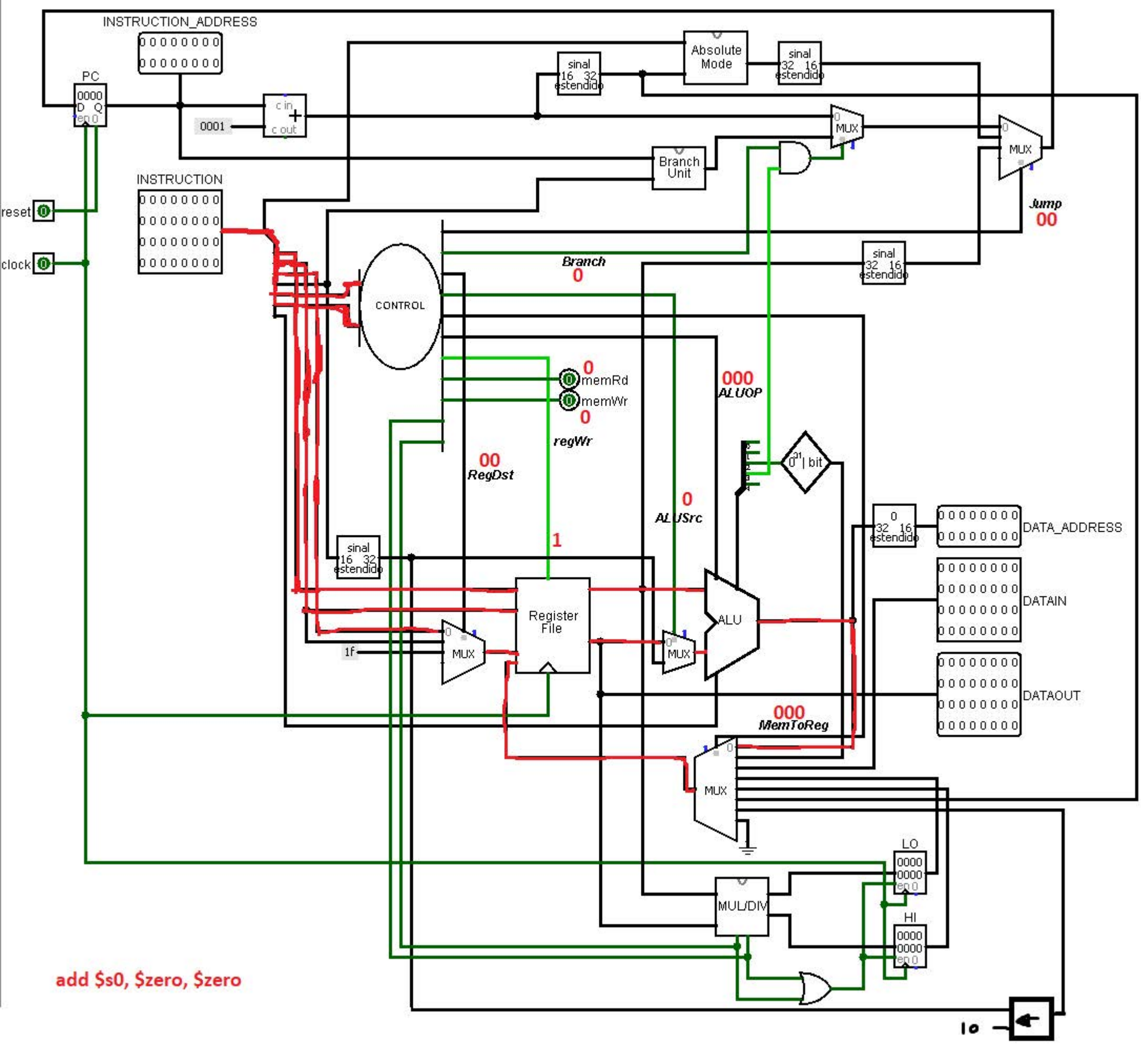
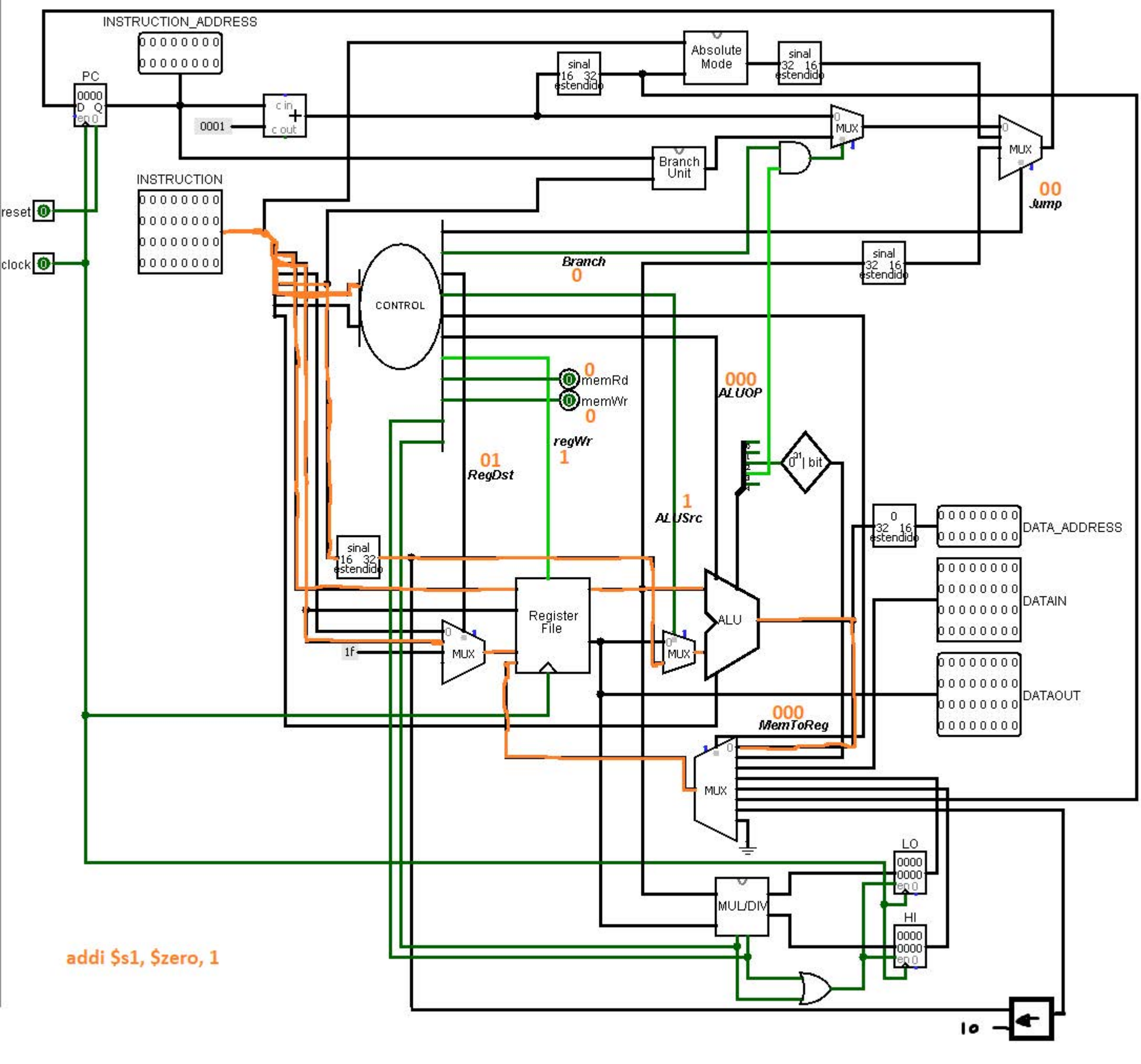

INSTRUCTION_ADDRESS
PC
0001
c in
c out
sinal 16 32 estendido
Absolute Mode
sinal 32 16 estendido
MUX
Branch Unit
Jump
00
INSTRUCTION
reset
clock
CONTROL
Branch
0
sinal 32 16 estendido
0
memRd
memWr
0
regWr
000
ALUOP
00
RegDst
0
ALUSrc
1
bit
DATA_ADDRESS
DATAIN
DATAOUT
sinal 16 32 estendido
Register File
ALU
1f
000
MemToReg
LO
HI
MUL/DIV
add $s0, $zero, $zero
10


INSTRUCTION_ADDRESS
PC
0001
c in
c out
sinal 16 32 estendido
Absolute Mode
sinal 32 16 estendido
MUX
Branch Unit
00
Jump
INSTRUCTION
reset
clock
CONTROL
Branch
0
sinal 32 16 estendido
0
memRd
memWr
0
regWr
1
01
RegDst
000
ALUOP
1
ALUSrc
1 bit
0
32 16 estendido
DATA_ADDRESS
DATAIN
DATAOUT
sinal 16 32 estendido
Register File
ALU
MUX
1f
000
MemToReg
LO
HI
MUL/DIV
addi $s1, $zero, 1
10

add $s0, $zero, $zero
0000 0000 0000 0000 1000 0000 0010 0000
00008020

addi $s1, $zero, 1
0010 0000 0001 0001 0000 0000 0000 0001
20110001

addi $v0, $zero, 1
0010 0000 0000 0010 0000 0000 0000 0001
20020001

add $a0, $zero, $s0
0000 0000 0001 0000 0010 0000 0010 0000
00102020

addi $v0, $zero, 4
0010 0000 0000 0010 0000 0000 0000 0100
20020004

lui
0011 1100 0000 0001 0001 0000 0000 0001
3 c 0 1 1 0 0 1
ori
0011 0100 0010 0100 0000 0000 0000 0000
3 4 2 4 0 0 0 0

addi $v0, $zero, 1
0010 0000 0000 0010 0000 0000 0000 0001
20020001

add $a0, $zero, $s1
0000 0000 0001 0001 0010 0000 0010 0000
0 0 1 1 2 0 2 0

addi $v0, $zero, 4
0010 0000 0000 0010 0000 0000 0000 0100
2 0 0 2 0 0 0 4

lui
0011 1100 0000 0001 0001 0000 0000 0001
3 c 0 1 1 0 0 1
ori
0011 0100 0010 0100 0000 0000 0000 0000
3 4 2 4 0 0 0 0

add $t2, $zero, $zero

0000 0000 0000 0000 0101 0000 0010 0000
0 0 0 0 5 0 2 0

addi $t4, $zero, 9
0010 0000 0000 0110 0000 0000 0000 1001
2 0 0 c 0 0 0 9

slt $t3, $t2, $t4
0000 0001 0100 1100 0101 1000 0010 1010
014c582a

beq $t3, $zero, SAI
0001 0001 0110 0000 0000 0000 0001 0010
11600012

add $s0, $s1, $s0
0000 0010 0011 0000 1000 0000 0010 0000
0 2 3 0 8 0 2 0

addi $v0, $zero, 1
0010 0000 0000 0010 0000 0000 0000 0001
2 0 0 2 0 0 0 1

add $a0, $zero, $s0
0000 0000 0001 0000 0010 0000 0010 0000
0 0 1 0 2 0 2 0

addi $v0, $zero, 4
0010 0000 0000 0010 0000 0000 0000 0100
2 0 0 2 0 0 0 4

lui
0011 1100 0000 0001 0001 0000 0000 0001
3 c 0 1 1 0 0 1
ori
0011 0100 0010 0100 0000 0000 0000 0000
3 4 2 4 0 0 0 0

add $s1, $s0, $s1
0000 0010 0001 0001 1000 1000 0010 0000
0 2 1 1 8 8 2 0

addi $v0, $zero, 1
0010 0000 0000 0010 0000 0000 0000 0001
2 0 0 2 0 0 0 1

add $a0, $zero, $s1
0000 0000 0001 0001 0010 0000 0010 0000
0 0 1 1 2 0 2 0

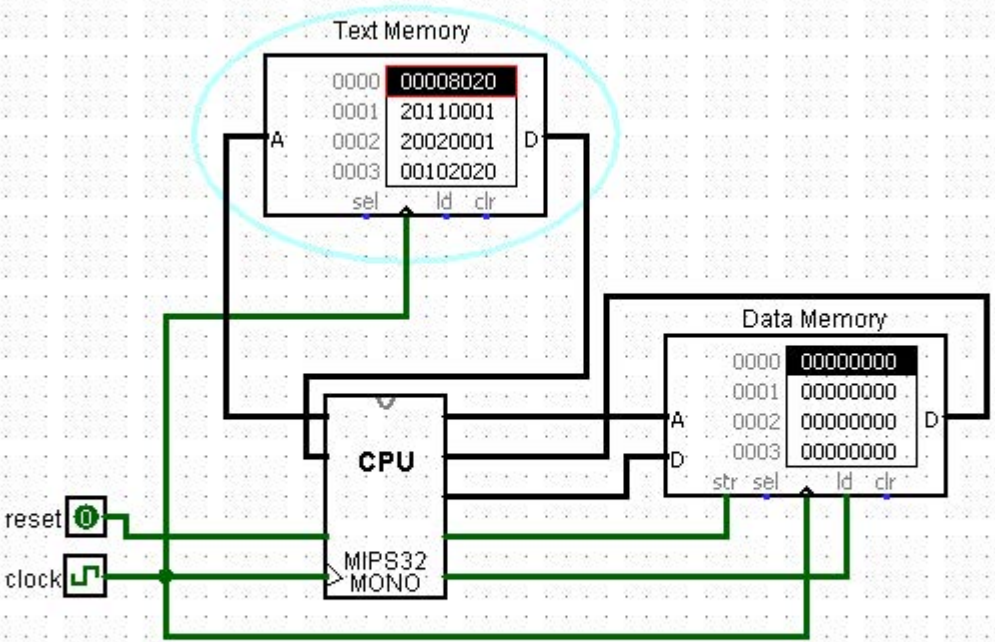
addi $v0, $zero, 4
0010 0000 0000 0010 0000 0000 0000 0100
2 0 0 2 0 0 0 4

lui
0011 1100 0000 0001 0001 0000 0000 0001
3 c 0 1 1 0 0 1
ori
0011 0100 0010 0100 0000 0000 0000 0000
3 4 2 4 0 0 0 0

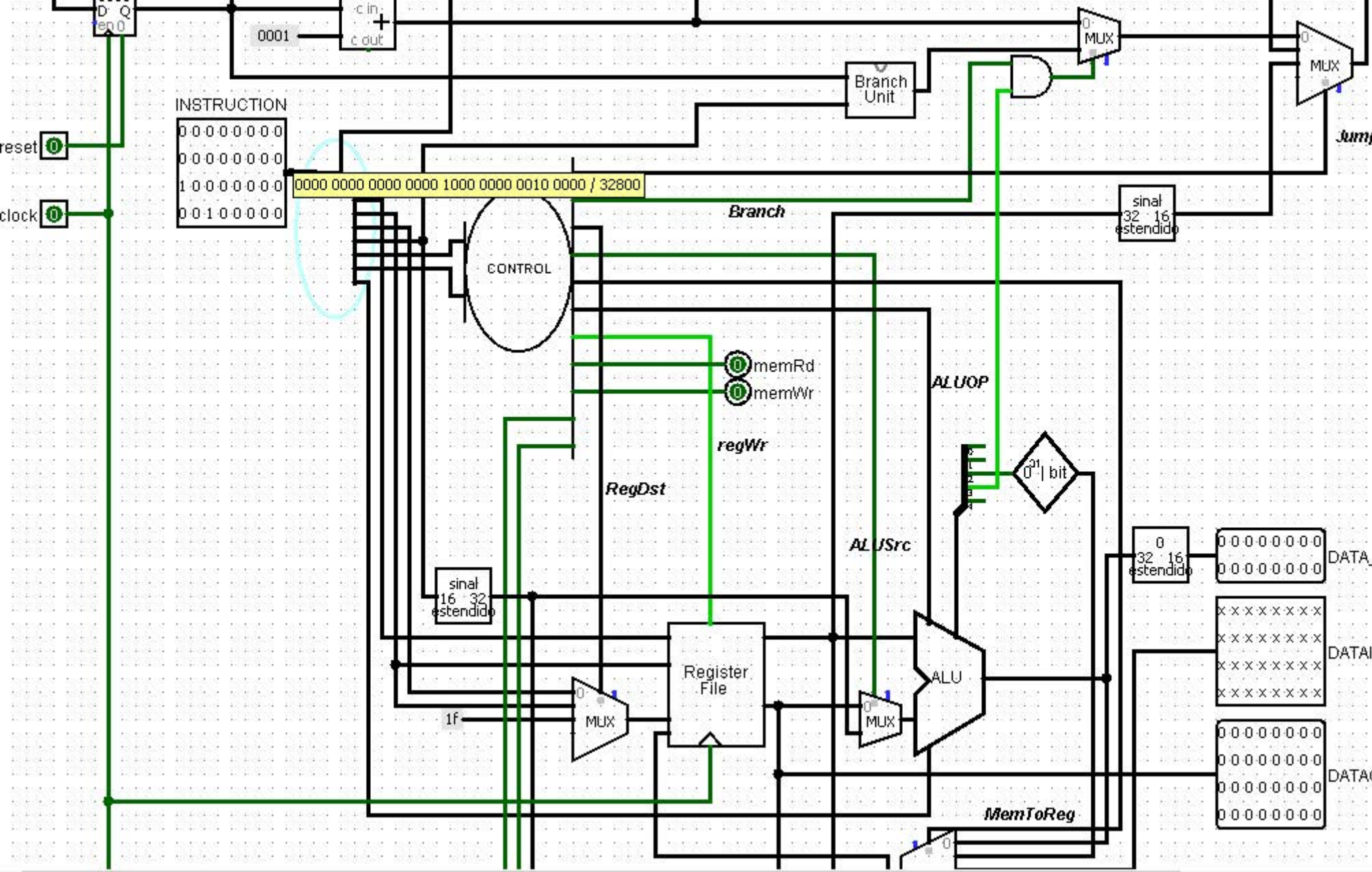
addi $t2, $t2, 1
0010 0001 0100 1010 0000 0000 0000 0001
2 1 4 a 0 0 0 1

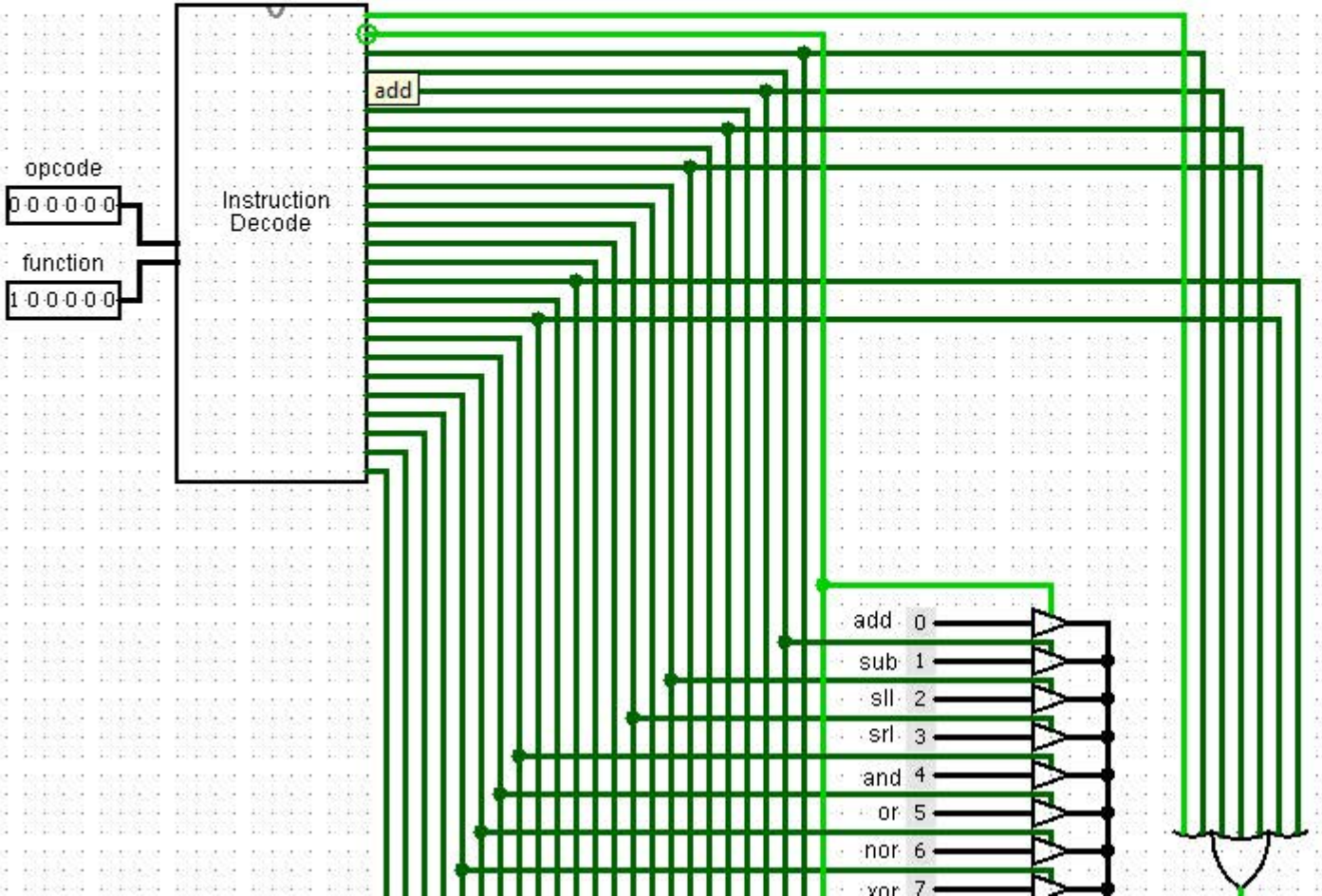
j for
0000 1000 0000 0000 0000 0000 0000 1100
0800000c

addi $v0, $zero, 10
0010 0000 0000 0010 0000 0000 0000 1010
2 0 0 2 0 0 0 a



Projeto:	MIPS-32 Monociclo set de Intruções Reduzidas	
	Versão: 0.55	Data: 22/05/2016
Projetista:	*Prof. Dr. rer. nat. Daniel Duarte Abdala*	


INSTRUCTION
0000 0000 0000 0000 1000 0000 0010 0000 / 32800
reset
clock
0001
c in
c out
Branch Unit
MUX
Jump
Branch
sinal 32 16 estendido
CONTROL
memRd
memWr
ALUOP
regWr
RegDst
ALUSrc
bit
sinal 16 32 estendido
0 32 16 estendido
Register File
ALU
1f
MemToReg
DATA



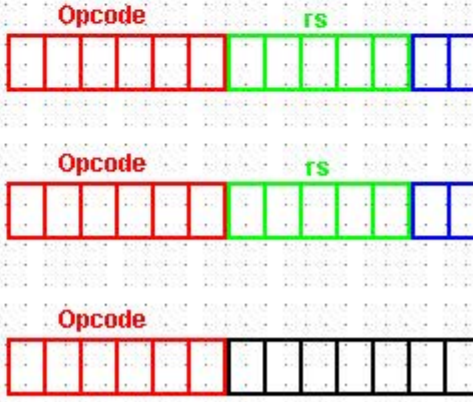
Registers

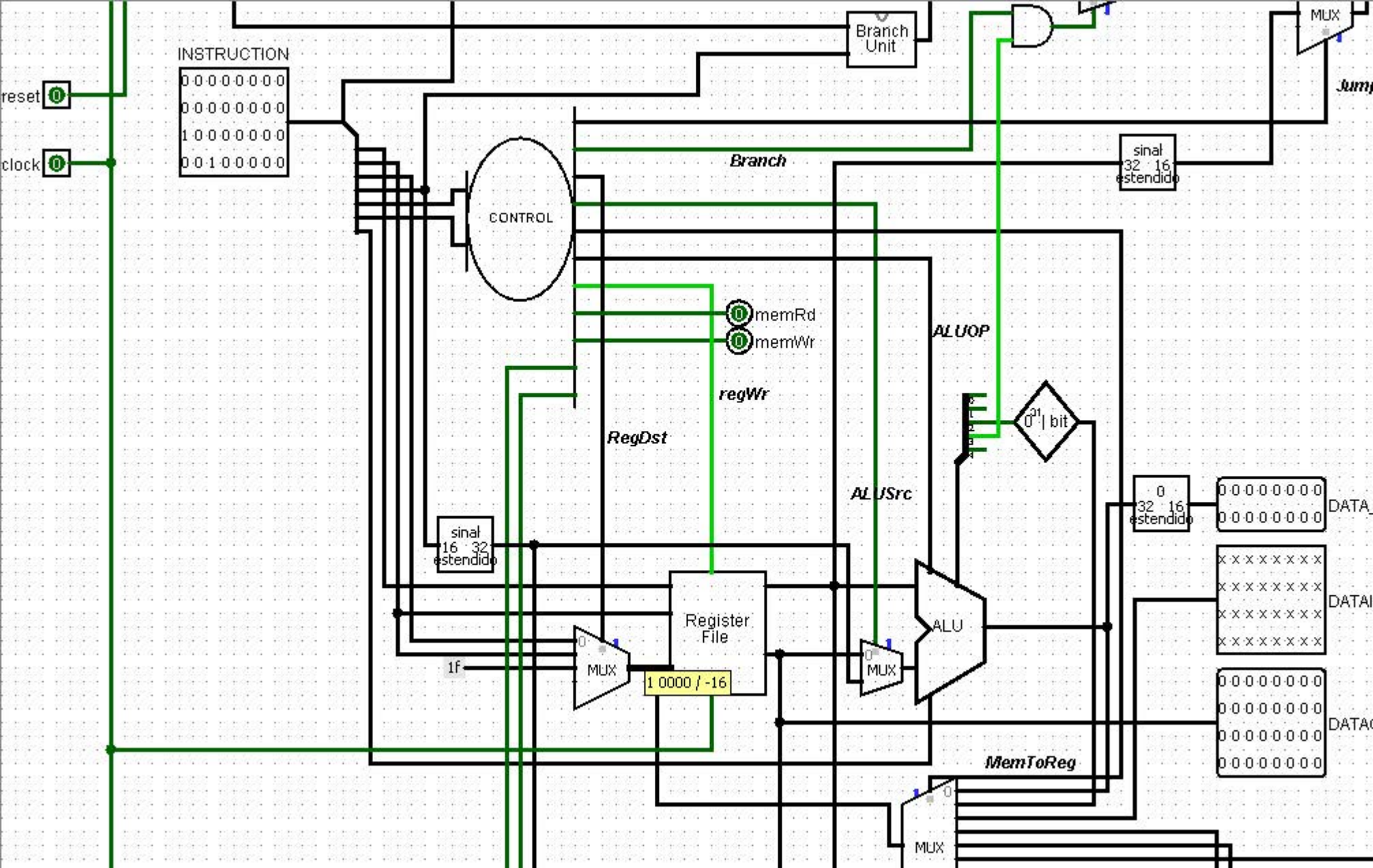
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$S0-$S7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31

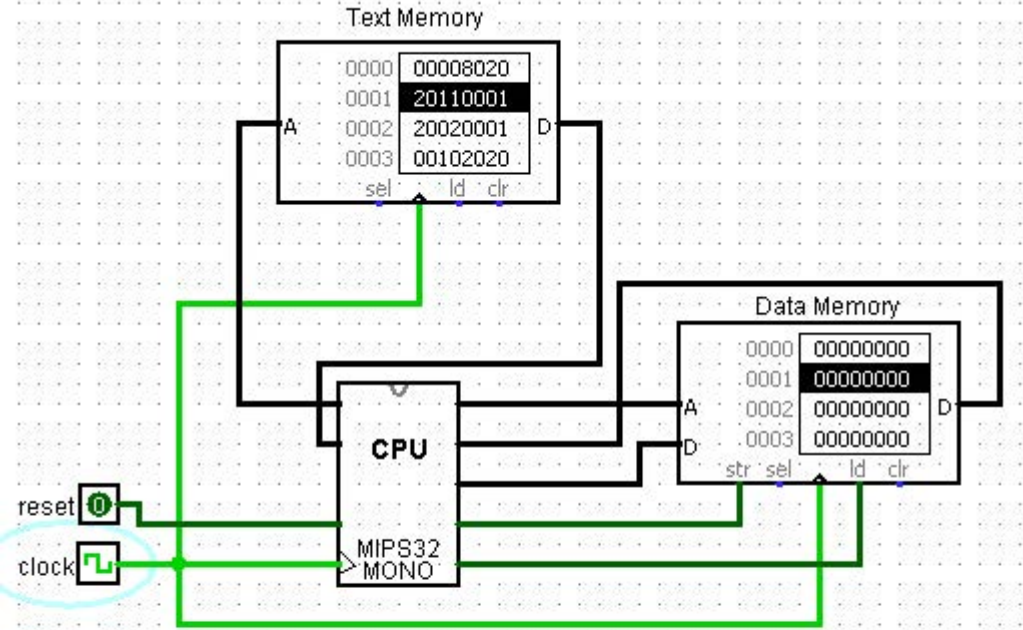
Control Sign

Instruction	op[
add	0
sub	0
and	0
or	0
nor	0
xor	0
slt	0
addi	0
andi	0
ori	0
xori	0
sll	0
srl	0
beq	0
j	0
jr	0
jal	0
lw	1
sw	1
mul	0
div	0
mfo	0
mfhi	0
lui	0

Instruction Format



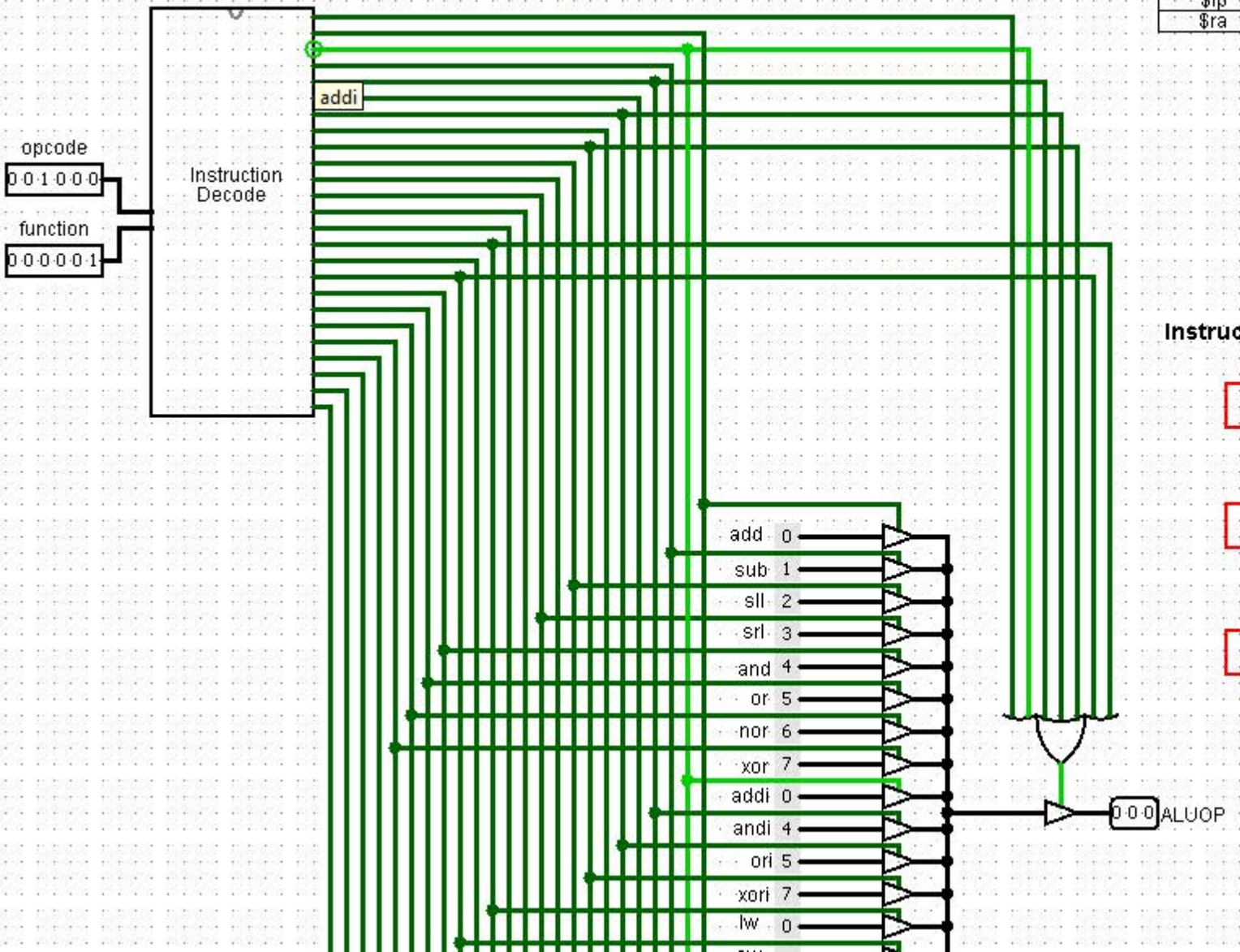

INSTRUCTION
reset
clock
Branch Unit
MUX
Jump
Branch
sinal 32 16 estendido
CONTROL
memRd
memWr
ALUOP
regWr
RegDst
ALUSrc
bit
sinal 16 32 estendido
0 32 16 estendido
DATA
DATA
DATA
Register File
1f
MUX
1 0000 / -16
MUX
ALU
MemToReg
MUX



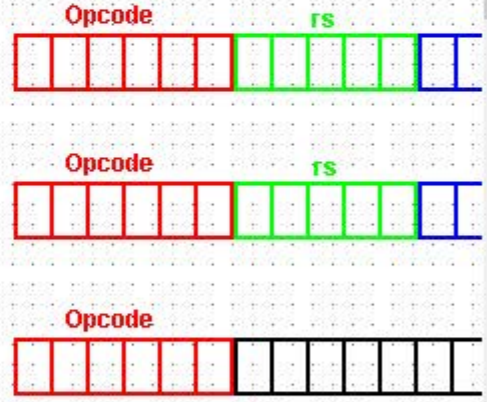
Projeto:	**MIPS-32 Monociclo set de Intruções Reduzidas**		
		Versão: 0.55	**Data: 22/05/2016**
Projetista:	***Prof. Dr. rer. nat. Daniel Duarte Abdala***		

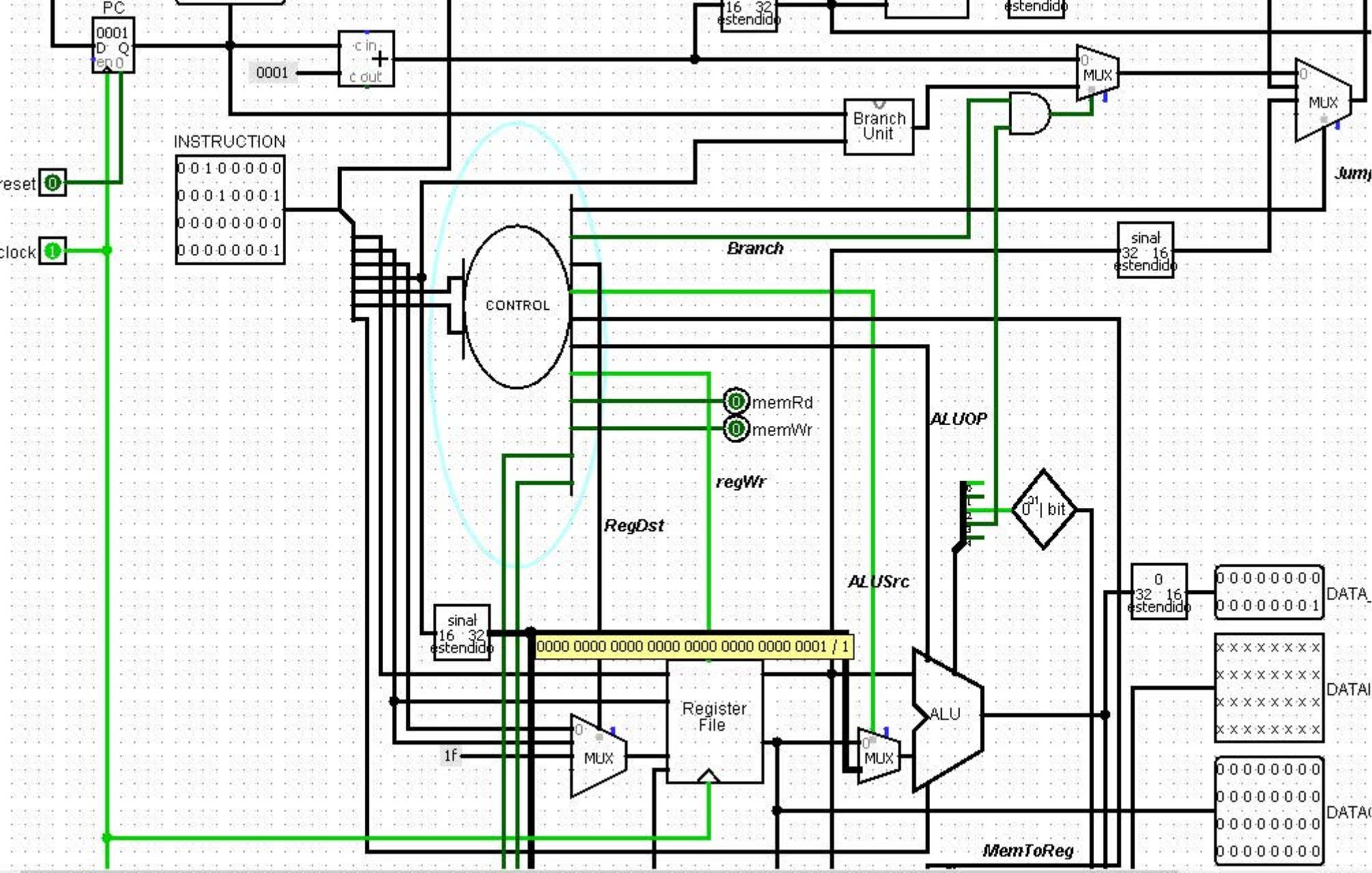
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31

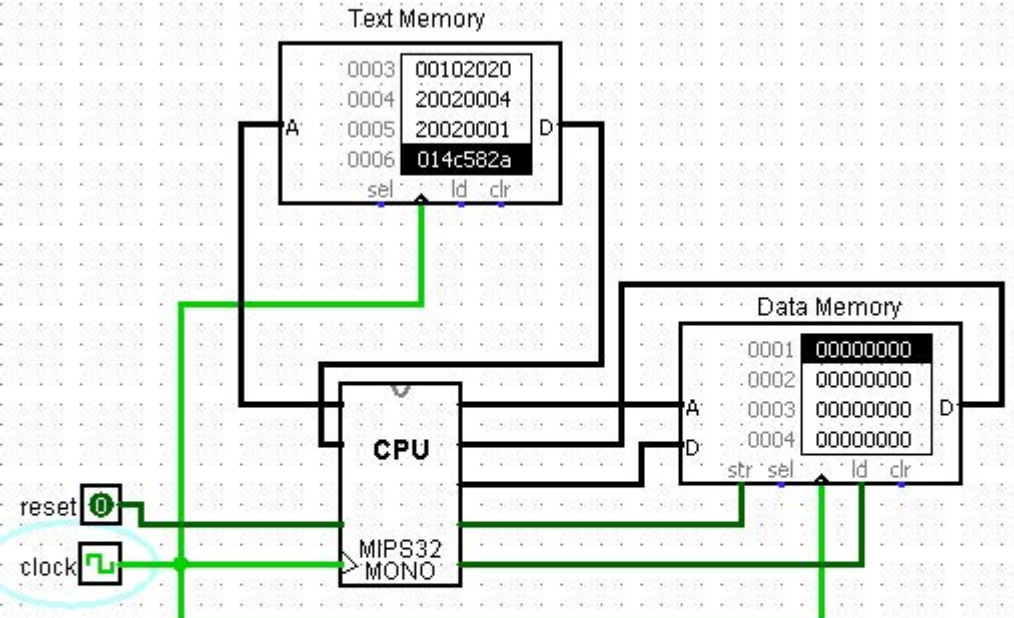
slt	0
addi	0
andi	0
ori	0
xori	0
sll	0
srl	0
beq	0
j	0
jr	0
jal	0
lw	1
sw	1
mul	0
div	0
mfo	0
mfhi	0
lui	0



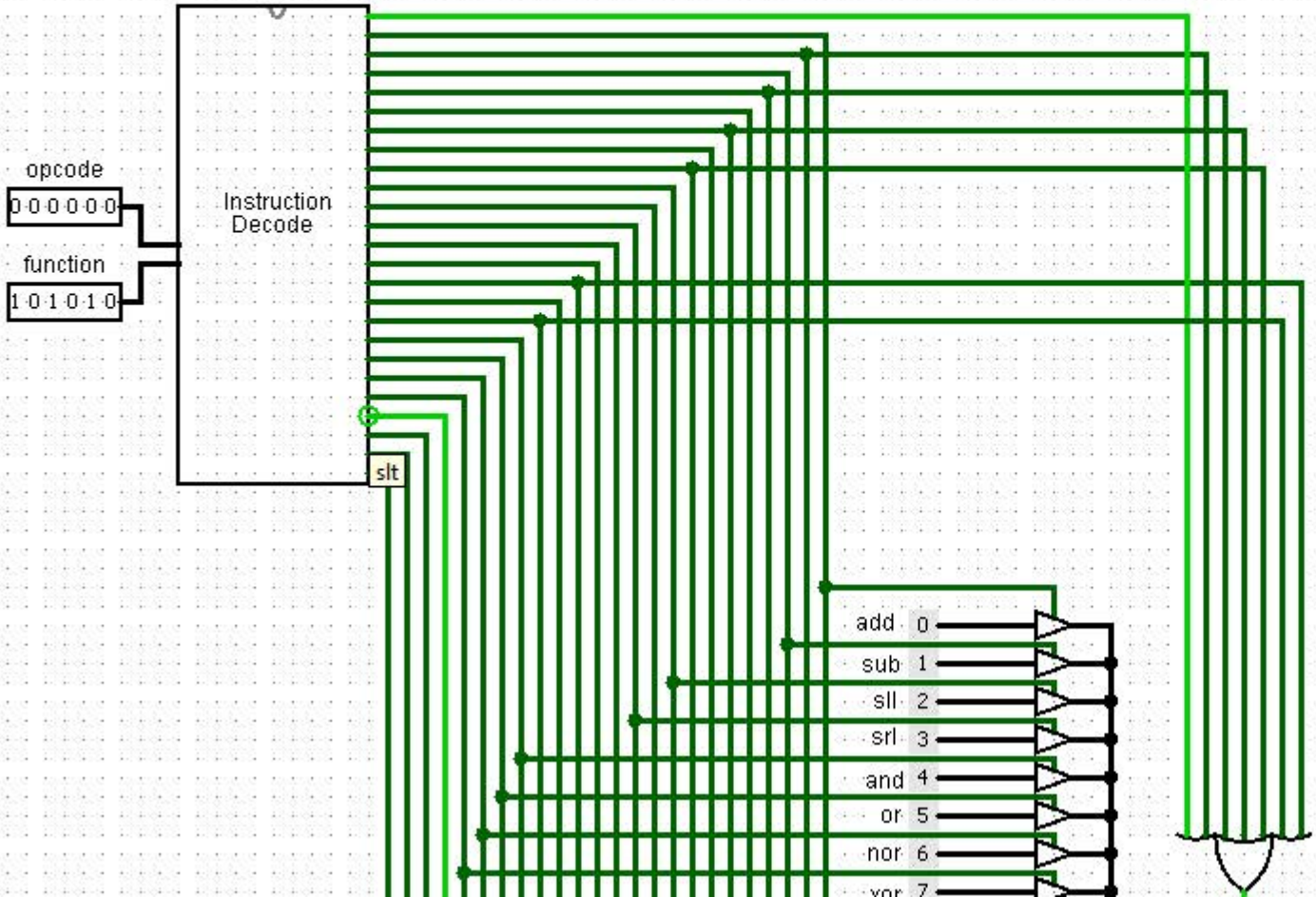
Instruction Format




PC
0001
D Q
en 0
0001
c in
c out
16 32
estendido
MUX
Branch Unit
INSTRUCTION
reset
clock
CONTROL
Branch
sinal
32 16
estendido
memRd
memWr
regWr
RegDst
ALUOP
ALUSrc
1 bit
0000 0000 0000 0000 0000 0000 0000 0001 / 1
Register File
ALU
1f
MemToReg
DATA
DATAI
DATA



Projeto:	**MIPS-32 Monociclo set de Intruções Reduzidas**		
		Versão: 0.55	**Data: 22/05/2016**
Projetista:	***Prof. Dr. rer. nat. Daniel Duarte Abdala***		



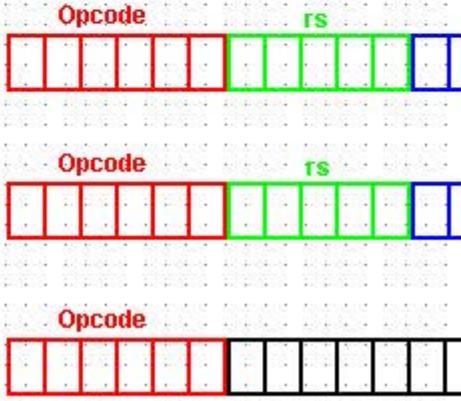
Registers

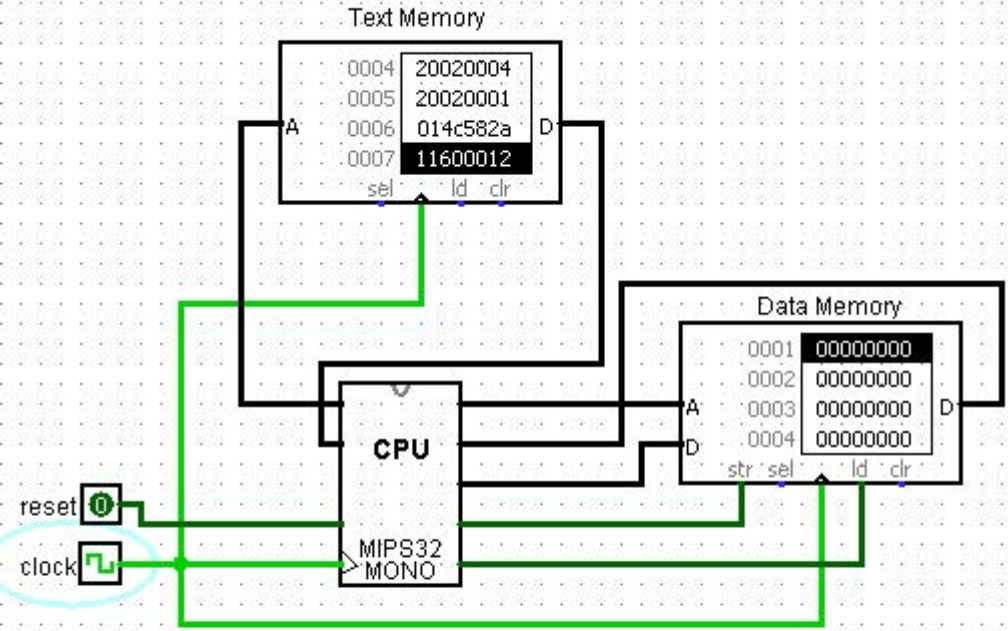
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$S0-$S7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31

Control Sig

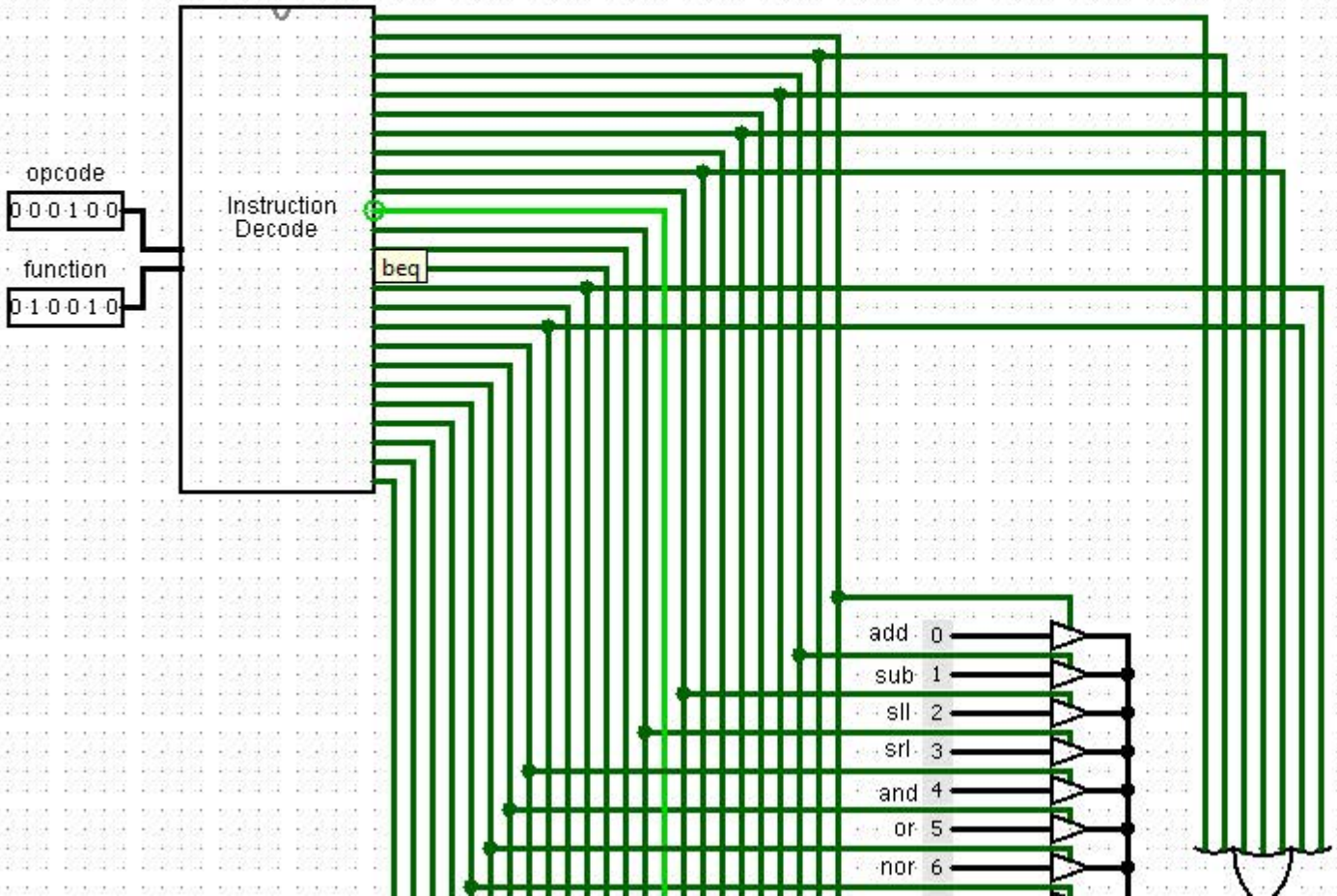
Instruction	op
add	
sub	
and	
or	
nor	
xor	
slt	
addi	
andi	
ori	
xori	
sll	
srl	
beq	
j	
jr	
jal	
lw	
sw	
mul	
div	
mfo	
mfhi	
lui	

Instruction Format





Projeto:	MIPS-32 Monociclo set de Intruções Reduzidas	
	Versão: 0.55	Data: 22/05/2016
Projetista:	*Prof. Dr. rer. nat. Daniel Duarte Abdala*	



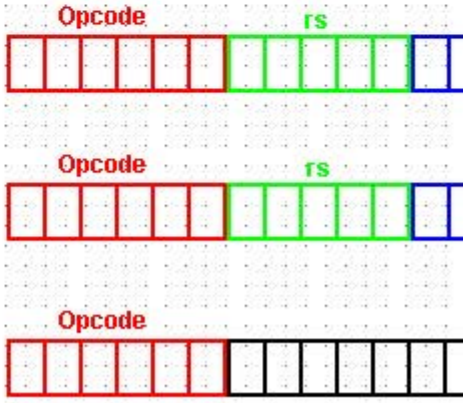
Registers

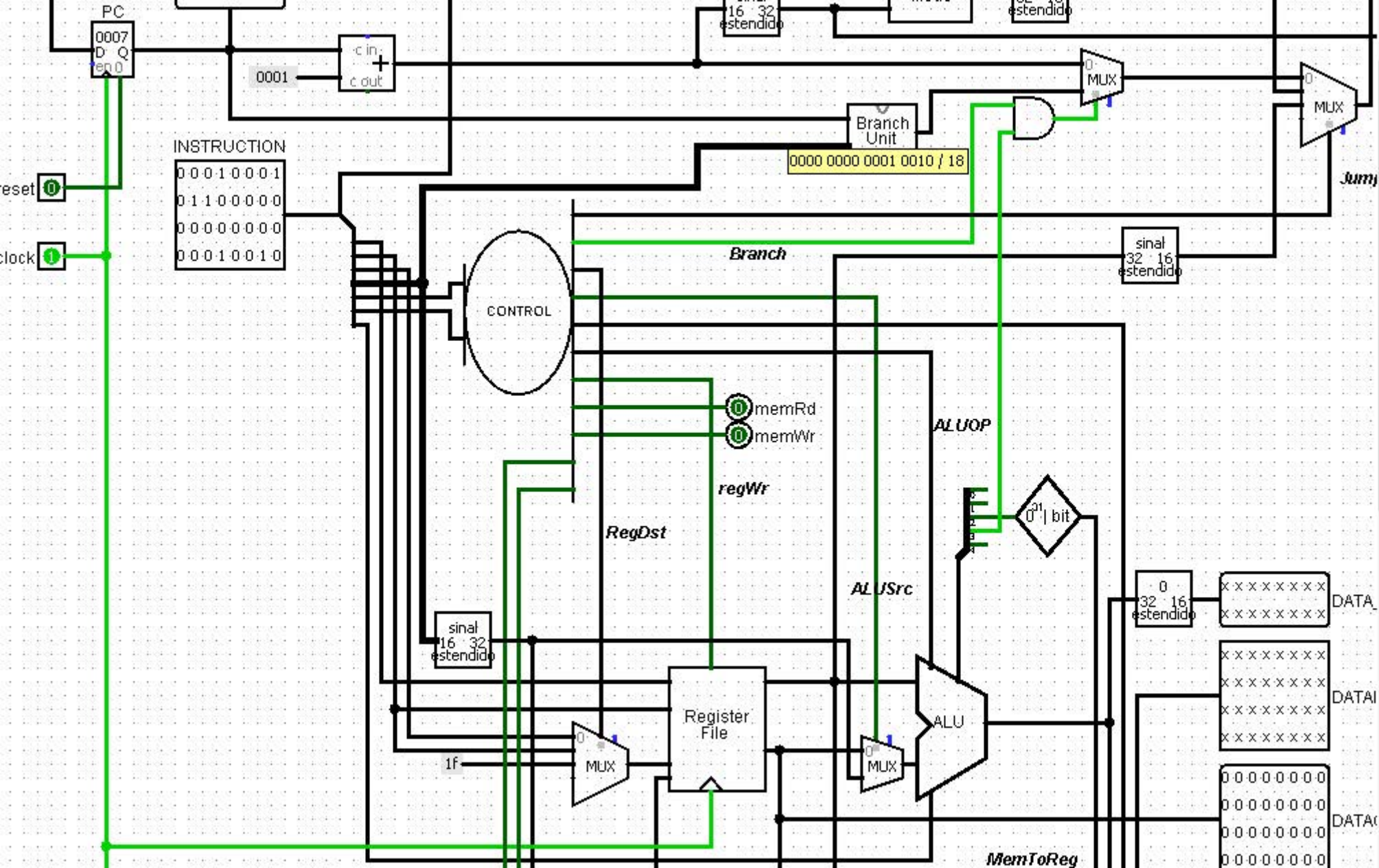
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$S0-$S7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31

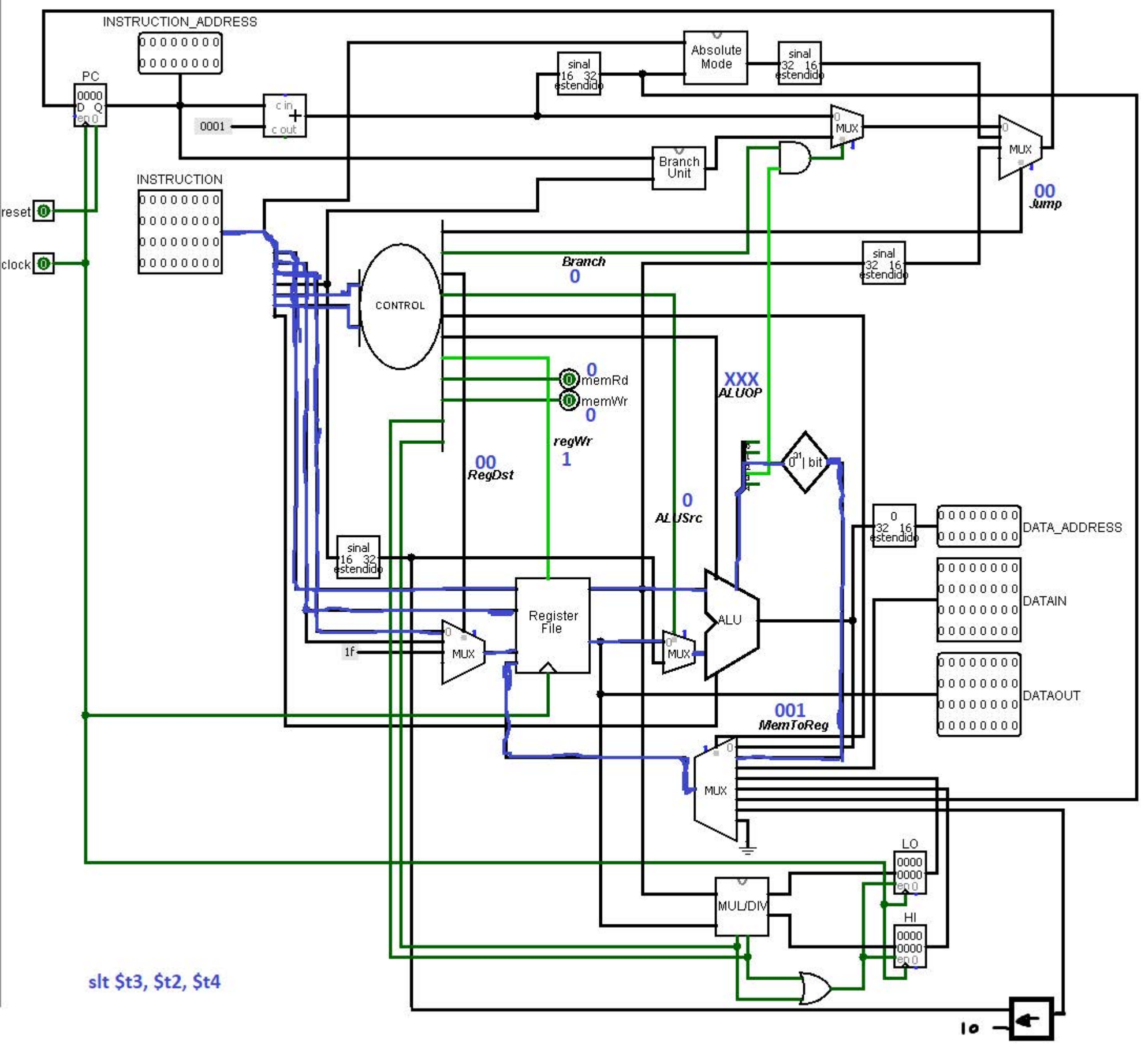
Control Sig

Instruction	op
add	0
sub	0
and	0
or	0
nor	0
xor	0
slt	0
addi	0
andi	0
ori	0
xori	0
sll	0
srl	0
beq	0
j	0
jr	0
jal	0
lw	1
sw	1
mul	0
div	0
mfo	0
mfhi	0
lui	0

Instruction Format




PC
0007
D Q
en 0
0001
c in
c out
INSTRUCTION
0 0 0 1 0 0 0 1
0 1 1 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 1 0 0 1 0
reset
clock
Branch Unit
0000 0000 0001 0010 / 18
MUX
Jump
Branch
sinal
16 32
estendido
CONTROL
memRd
memWr
regWr
RegDst
ALUOP
ALUSrc
0
31
bit
Register File
1f
ALU
DATA
MemToReg


INSTRUCTION_ADDRESS
PC
0001
c in
c out
sinal 16 32 estendido
Absolute Mode
sinal 32 16 estendido
MUX
Branch Unit
00 Jump
INSTRUCTION
reset
clock
CONTROL
Branch 0
sinal 32 16 estendido
0 memRd
memWr 0
regWr 1
00 RegDst
XXX ALUOP
0 ALUSrc
1 bit
0 32 16 estendido
DATA_ADDRESS
DATAIN
DATAOUT
sinal 16 32 estendido
Register File
ALU
MUX
1f
001 MemToReg
LO
HI
MUL/DIV
10
slt $t3, $t2, $t4