0.1 Simulink: minseg_M2V3_2017a.slx

minseg_M2V3_2017a.slx is the label of the Simulink model file. The label includes the label of the hardware which it represents as well as the version of the Mathworks Software Suite with which it was created. [Using the model in a different version of the Simulink will require conversion; therefore, the two files will not be equivalent.]

The Simulink model is hierarchical. The sections which follow will describe the model and will be similarly organized, as depicted in the extended-precision list of contents below.

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0.1.1 Root

The top level of the model, also known as the model root, is depicted in Figure 0.1.

The model root is contains the three primary components of the system:

- Plant
- Controller
- $\bullet\,$ Board Inputs and Outputs

0.1.1.1 Bus Structures

Note that all of the components are passed into a bus structure, and that those bus structures are in turn merged into one global bus structure.

It is from this global bus structure that any notable signal in the system could be called. [The user should take care to implement a delay in the path of a signal wherever an algebraic/feedback loop may form from using a signal recursively.]

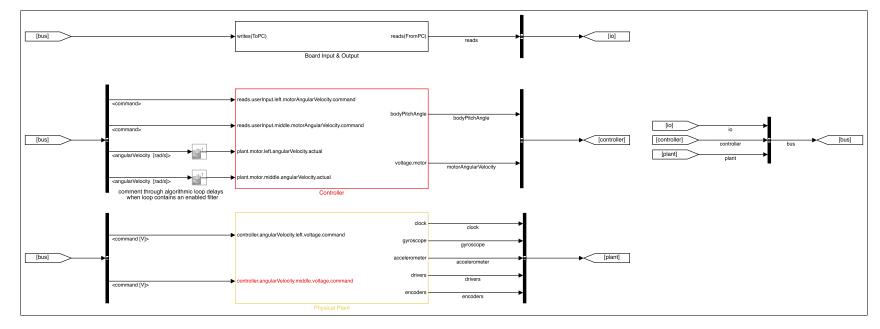


Figure 0.1: [Simulink]: Root

- 0.1.2 Plant
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0.1.2.2 Hardware-Equivalent Nonlinear Dynamics

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0.1.3 Controller

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