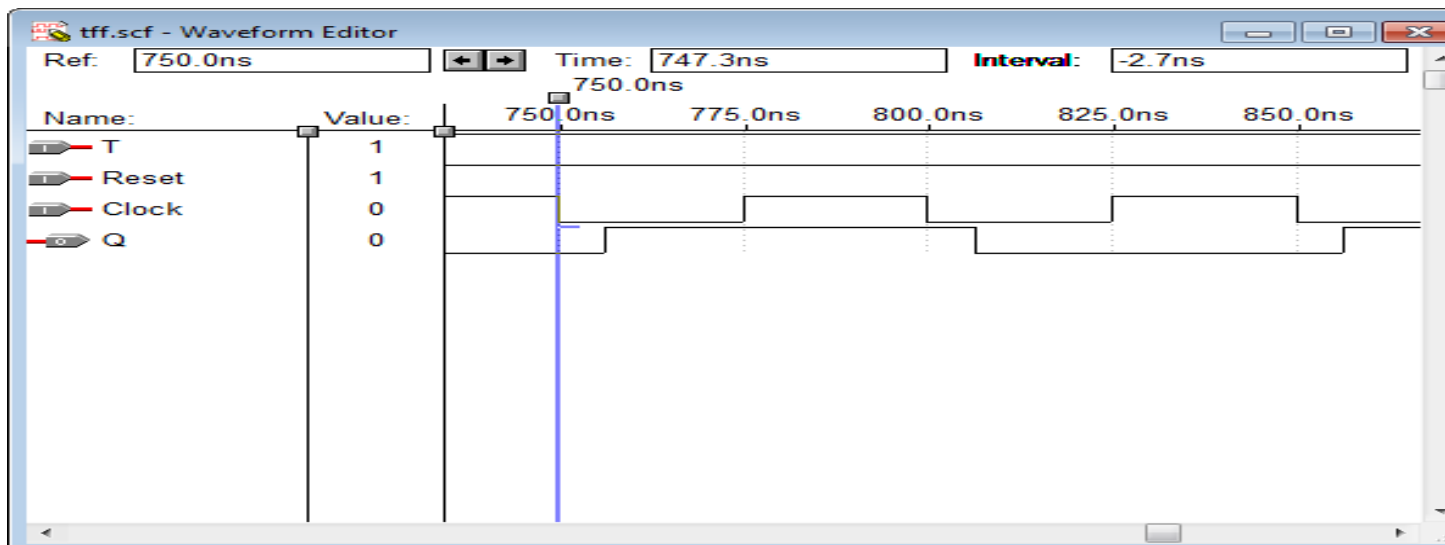


WEEK 6 LAB 6 :1.

Write behavioral Verilog code for a negative edge triggered T FF with asynchronous active low reset.

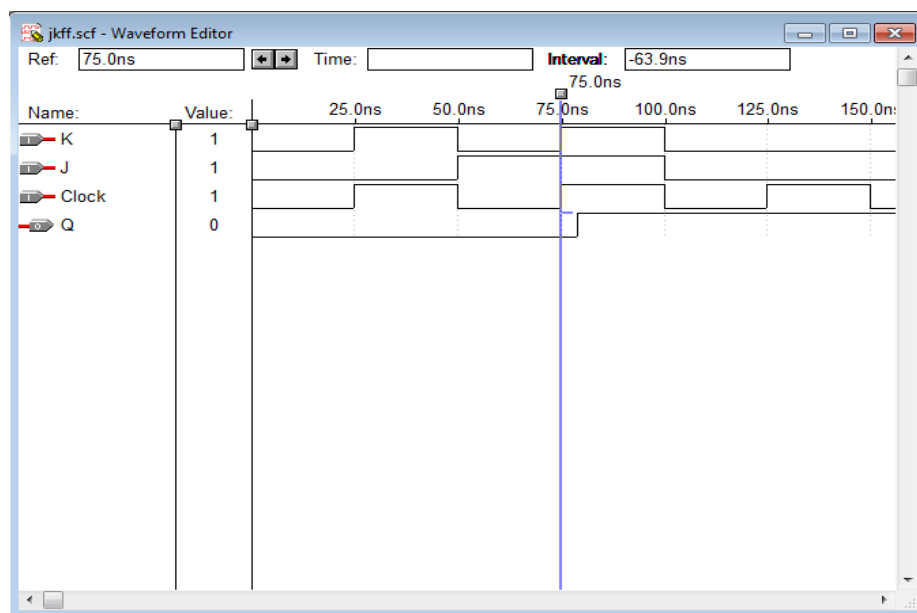
```
module tff(T,Clock,Reset,Q);  
input T,Clock, Reset;  
output Q;  
reg Q;  
always @ (negedge Clock or negedge Reset)  
    if(!Reset)  
        Q <= 0;  
    else  
        if(T)  
            Q <= ~Q;  
        else  
            Q <= Q;  
endmodule
```

**OUTPUT :**

2. Write behavioral Verilog code for a positive edge-triggered JK FF with synchronous active high reset .

```
module jkff(J,K,Clock,Q);  
    input J, K, Clock;  
    output Q;  
    reg Q;  
    always @ (posedge Clock)  
        begin  
            case({J, K})  
                0: Q <= Q;  
                1: Q <= 0;  
                2: Q <= 1;  
                3: Q <= ~Q;  
            endcase  
        end  
end  
endmodule
```

**OUTPUT :**



**3.** Design and simulate the following counters

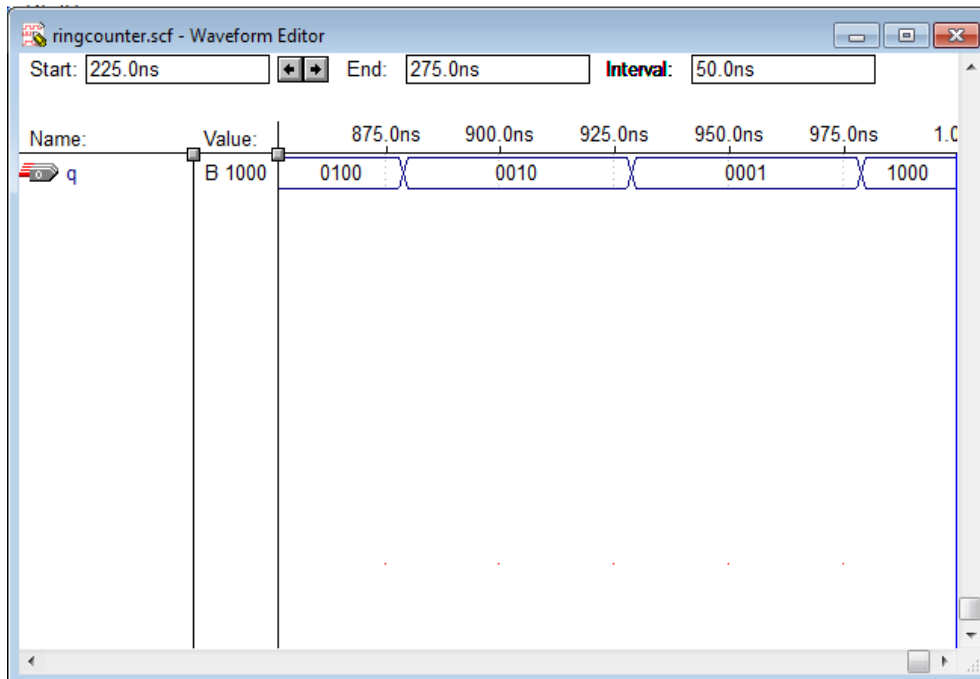
a) 4-bit ring counter.

b) 5 bit Johnson counter.

**3(a).**

```
module ringcounter(q,clock,clear);  
    input clock,clear;  
    output [3:0]q;  
    reg [3:0]q;  
    always @(posedge clock)  
        if(clear==1)  
            q<=4'b1000;  
        else  
            begin  
                q[3]<=q[0];  
                q[2]<=q[3];  
                q[1]<=q[2];  
                q[0]<=q[1];  
            end  
    end  
endmodule
```

**OUTPUT :**



**3(b).**

```
odule jonsoncounter(clock,Q);
```

```
input clock;
```

```
output [4:0]Q;
```

```
reg [4:0]Q;
```

```
always@(posedge clock)
```

```
begin
```

```
case(Q)
```

```
5'b00000: Q<=5'b10000;
```

```
5'b10000: Q<=5'b11000;
```

```
5'b11000: Q<=5'b11100;
```

```
5'b11100: Q<=5'b11110;
```

```
5'b11110: Q<=5'b11111;
```

```
5'b11111: Q<=5'b01111;
```

```
5'b01111: Q<=5'b00111;
```

```
5'b00111: Q<=5'b00011;
```

```
5'b00011: Q<=5'b00001;
```

```
5'b00001: Q<=5'b00000;
```

```
endcase
```

```
end
```

```
endmodule
```

OUTPUT :

