

IT3E01
Cadence, TSpice, Verilog Xilinx
LAB

Objectives:

- To design and draw the internal structure of the various digital integrated circuits.
- To develop Verilog HDL source code, perform simulation using relevant simulator and analyze the obtained simulation results using necessary synthesizer.
- To verify the logical operations of the digital ICs (Hardware) in the laboratory.

Course Outcomes:

After completion of the course the students will be able to

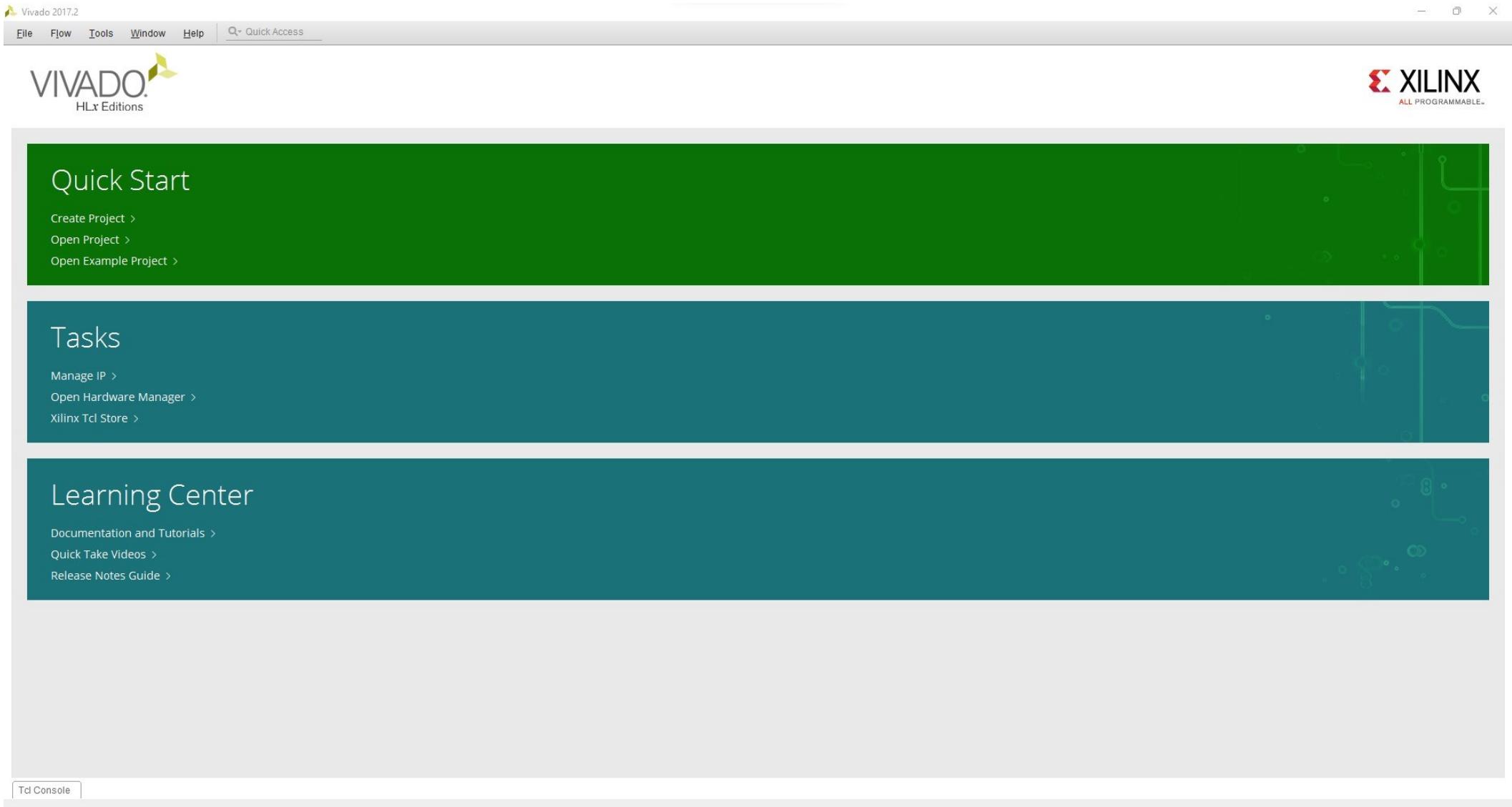
- Design and draw the internal structure of the various digital integrated circuits
- Develop Verilog HDL source code, perform simulation using relevant simulator and analyze the obtained simulation results using necessary synthesizer.
- The course helps to acquire knowledge about hardware implementation (FPGA) based.

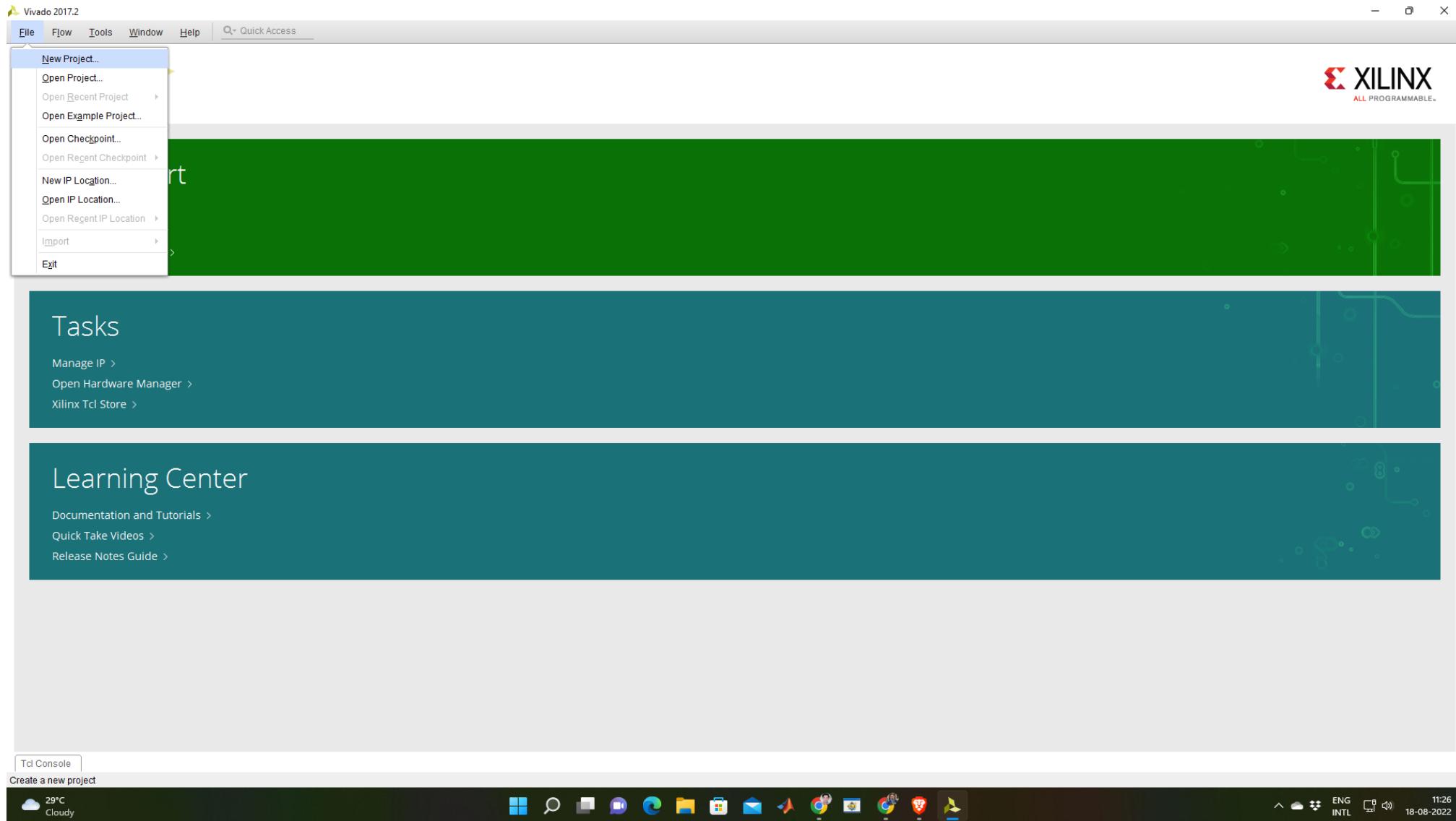
List of Experiments

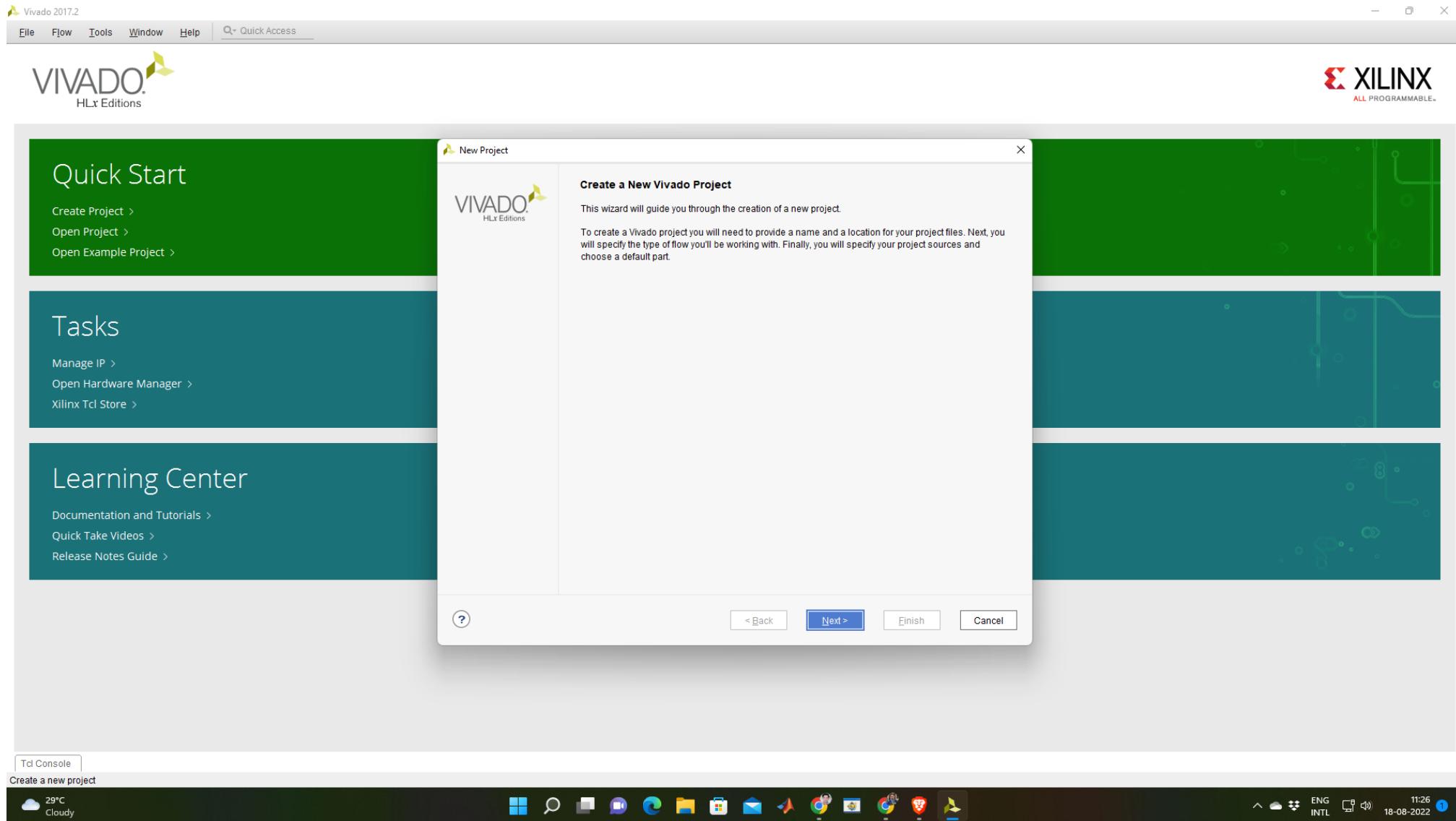
1. Design logic gates and write Verilog codes for the realization of the logic gates.
2. Design and write Verilog code for 4-bit Adder and subtractor.
3. Design and Write a Verilog code for 8×1 Multiplexer and 2×4 De-Multiplexer.
4. Design and write Verilog code for 3 to 8 Decoder and 4-bit Comparator
5. Write a Verilog code for D Flip-Flop and counter.
6. Design and write Verilog code for Shift registers and a 3-bit binary code to 3-bit grey code conversion.
7. Project

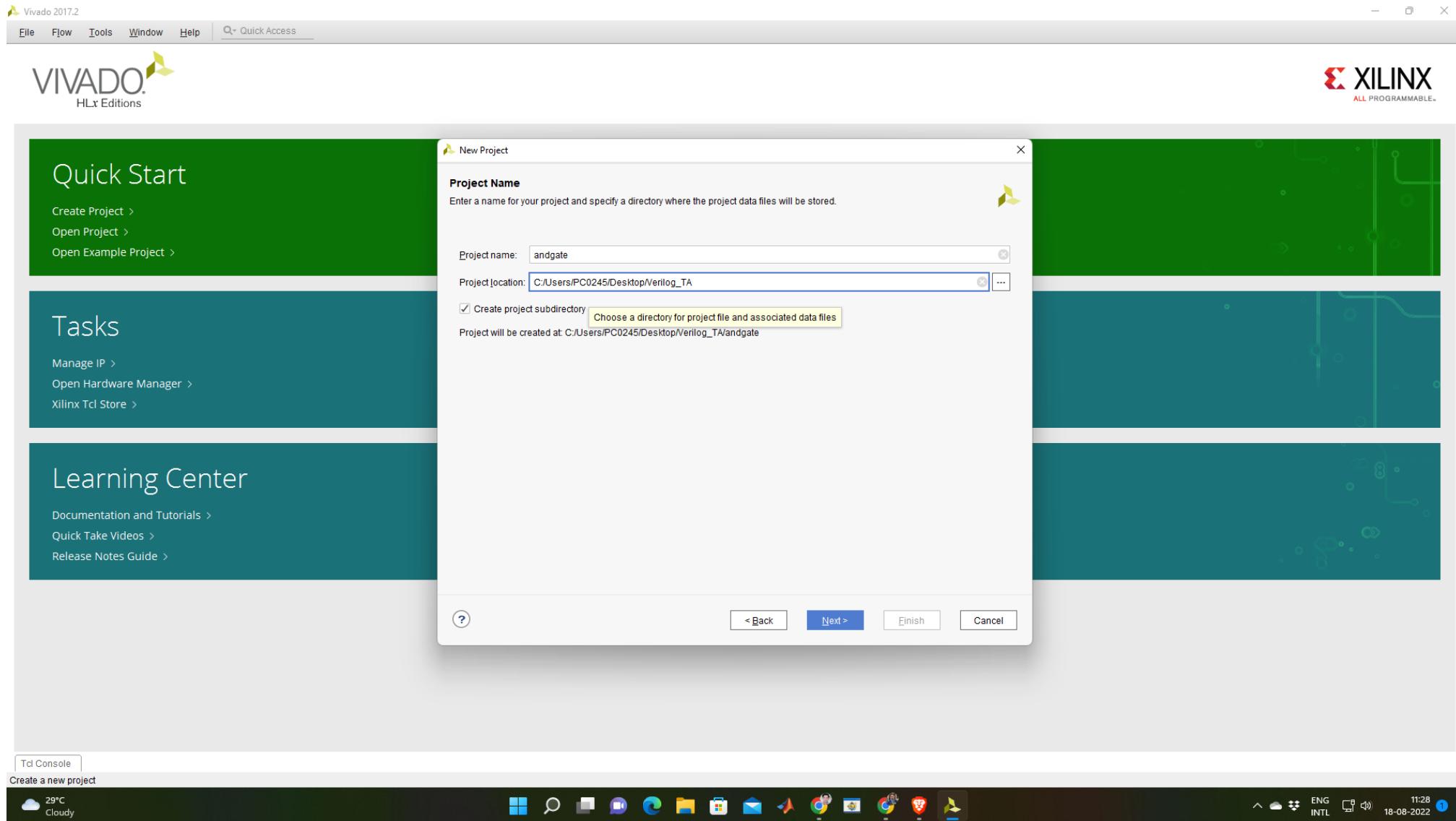
Vivado 2017.2

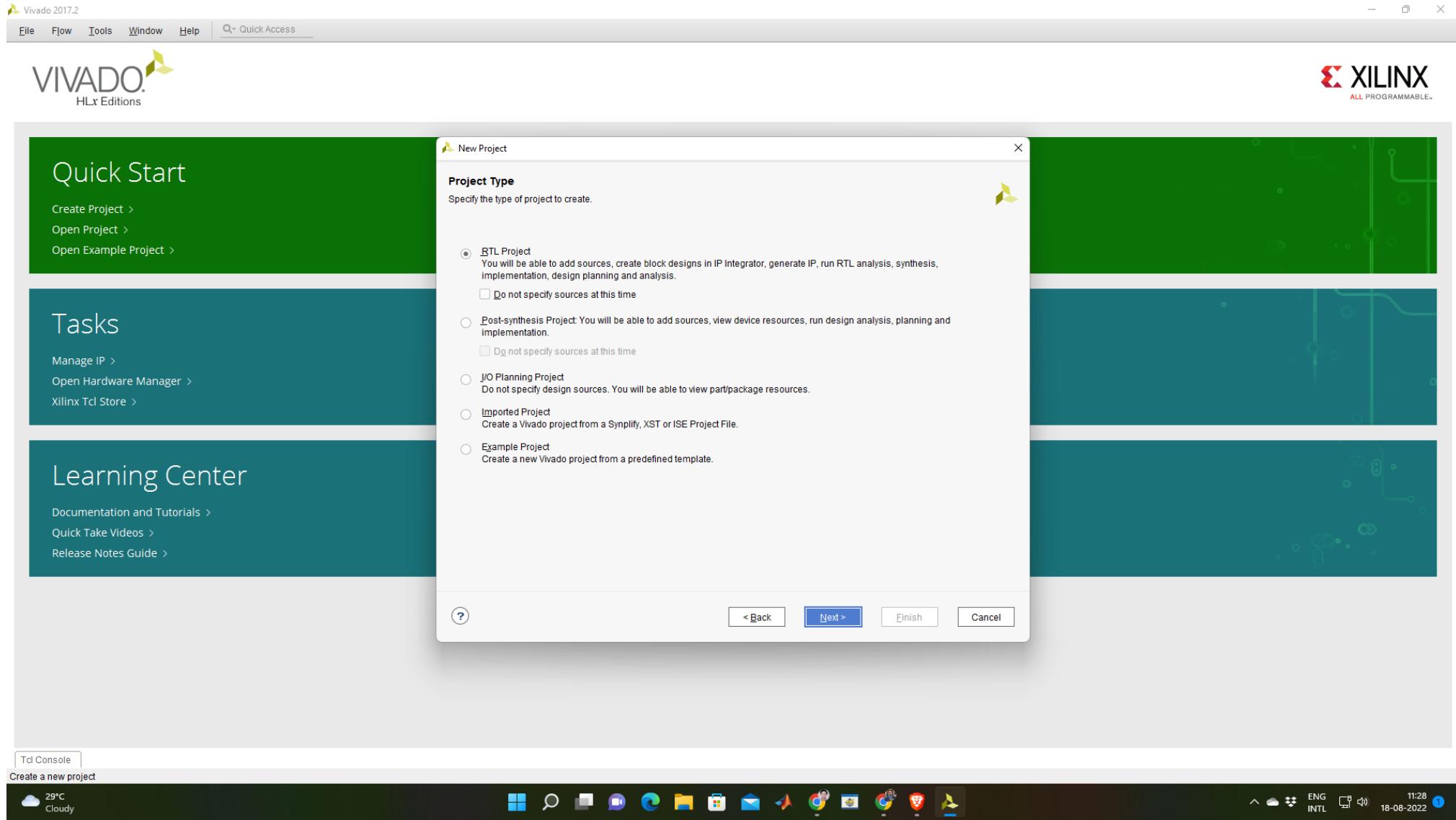
IT3E01 Lab

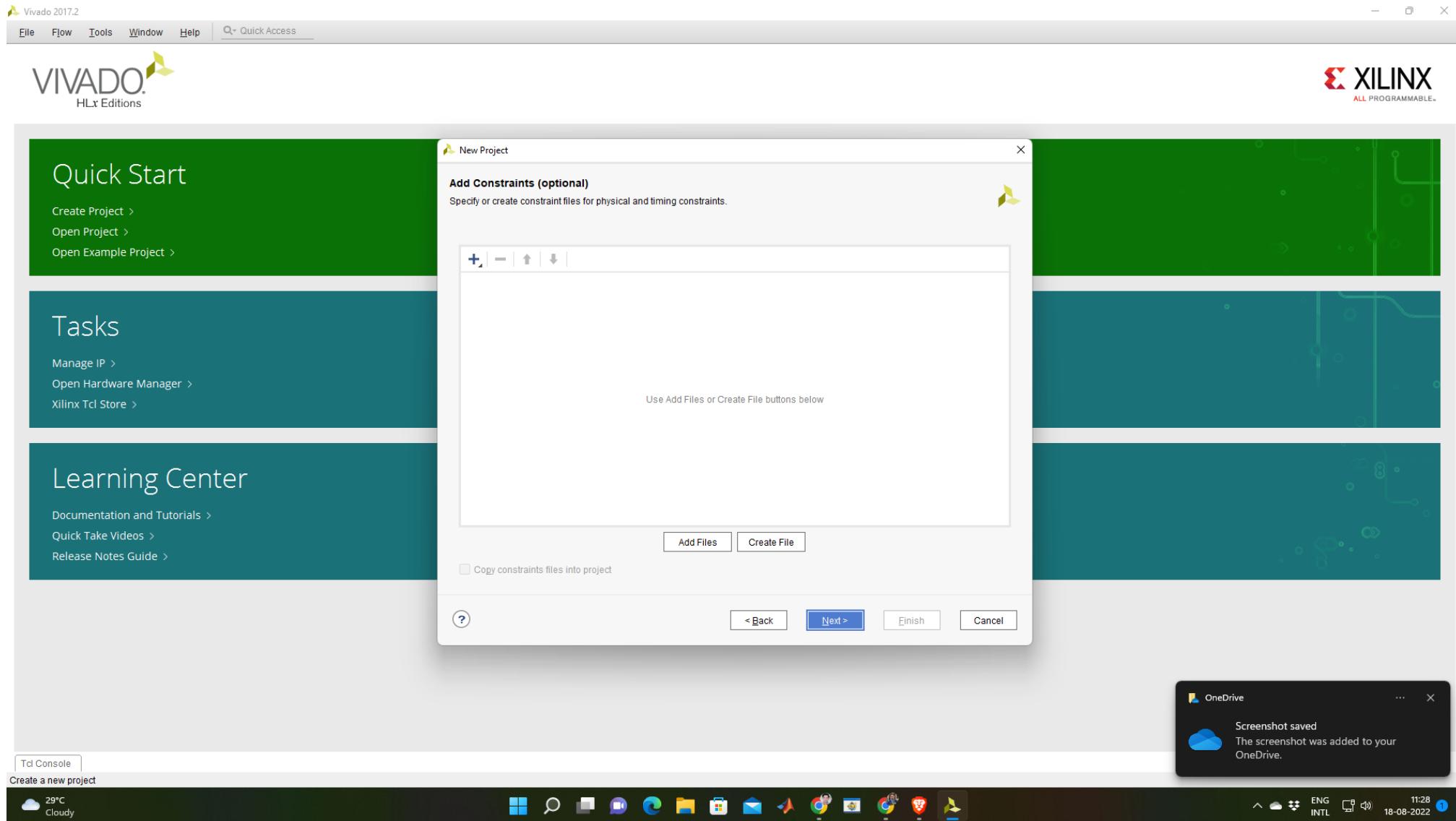


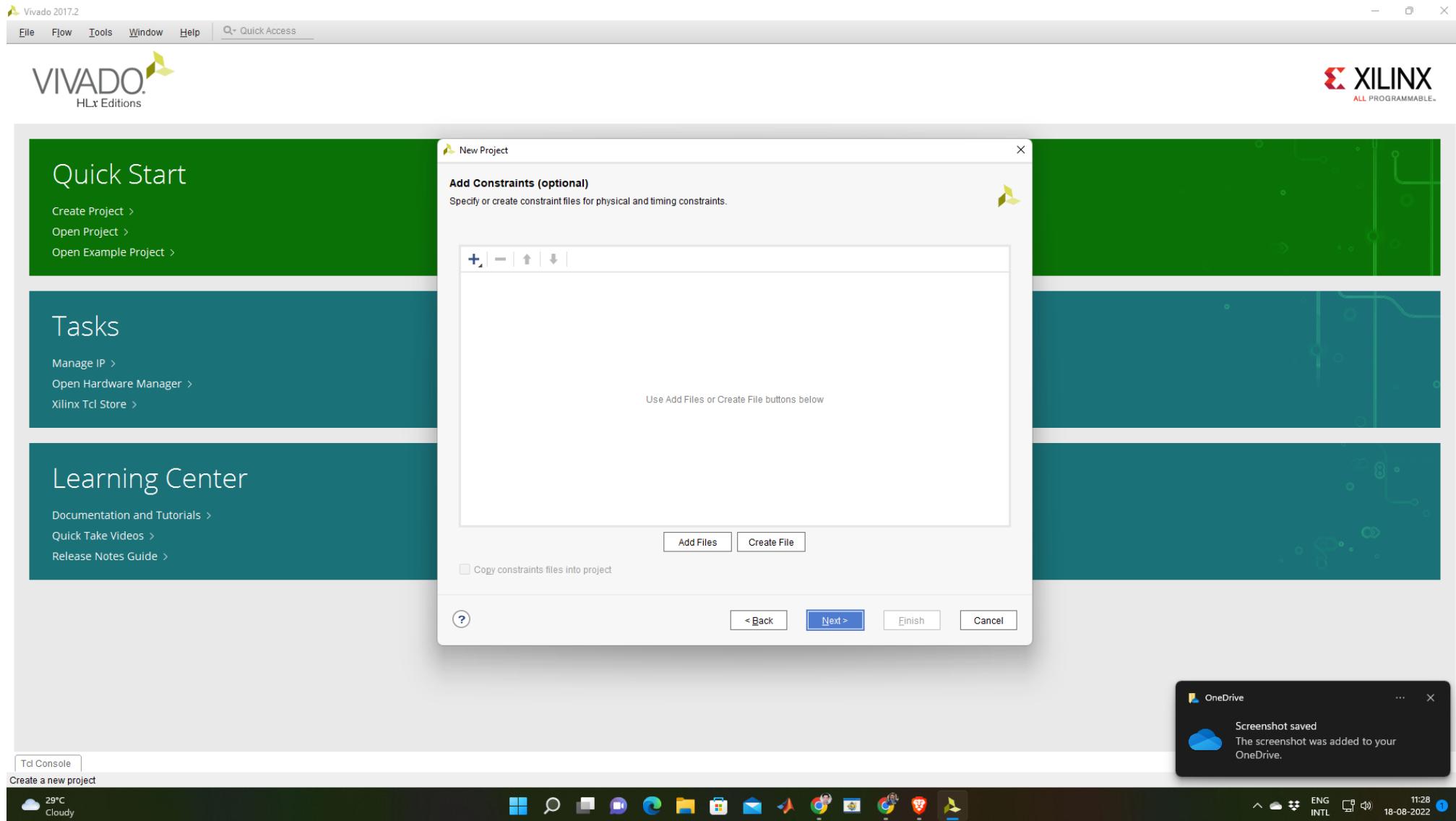


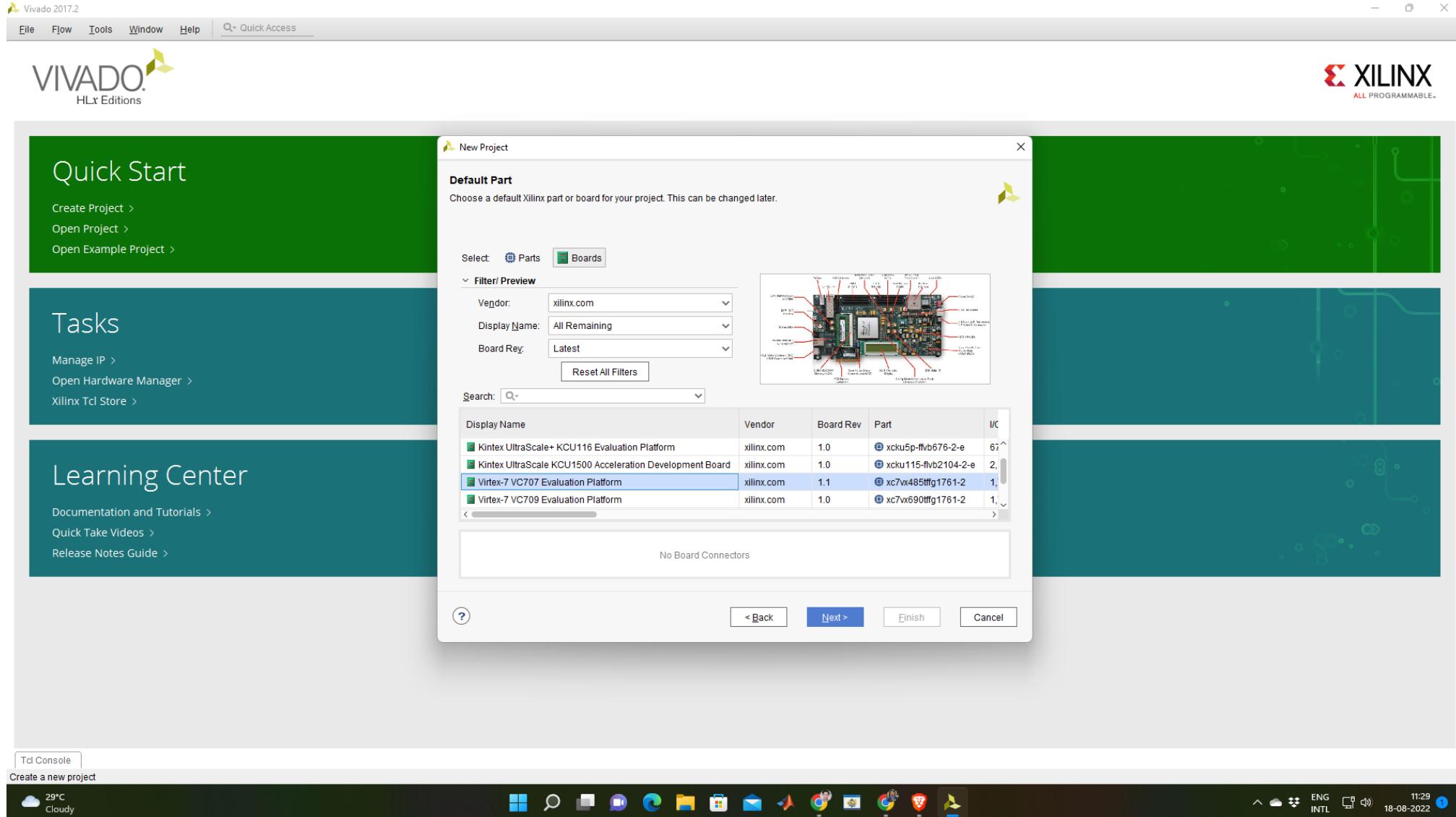


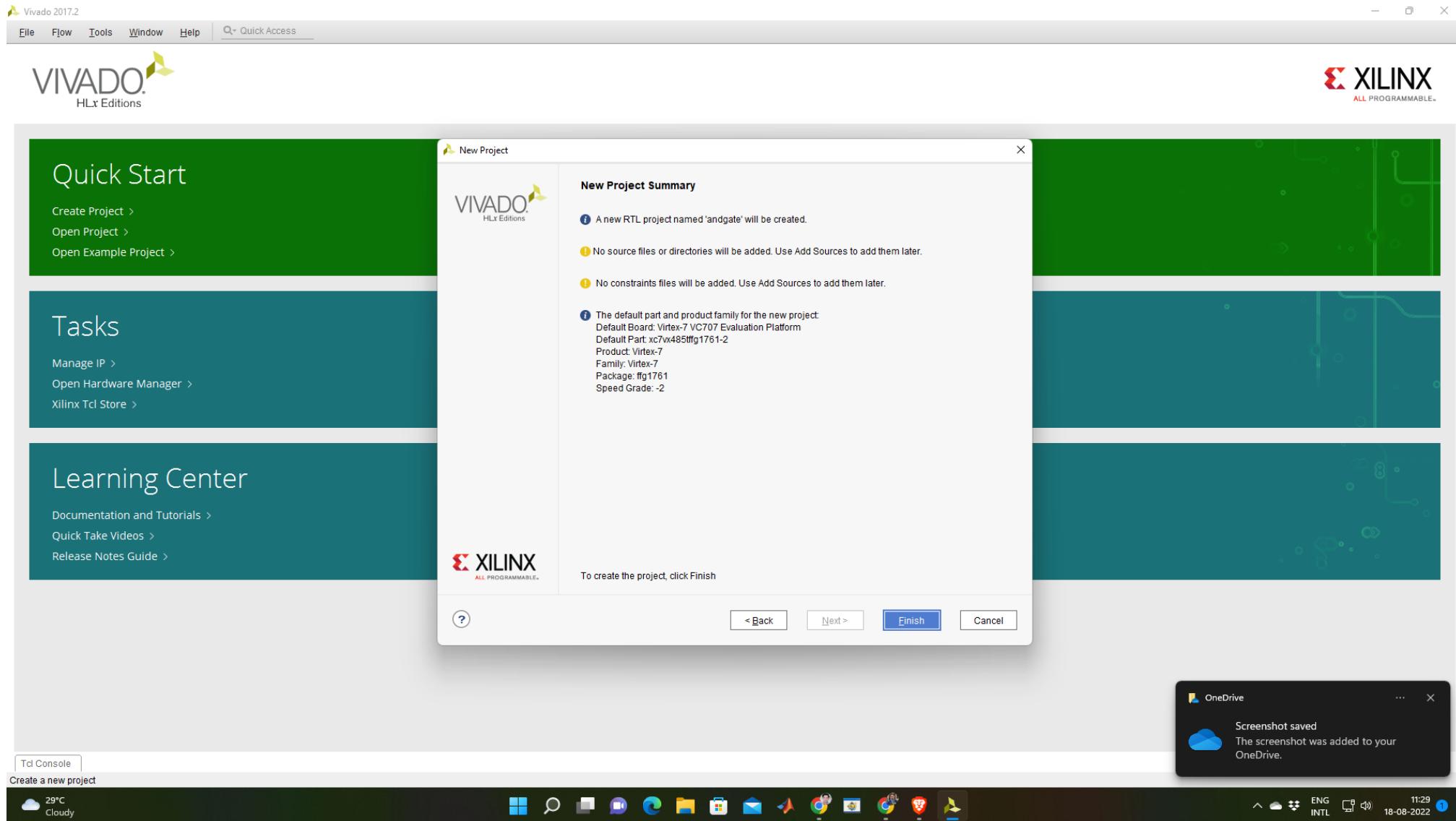












andgate - [C:/Users/PC0245/Desktop/Verilog_TA/andgate.xpr] - Vivado 2017.2

File Edit Flow Tools Window Layout View Help Quick Access Ready Default Layout

PROJECT MANAGER - andgate

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Hierarchy Libraries Compile Order

Properties

Display name: Virtex-7 VC707 Evaluation Platform
 Board part name: xilinx.com:vc707:part0:1.3
 Connectors:
 Repository path: C:/Xilinx/Vivado/2017.2/data/boards/board_files
 URL: www.xilinx.com/vc707
 Board overview: Virtex-7 VC707 Evaluation Platform

Select an object to see properties

Project Summary

Settings Edit

Project name: andgate
 Project location: C:/Users/PC0245/Desktop/Verilog_TA/andgate
 Product family: Virtex-7
 Project part: Virtex-7 VC707 Evaluation Platform (xc7vx485tffg1761-2)
 Top module name: Not defined
 Target language: Verilog
 Simulator language: Verilog

Board Part



Display name: Virtex-7 VC707 Evaluation Platform
 Board part name: xilinx.com:vc707:part0:1.3
 Connectors:
 Repository path: C:/Xilinx/Vivado/2017.2/data/boards/board_files
 URL: www.xilinx.com/vc707
 Board overview: Virtex-7 VC707 Evaluation Platform

Synthesis

Status: Not started
 Messages: No errors or warnings
 Part: xc7vx485tffg1761-2

Implementation

Status: Not started
 Messages: No errors or warnings
 Part: xc7vx485tffg1761-2

Tcl Console

Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1761-2	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1761-2	Default settings for Implementation

Specify and/or create source files to add to the project

Cloudy 29°C

Windows taskbar icons: File Explorer, Search, Task View, Edge, Mail, OneDrive, File Explorer, Google Chrome, File Explorer, File Explorer.

System tray: Battery, ENG INTL, 11:30, 18-08-2022, 1 battery icon.

andgate - [C:/Users/PC0245/Desktop/Verilog_TA/andgate.xpr] - Vivado 2017.2

File Edit Flow Tools Window Layout View Help Quick Access Ready Default Layout

Flow Navigator PROJECT MANAGER - andgate

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources Project Summary

Design Sources Constraints Simulation Sources sim_1

Project name: andgate

Add Sources

VIVADO HLx Editions

Add Sources

This guides you through the process of adding and creating sources for your project

Add or create constraints

Add or create design sources

Add or create simulation sources

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

XILINX ALL PROGRAMMABLE

Tcl Console Messages Log Reports

Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMs URAM DSP Start Elapsed Strategy Part Description

synth_1	constrs_1	Not started												Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tfg1761-2	Vivado Synthesis Defaults
impl_1	constrs_1	Not started												Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tfg1761-2	Default settings for Implementation

OneDrive Screenshot saved The screenshot was added to your OneDrive.

Specify and/or create source files to add to the project

Cloudy 29°C

Windows Taskbar icons: File Explorer, Search, Task View, Edge, Mail, Photos, OneDrive, Google Chrome, Vivaldi, VLC, Steam, and others.

System tray: Battery, Network, Volume, Language (ENG INTL), Date (18-08-2022), Time (11:30).

andgate - [C:/Users/PC0245/Desktop/Verilog_TA/andgate.xpr] - Vivado 2017.2

File Edit Flow Tools Window Layout View Help Quick Access Ready Default Layout

PROJECT MANAGER - andgate

Sources

Design Sources
Constraints
Simulation Sources sim_1

Project Summary

Settings Edit Project name: andgate

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Add Files Add Directories Create File

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Not started
No errors or warnings
xc7vx485tfg1761-2

Tcl Console Messages Log Reports

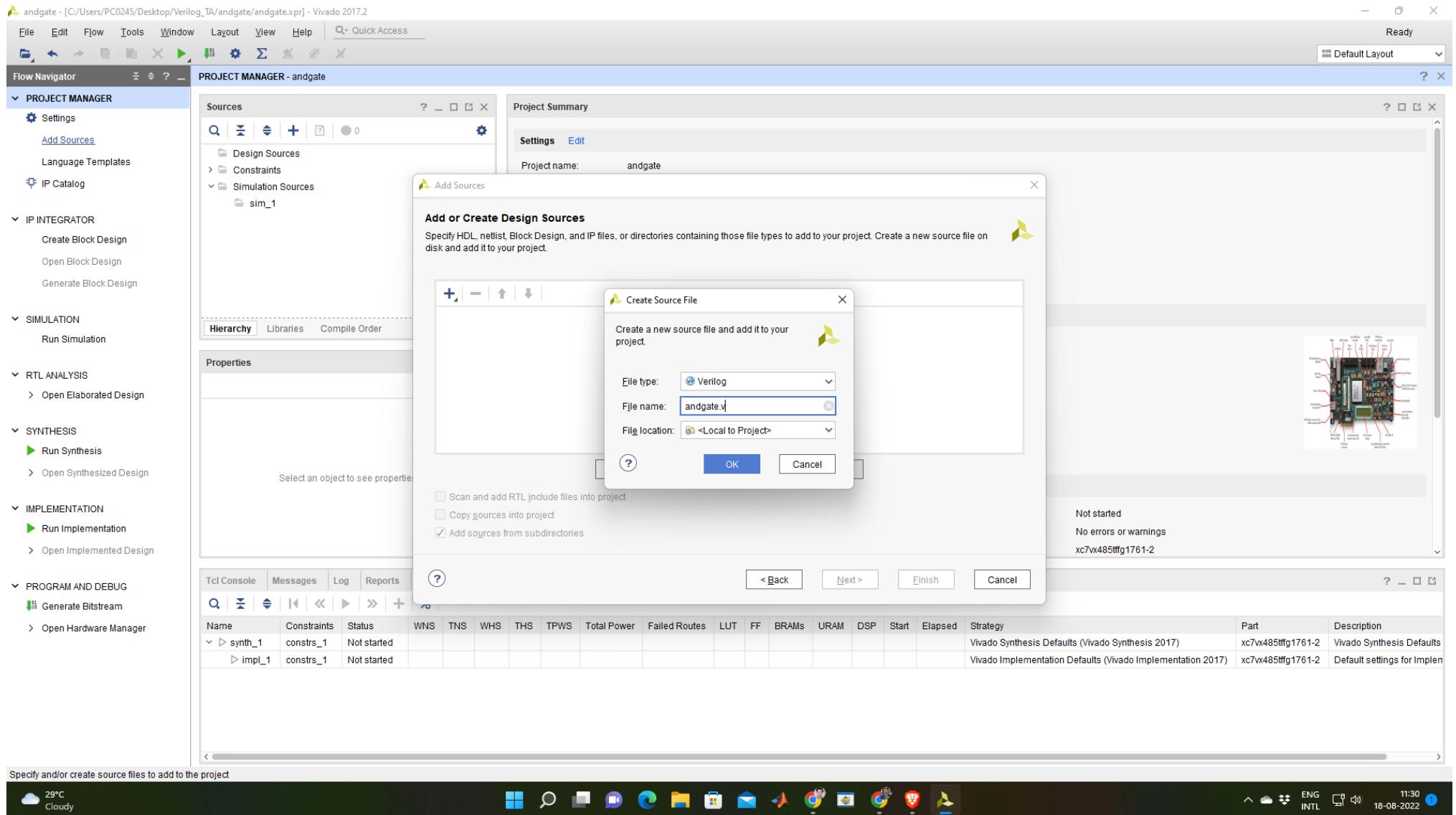
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMs URAM DSP Start Elapsed Strategy Part Description

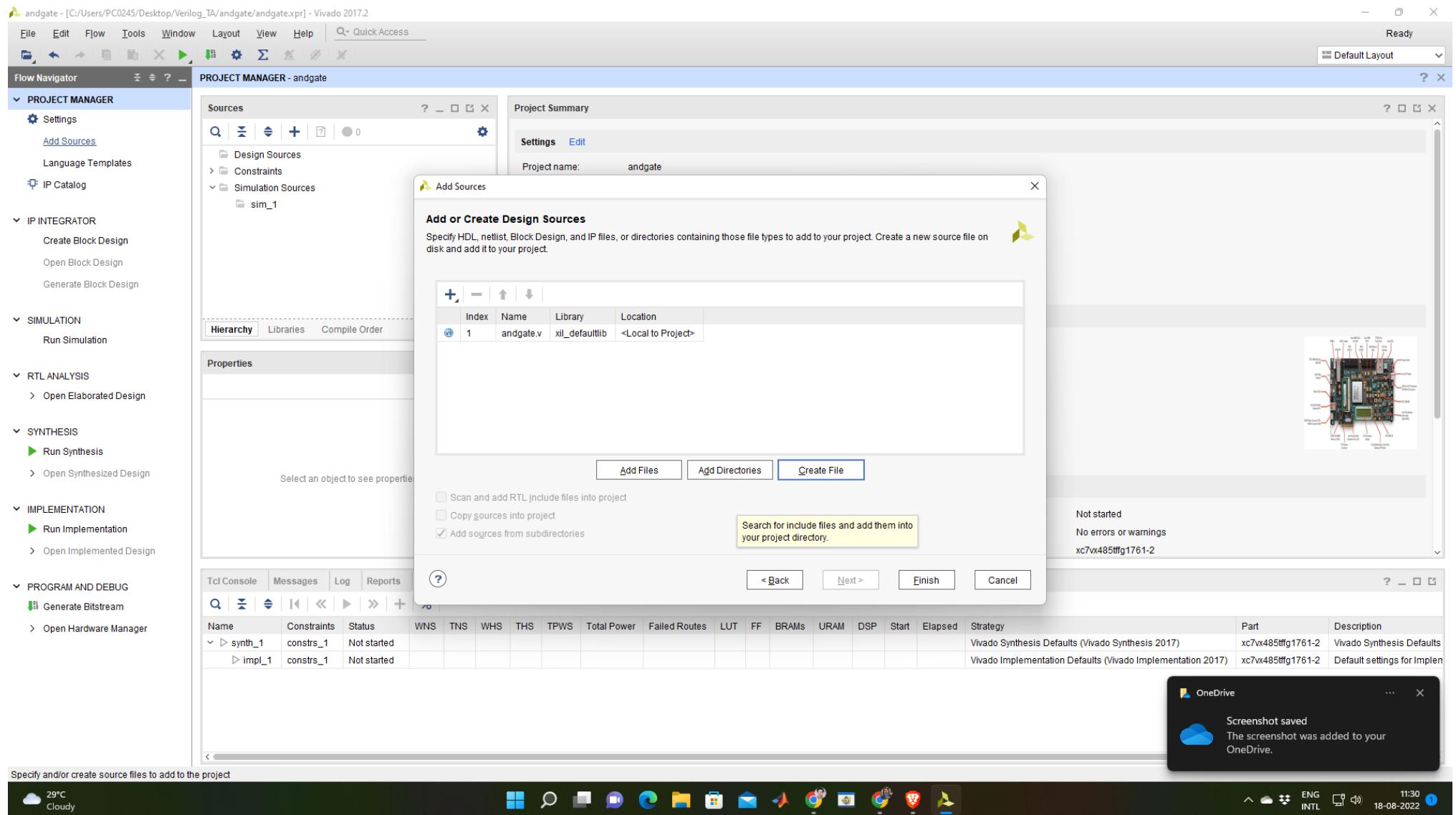
synth_1	constrs_1	Not started											Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tfg1761-2	Vivado Synthesis Defaults
impl_1	constrs_1	Not started											Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tfg1761-2	Default settings for Implementation

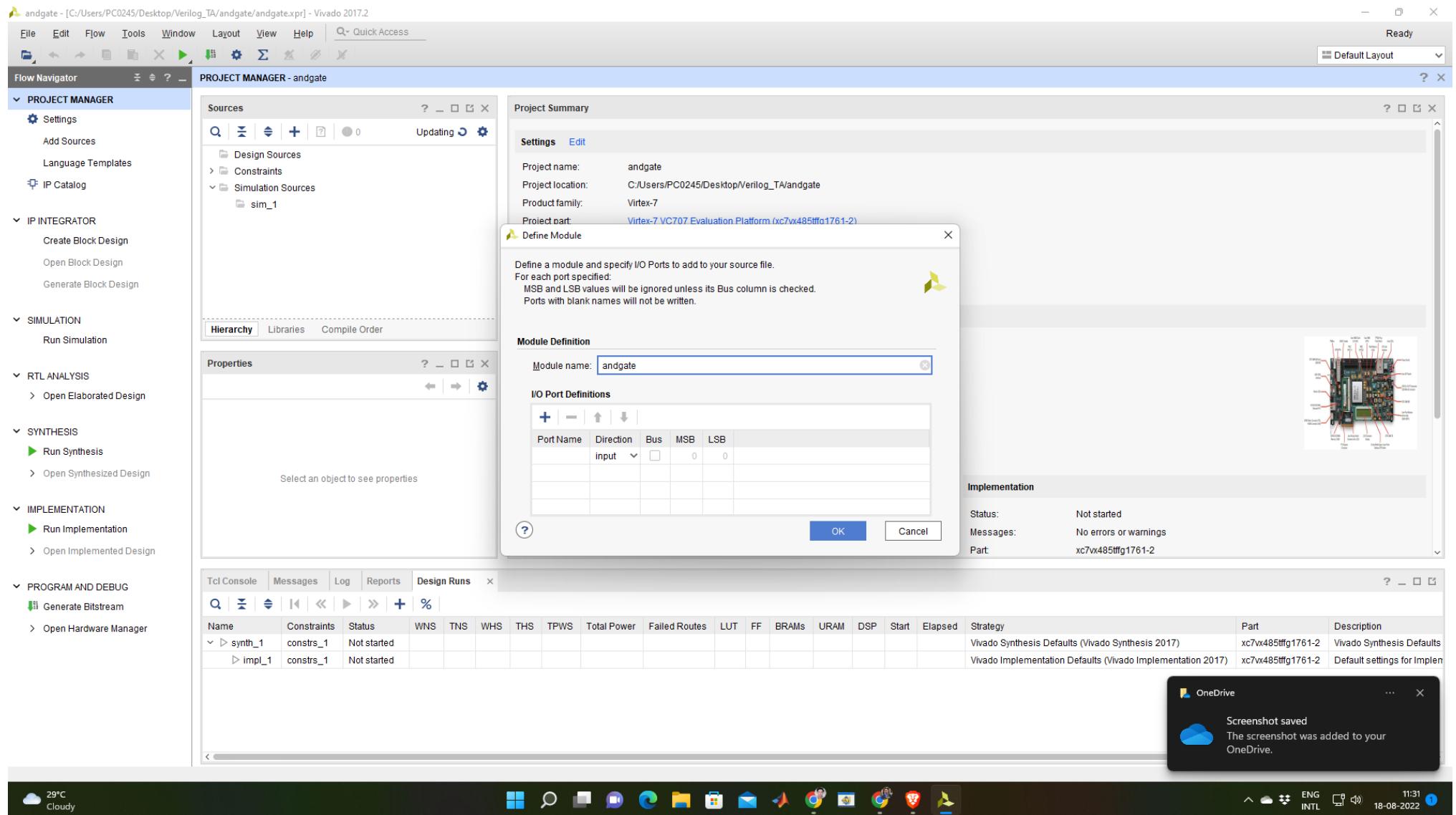
Specify and/or create source files to add to the project

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11:30 18-08-2022 ENG INTL







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File Edit Flow Tools Window Layout View Help Quick Access Ready Default Layout

PROJECT MANAGER - andgate

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Project Summary

Settings Edit

Project name: andgate
 Project location: C:/Users/PC0245/Desktop/Verilog_TA/andgate
 Product family: Virtex-7
 Project part: Virtex-7 VC707 Evaluation Platform (xc7vx485tffg1761-2)

Define Module

Module name:
 I/O Port Definition

The module definition has not been changed.
 Are you sure you want to use these values?

Yes No

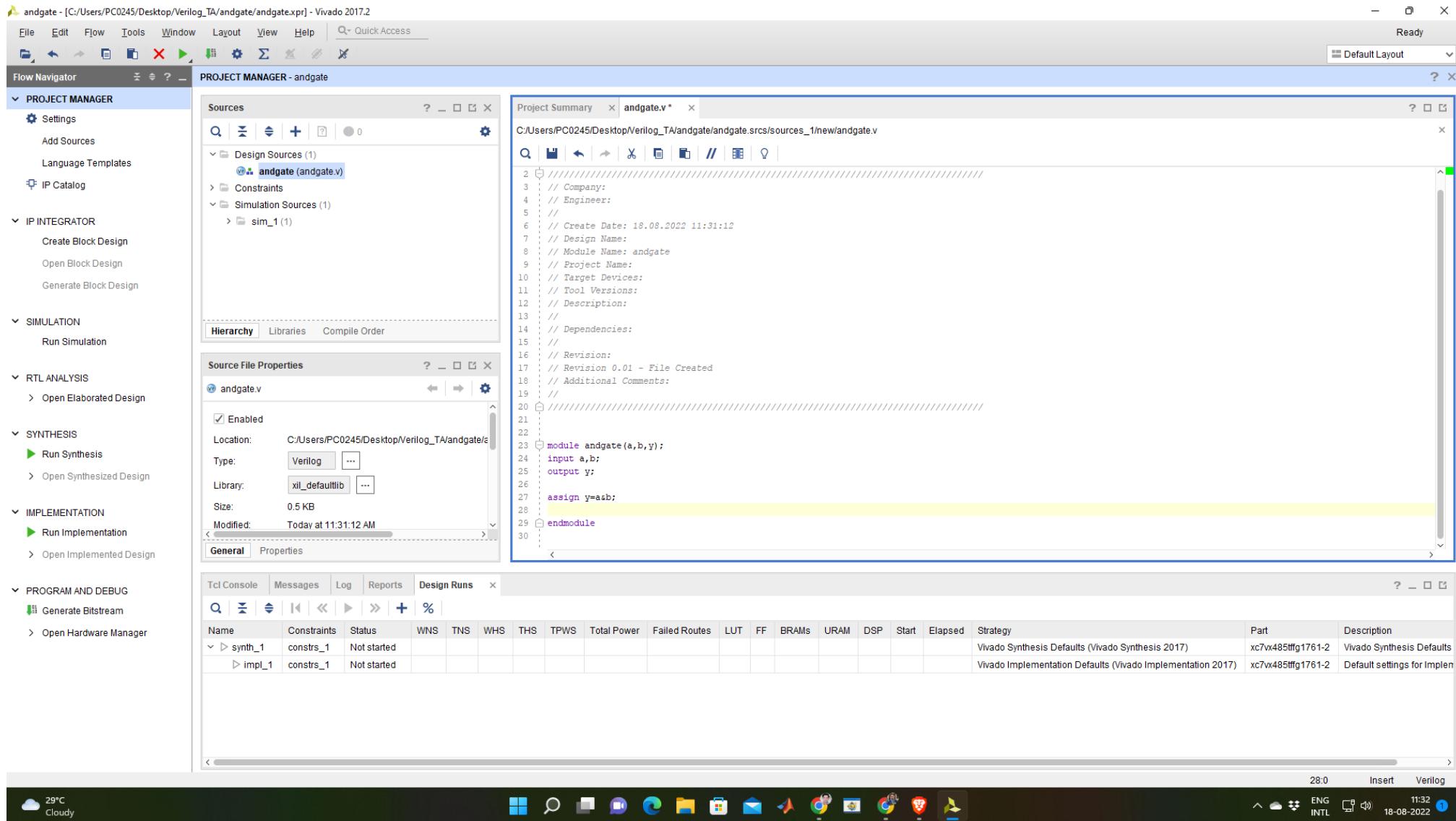
Implementation

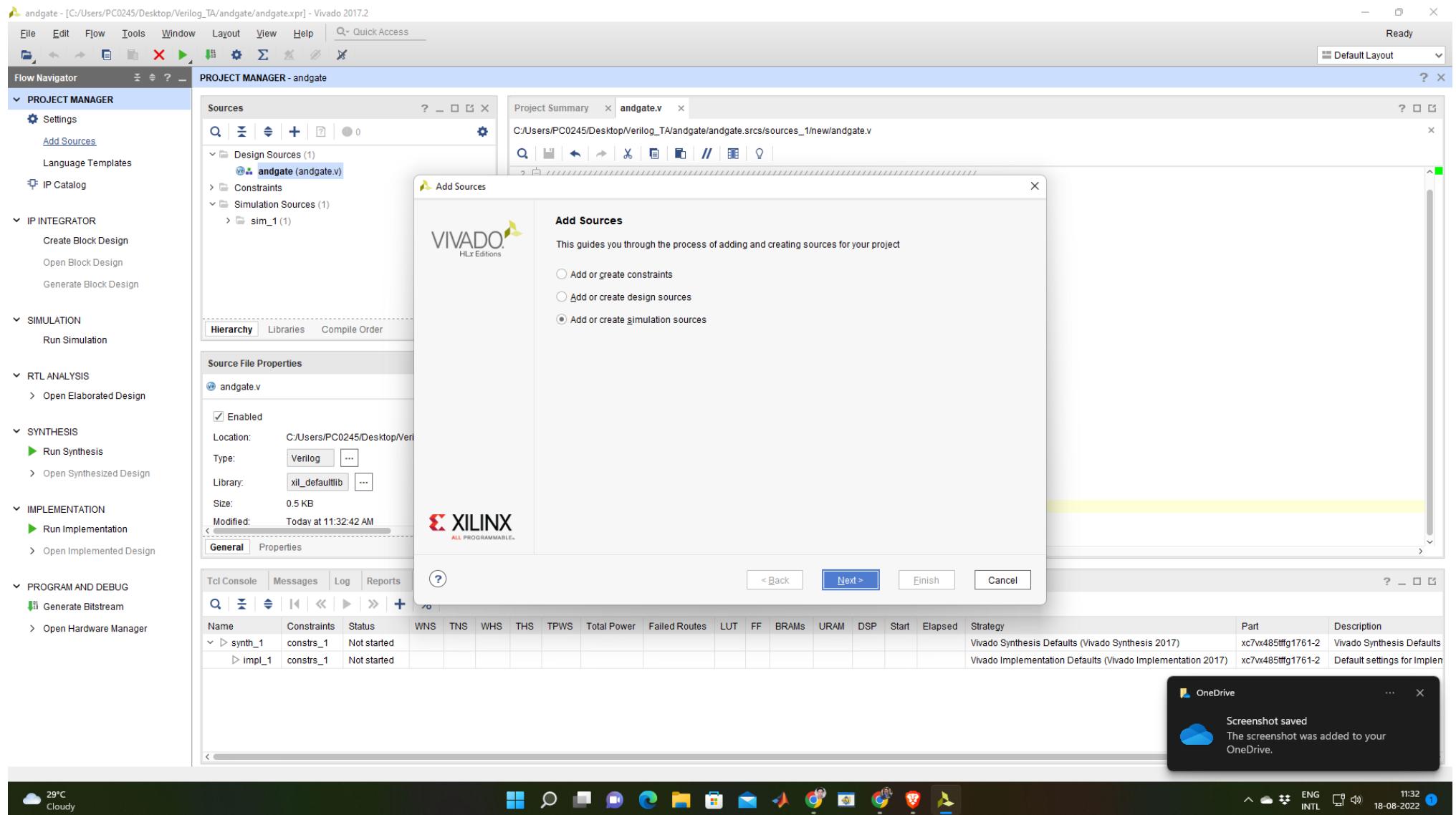
Status: Not started
 Messages: No errors or warnings
 Part: xc7vx485tffg1761-2

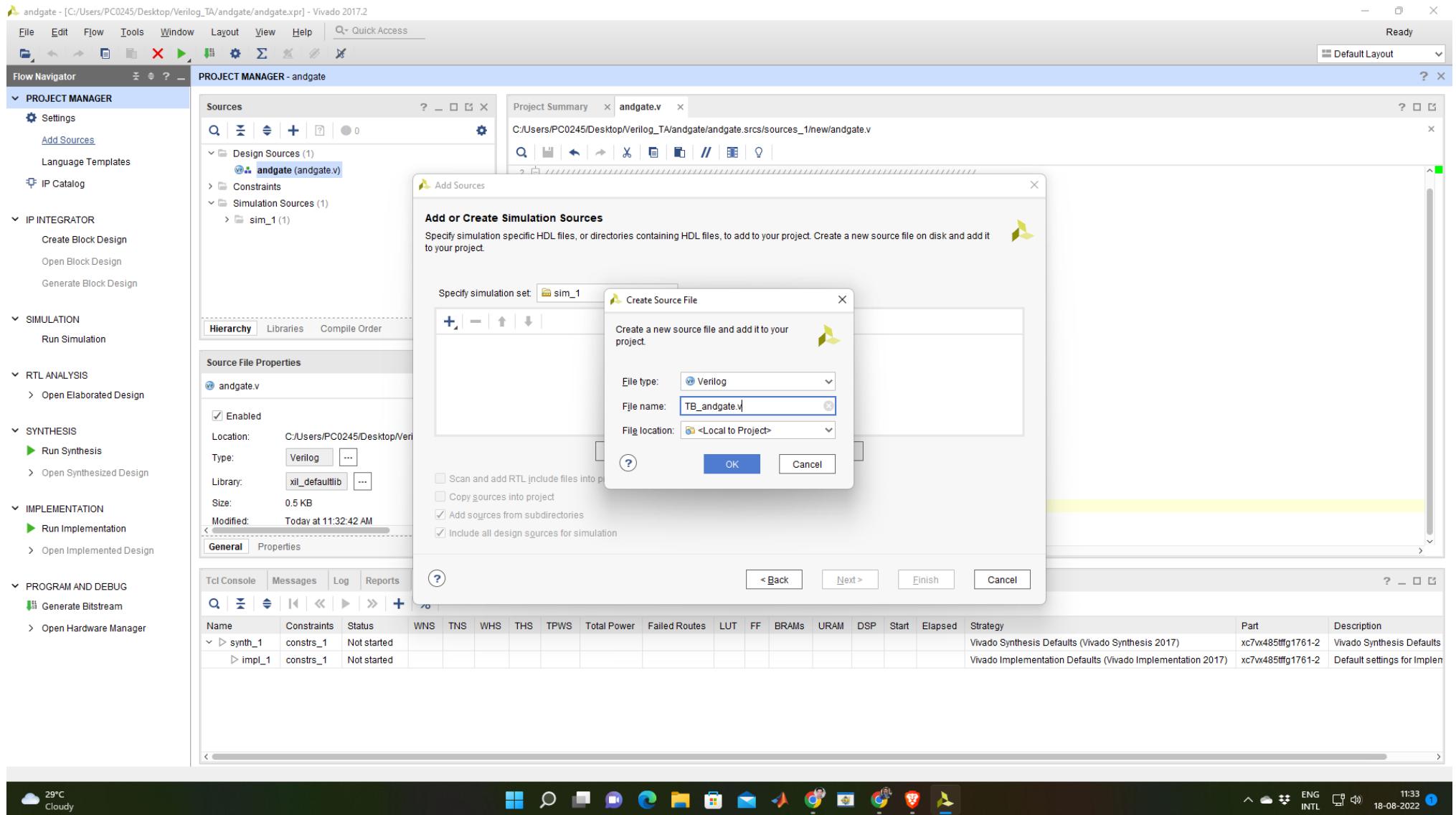
Design Runs

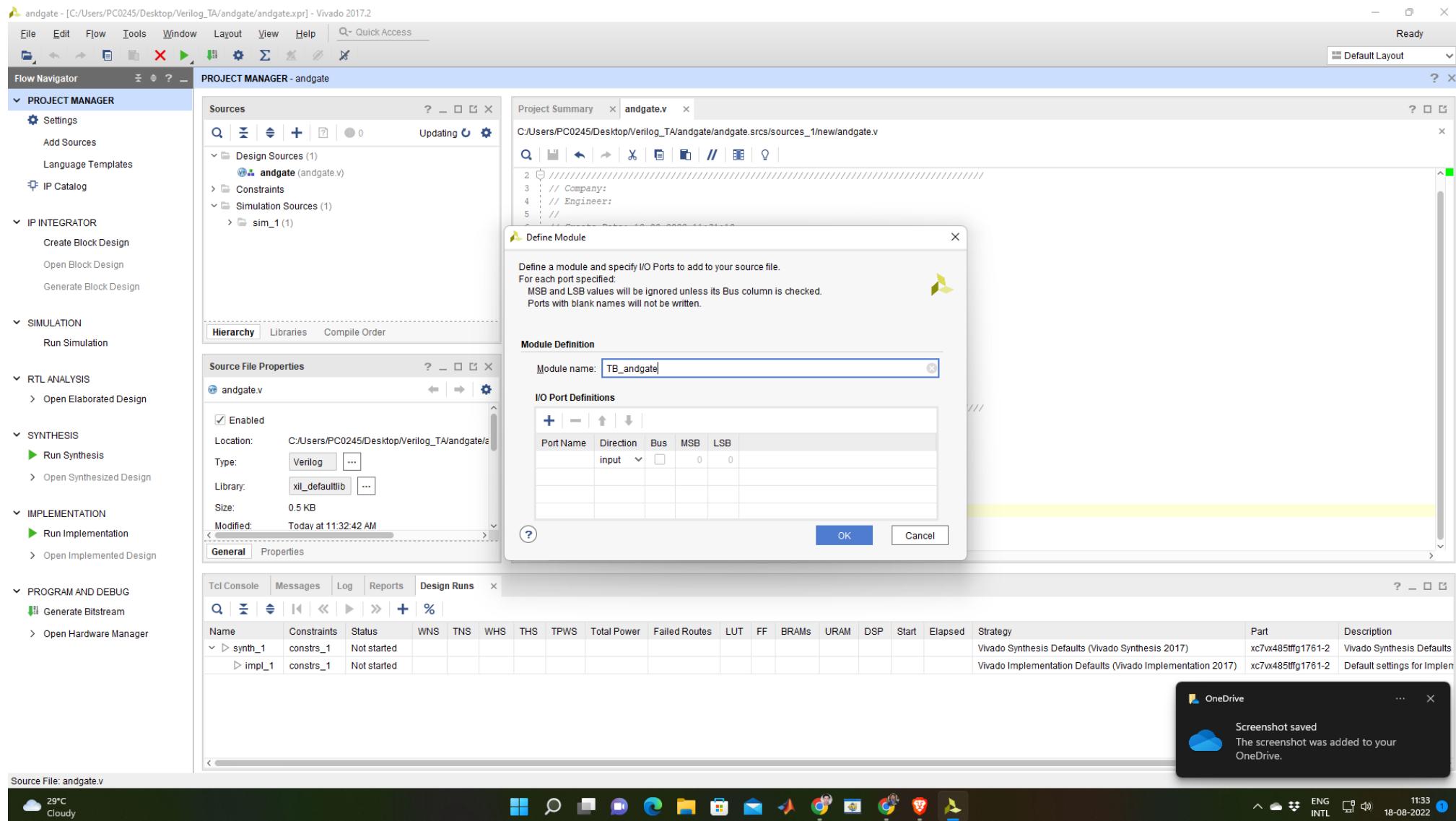
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tffg1761-2	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tffg1761-2	Default settings for Implementation

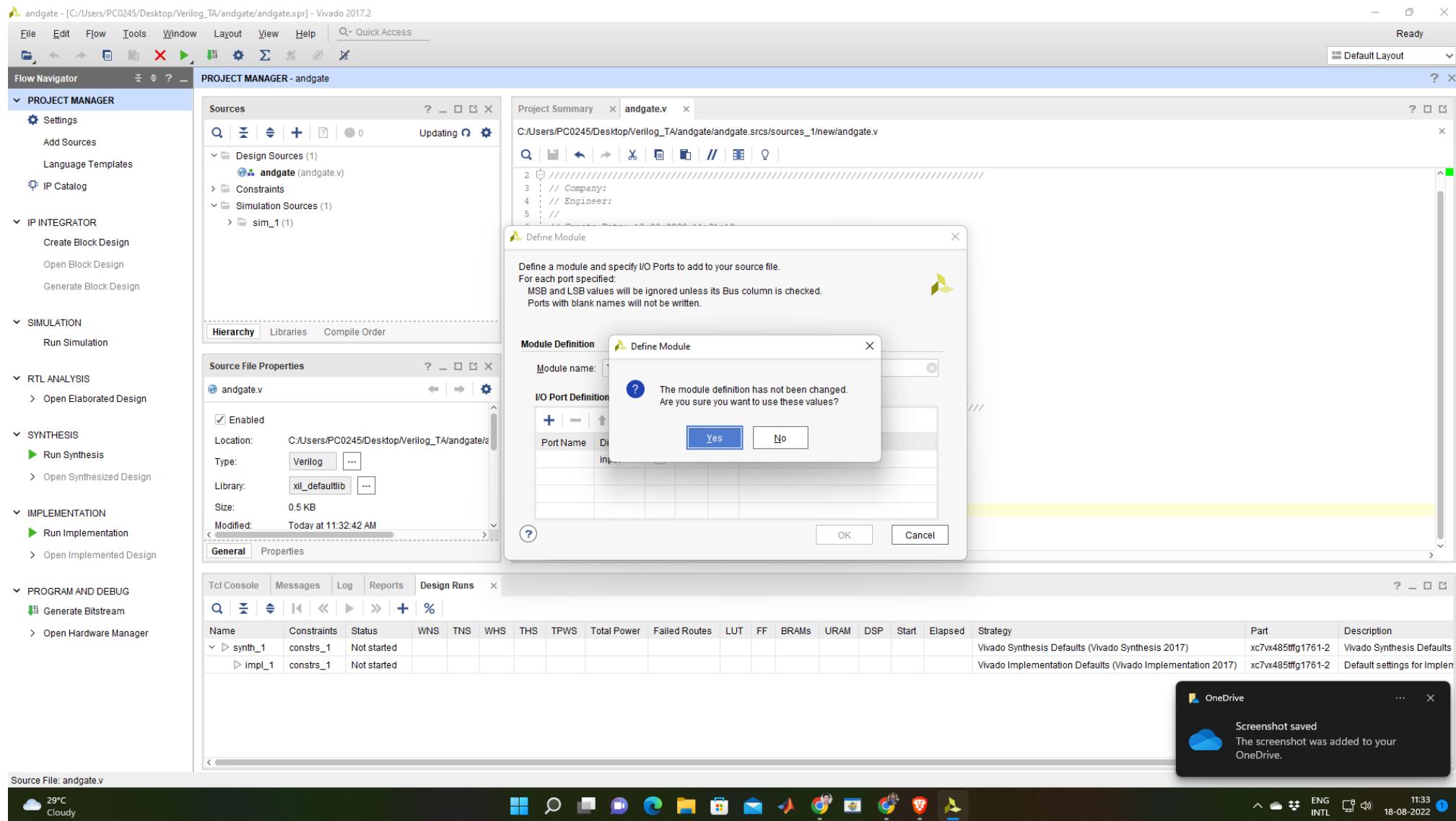
Cloudy 29°C 11:31 18-08-2022 ENG INTL

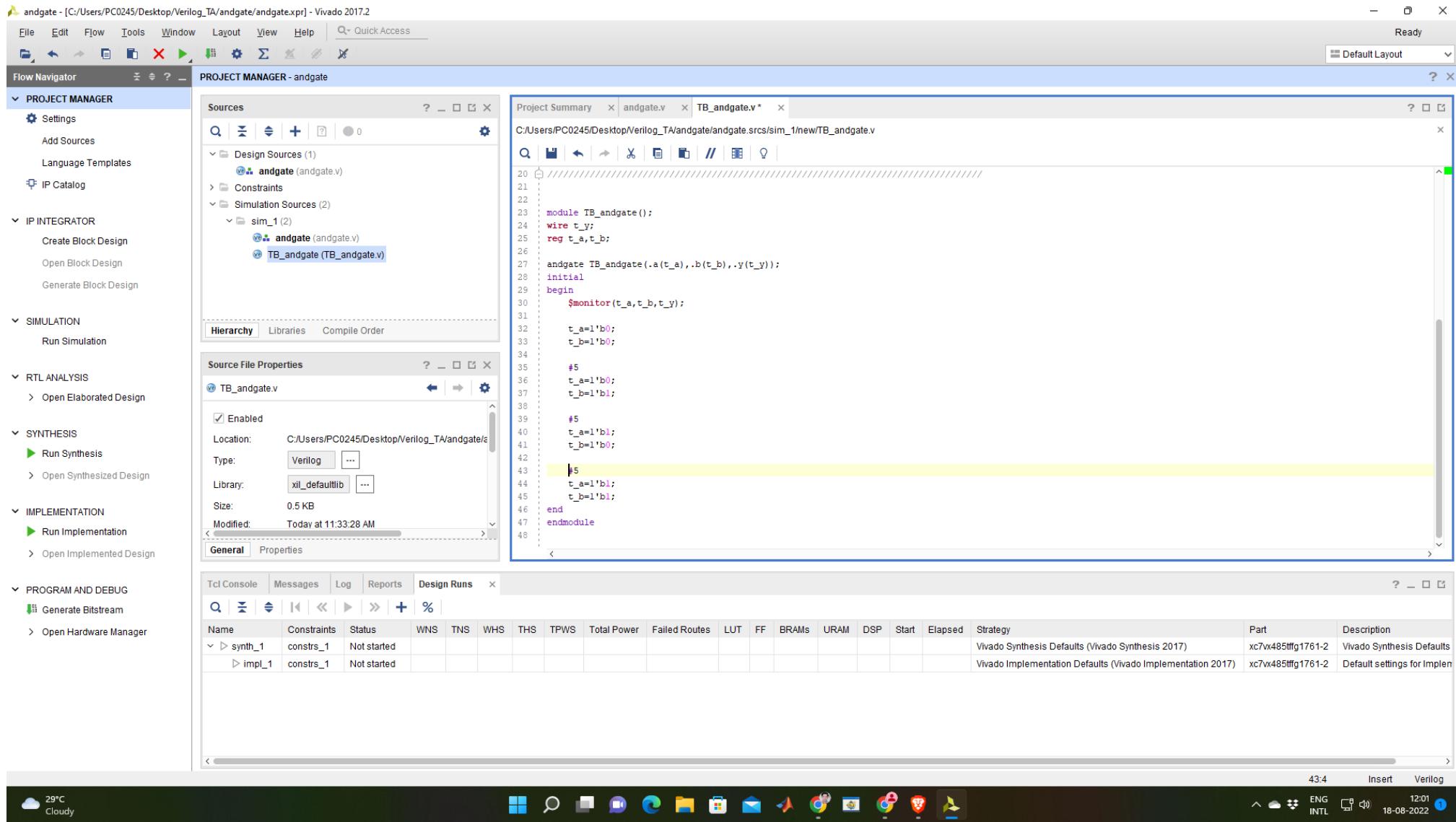


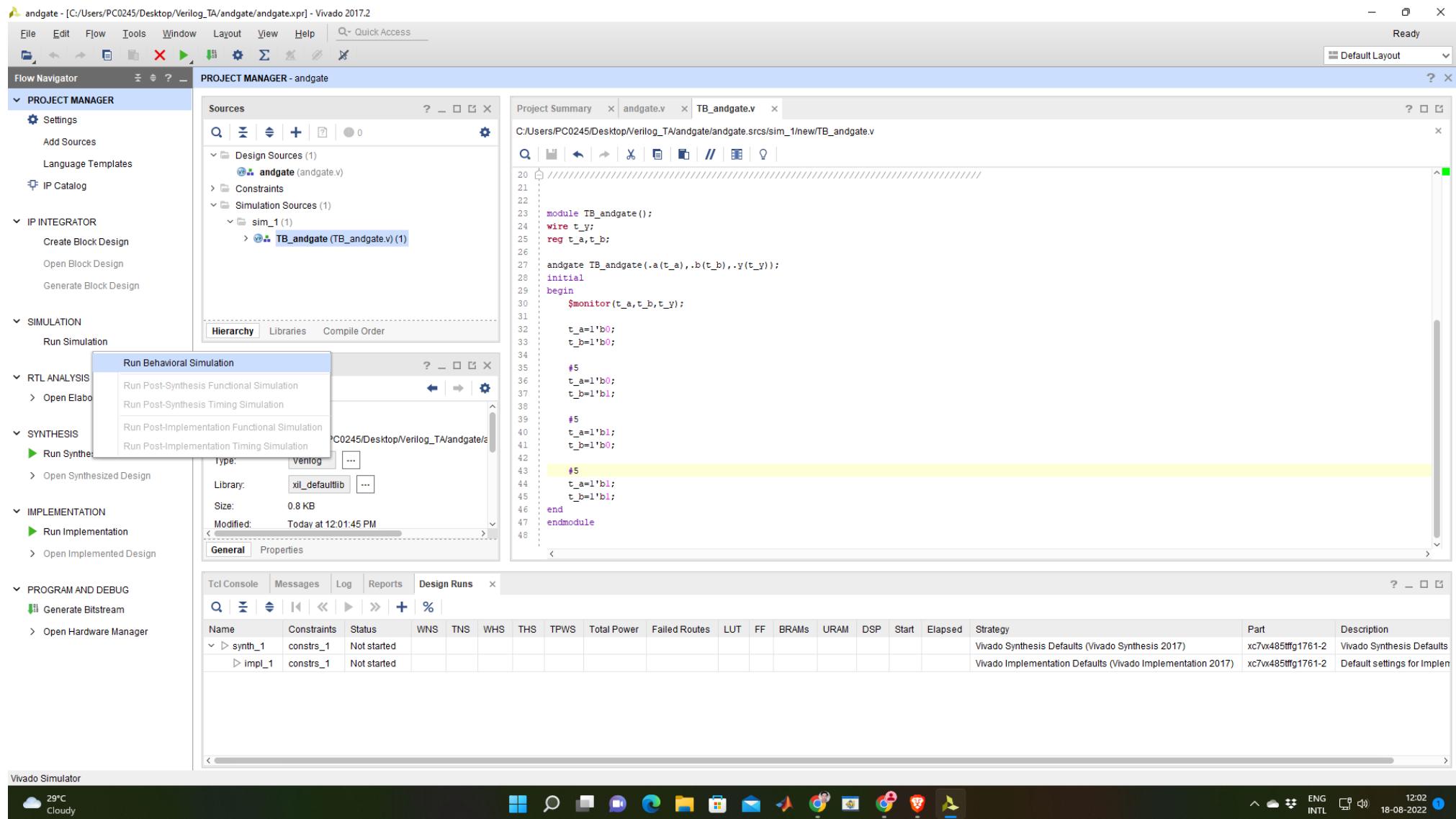


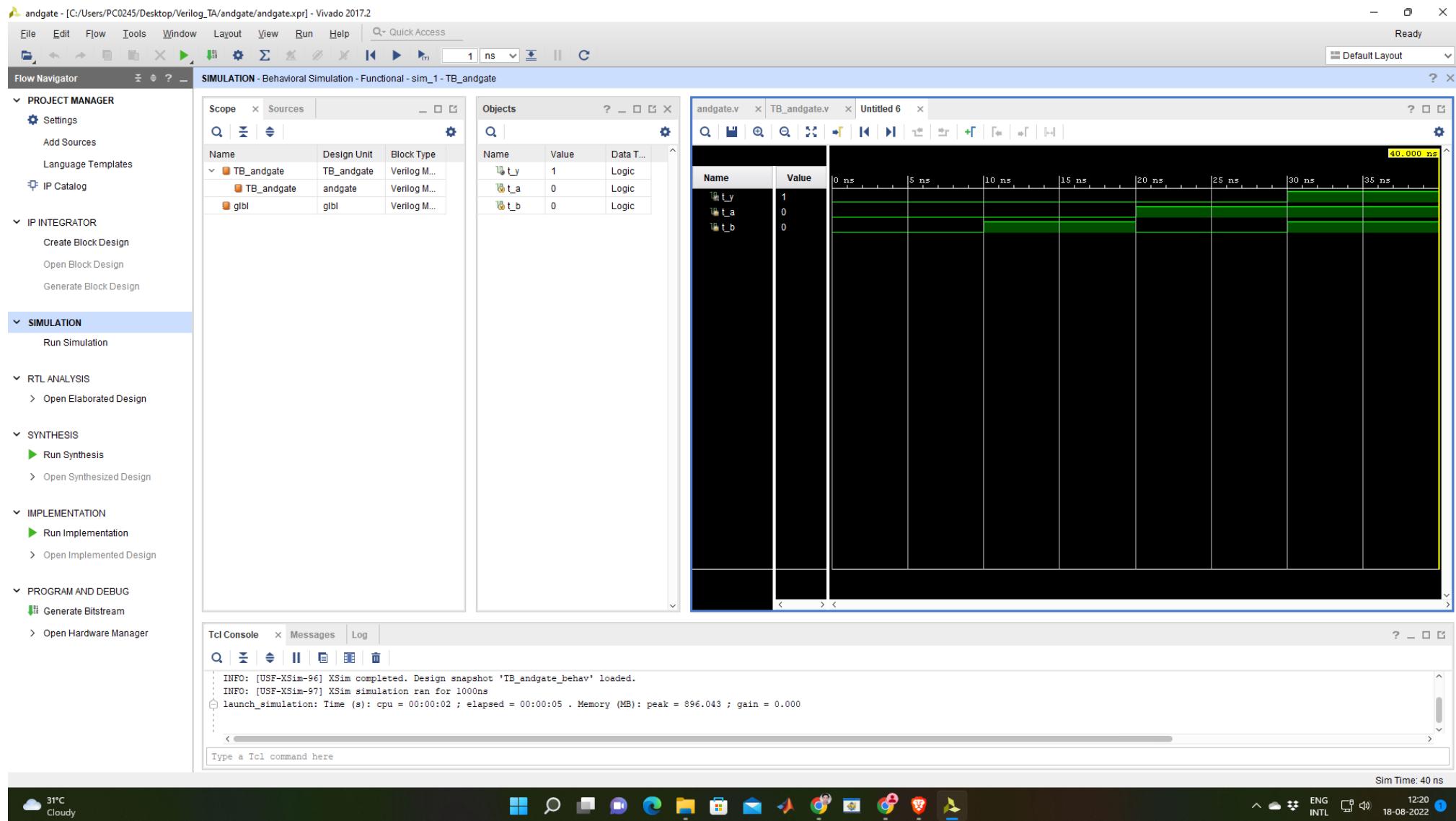












andgate - [C:/Users/PC0245/Desktop/Verilog_TA/andgate.xpr] - Vivado 2017.2

Synthesis Failed

Default Layout

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

ELABORATED DESIGN - xc7vx485tfg1761-2 (active)

Project Summary | Schematic | andgate.v | TB_andgate.v

1 Cell | 3 I/O Ports | 3 Nets

andgate

Nets (3)

Leaf Cells (1)

Simulation Scope Properties

Select an object to see properties

Tcl Console | Messages | Log | Reports | Design Runs

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Strategy	Part	Description
synth_1	constrs_1	synth_design ERROR													8/...	00:00:00	Vivado Synthesis Defaults (Vivado Synthesis 2017)	xc7vx485tfg1761-2	Vivado Synthes...
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2017)	xc7vx485tfg1761-2	Default settings

31°C Cloudy

12:22 18-08-2022