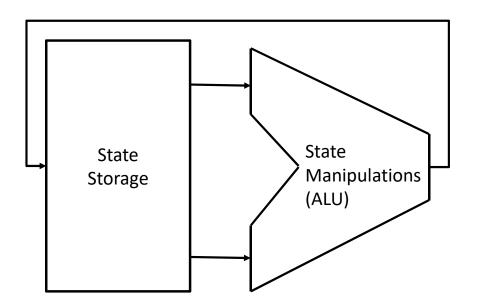
Finite State Machines

State – the central concept of computing

How do we generate control signals for circuits? Finite State Machines

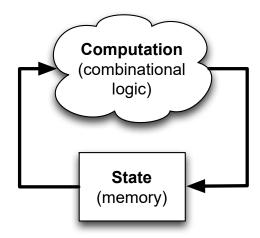


Today's lecture

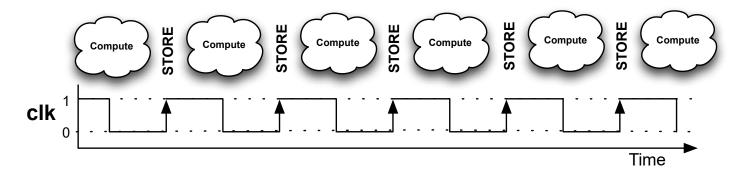
- Goal: Build a sequential circuit from a state diagram
 - Step 0: Problem specification
 - Step 1: Build the state diagram
 - Setp 2: Build the state table
 - Step 3: Build the sequential circuit using D flip-flops
- Timing diagram
- Another example: Sequence recognizer

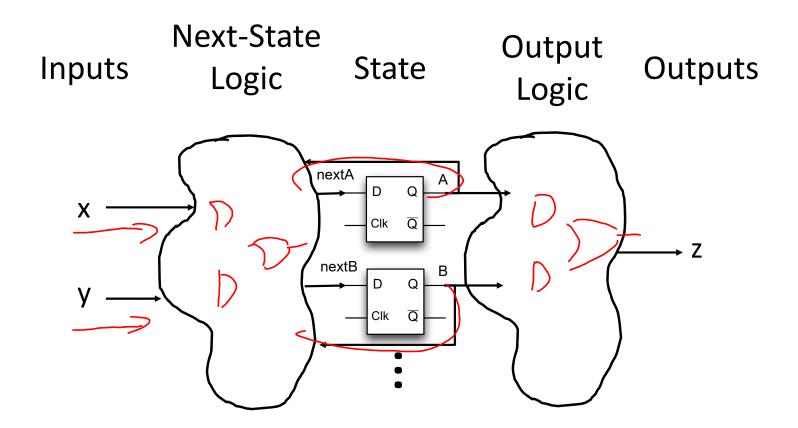
If a combinational logic circuit is an implementation of a Boolean function, then a sequential logic circuit can be considered an implementation of a finite state machine.

Synchronous Design, reminder



• Alternate between computation and updating state.





Step 0: Problem Specification

- We have a candy machine that dispenses candies that cost 15-cents
 - Accepts
 - nickels (5-cents)
 - dimes (10-cents)
 - Dispenses a candy if the balance is ≥ 15-cents
 - When the customer overpays
 - the machine does not return change, but
 - keeps the balance for future transactions



Step 1: Build the State Diagram

Inputs

d=1, iff dime is inserted of nickel inserted of nickel inserted of nickel in the nickel inserted of not possible of the candy should be dispersed capally capally

State identification

0¢,5€,10¢,15¢,20¢

Step 1: Build the State Diagram

Outputs: candy or candy'





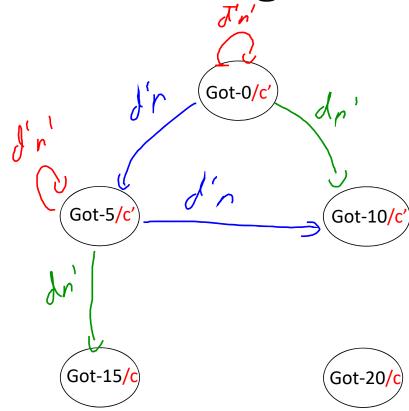






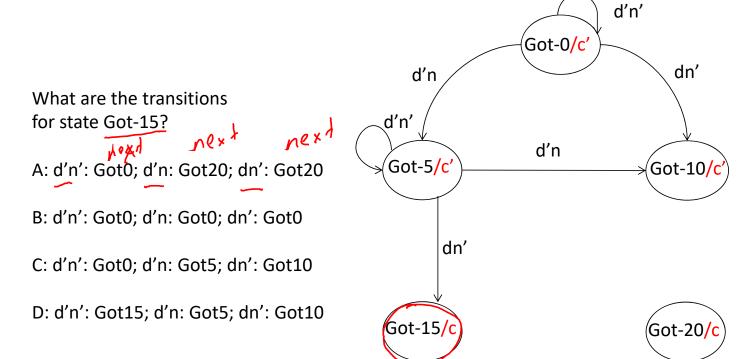
- a) candy
- b) candy'

Step 1: Build the State Diagram



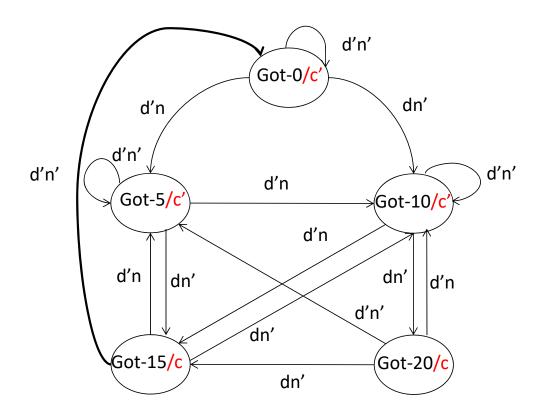
Inputs: d'n', d'n, dn'

Step 1: Build the State Diagram iclicker.

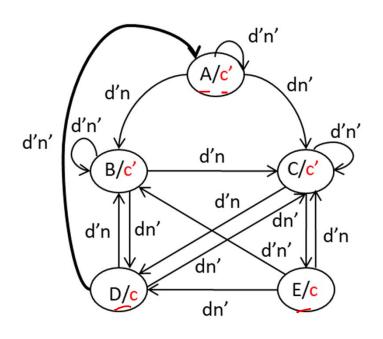


Inputs: d'n', d'n, dn'

Final State Diagram



Step 2: Build a State Table

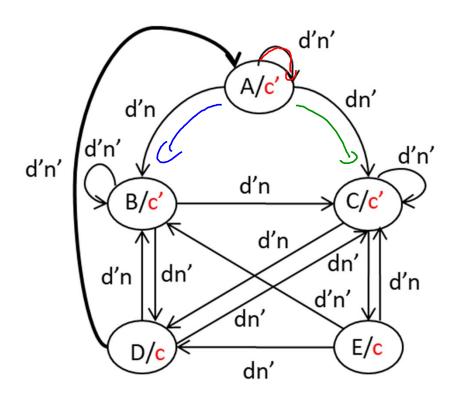


| Current State | Output candy |
|------------------|--------------|
| А | 0 |
| В | 0 |
| С | 0 |
| D | 1 |
| E | 1 |

(andy = D + E

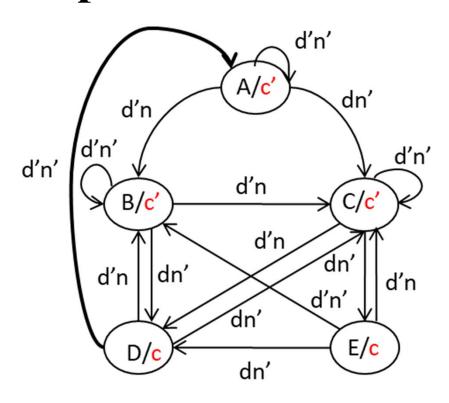
In a 'Moore machine', the outputs are a function only of the current state.

Step 2: Build a Next-State Table iclicker.



| Current State | Input | Next State | | | | | |
|------------------|------------|---------------|---|---|---|---|---|
| А | ď'n' | A | | | | | |
| Α | <u>d'n</u> | B | | | | | |
| Α | dn' | \ | A | В | С | D | E |
| В | d'n' | | Α | В | В | В | С |
| В | ďn | | В | С | С | D | D |
| В | dn' | | С | D | Е | Α | Е |
| С | d'n' | | | | | | |
| С | ďn | | | | | | |
| С | dn' | | | | | | |
| D | d'n' | | | | | | |
| D | ďn | | | | | | |
| D | dn' | | | | | | |
| E | d'n' | | | | | | |
| E | ďn | | | | | | |
| E | dn' | | | | | | |

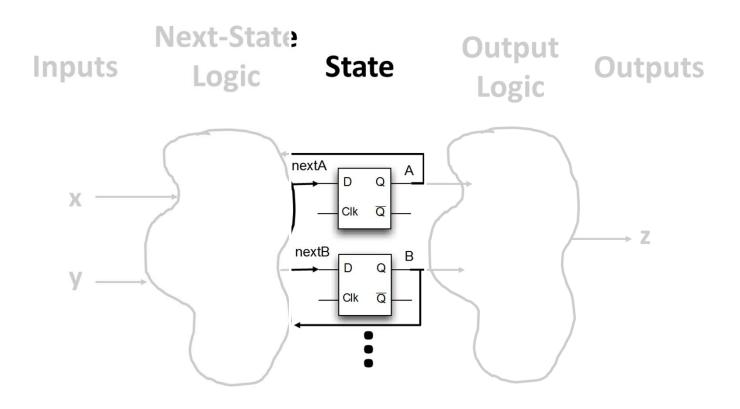
Step 2: Build a Next-State Table



Why do we need sequential logic to build this circuit?

| Current State | Input | Next State |
|------------------|-------|---------------|
| А | d'n' | Α |
| А | ďn | В |
| А | dn' | С |
| В | d'n' | В |
| В | ďn | С |
| В | dn' | D |
| С | d'n' | С |
| С | ďn | D |
| С | dn' | E |
| D | d'n' | Α |
| D | ďn | В |
| D | dn' | С |
| E | d'n' | В |
| E | ďn | С |
| E | dn' | D |

Step 3: Build Sequential Circuit



Step 3: Build Sequential Circuit (State)

| Current State | Input | Next State |
|------------------|-------|---------------|
| А | ďn' | Α |
| А | d'n | В |
| А | dn' | С |
| В | ďn' | В |
| В | d'n | С |
| В | dn' | D |
| С | ďn' | С |
| С | d'n | D |
| С | dn' | E |
| D | ďn' | А |
| D | d'n | В |
| D | dn' | С |
| E | ďn' | В |
| E | ďn | С |
| E | dn' | D |

State Encoding:

5 states: How many bits?

Step 3: Build Sequential Circuit (State)

| Current State | Input | Next State |
|------------------|-------|---------------|
| А | d'n' | Α |
| А | d'n | В |
| А | dn' | С |
| В | d'n' | В |
| В | d'n | С |
| В | dn' | D |
| С | d'n' | С |
| С | d'n | D |
| С | dn' | E |
| D | d'n' | Α |
| D | d'n | В |
| D | dn' | С |
| E | d'n' | В |
| E | ďn | С |
| E | dn' | D |

One hot encoding

ABCDE

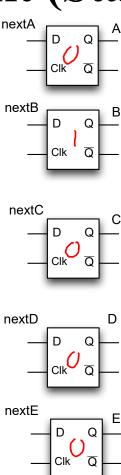
State A = 10000

State B = 01000

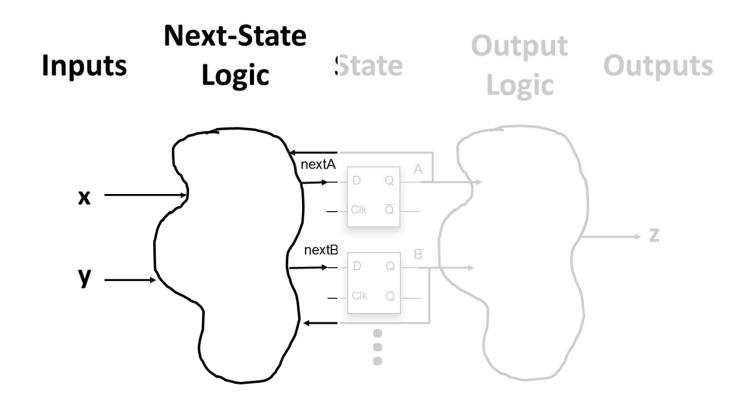
State C = 00100

State D = 00010

State E = 00001



Step 3: Build Sequential Circuit

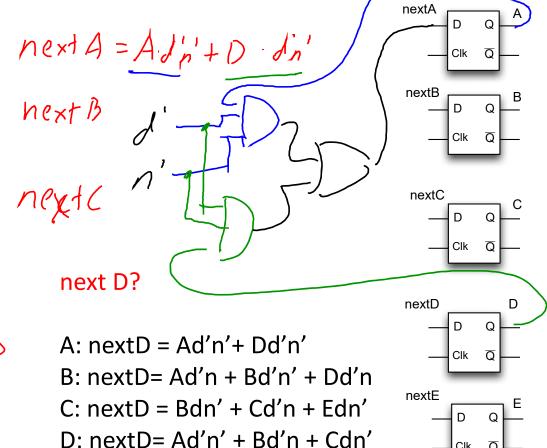


Step 3: Build Sequential Circuit (Next-State

E: nextD = 1

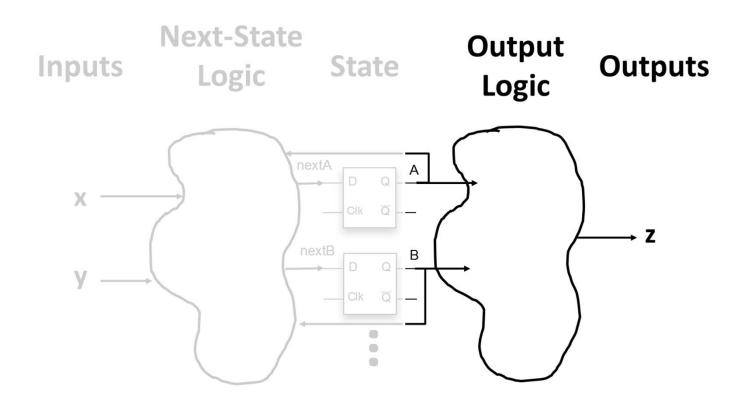
Logic)

| Input | Next State |
|-------|--|
| d'n' | A |
| ďn | В |
| dn' | С |
| d'n' | В |
| ďn | С |
| dn' | D |
| d'n' | С |
| ďn | D |
| dn' | E |
| ď'n' | Α |
| ďn | В |
| dn' | С |
| d'n' | В |
| ďn | С |
| dn' | D |
| | d'n' d'n dn' d'n' d'n dn' d'n' d'n dn' d'n' d'n' d'n dn' |



iclicker.

Step 3: Build Sequential Circuit



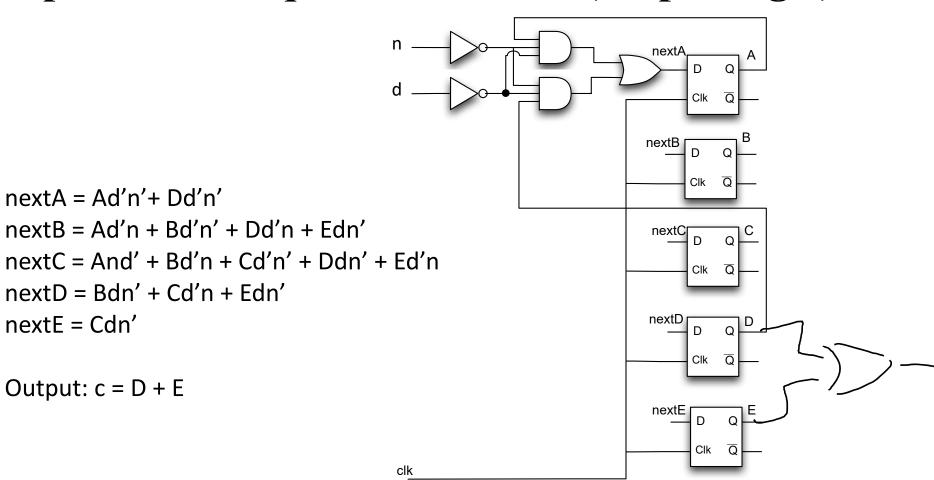
Step 3: Build Sequential Circuit (output logic)

| Current State | Input | Next State | Output |
|------------------|-------|---------------|--------|
| Α | d'n' | Α | 0 |
| А | d'n | В | 0 |
| А | dn' | С | 0 |
| В | d'n' | В | 0 |
| В | ďn | С | 0 |
| В | dn' | D | 0 |
| С | d'n' | С | 0 |
| С | ďn | D | 0 |
| С | dn' | E | 0 |
| D | d'n' | А | 1 |
| D | ďn | В | 1 |
| D | dn' | С | 1 |
| E | d'n' | В | 1 |
| E | d'n | С | 1 |
| E | dn' | D | 1 |

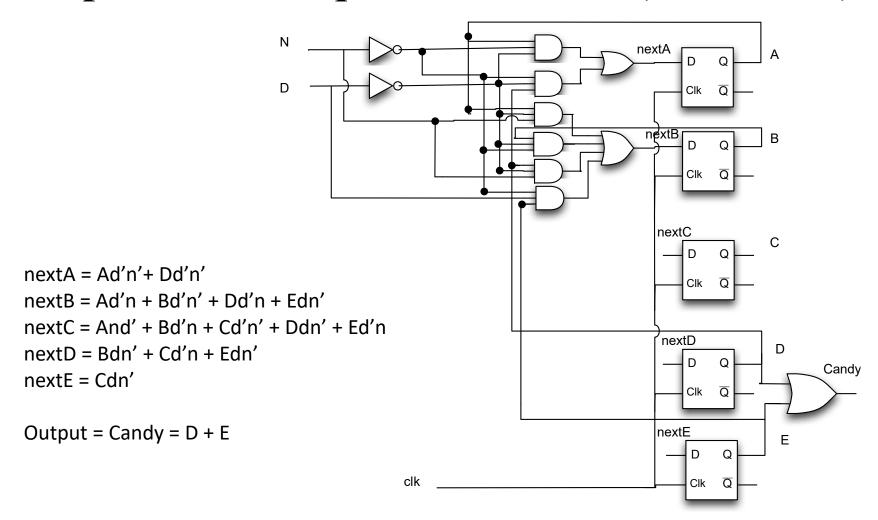
nextA = Ad'n'+ Dd'n'
nextB = Ad'n + Bd'n' + Dd'n + Edn'
nextC = And' + Bd'n + Cd'n' + Ddn' + Ed'n
nextD = Bdn' + Cd'n + Edn'
nextE = Cdn'

Output: Candy = D + E

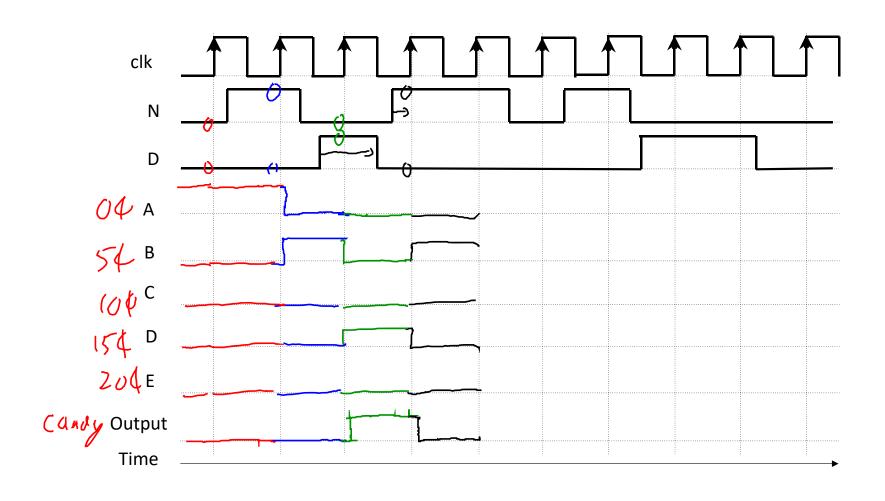
Step 3: Build Sequential Circuit (output logic)



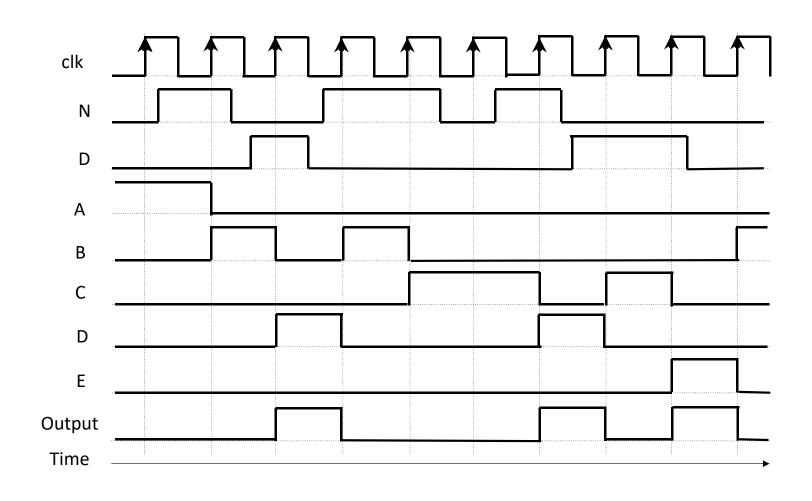
Step 3: Build Sequential Circuit ("finished")



Timing Diagram (update state on clock edges)



Timing Diagram



Another example: Sequence recognizer

- A sequence recognizer is a special kind of sequential circuit that looks for a special bit pattern in some input.
- The recognizer circuit has one input, X.
- There is one output, Z, which is 1 when the desired pattern is found.
- Our example will detect the bit pattern "1001":

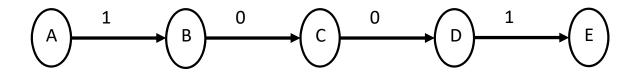
Inputs: 11100110100100110...

Outputs: 0000001000010010...

Here, one input and one output bit appear every clock cycle.

This requires a sequential circuit because the circuit has to "remember" the inputs from previous clock cycles, in order to determine whether or not a match was found.

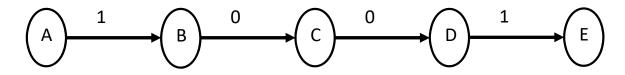
| State | Meaning |
|-------|--|
| Α | None of the desired pattern (1001) has been input yet. |
| В | We've already seen the first bit (1) of the desired pattern. |
| С | None of the desired pattern (1001) has been input yet. We've already seen the first bit (1) of the desired pattern. We've already seen the first two bits (10) of the desired pattern. |
| D | We've already seen the first three bits (100) of the desired pattern. |
| Е | We've seen the pattern (1001) |



| State | Meaning |
|-------|--|
| Α | None of the desired pattern (1001) has been input yet. We've already seen the first bit (1) of the desired pattern. We've already seen the first two bits (10) of the desired pattern. We've already seen the first three bits (100) of the desired pattern. |
| В | We've already seen the first bit (1) of the desired pattern. |
| С | We've already seen the first two bits (10) of the desired pattern. |
| D | We've already seen the first three bits (100) of the desired pattern. |
| Ε | We've seen the pattern (1001) |



• We need two outgoing arrows for each node, to account for the possibilities of X=0 and X=1.



Inputs: 11100110100100110...

Outputs: 0000001000010010...

Transitions for E:

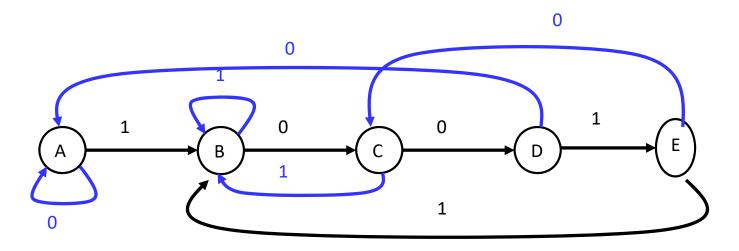
A: x=0-> A; x=1 -> B

B: x=0-> C; x=1 -> B

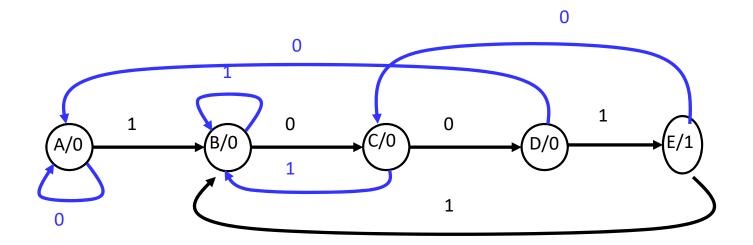
C: x=0-> B; x=1 -> A

D: x=0-> D; x=1 -> B

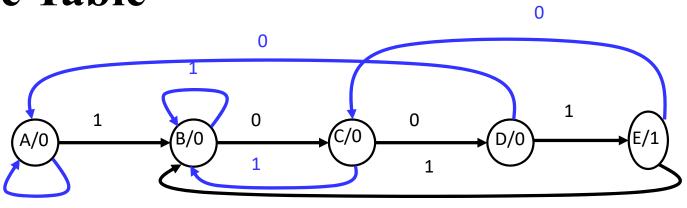
• We need *two* outgoing arrows for each node, to account for the possibilities of X=0 and X=1.



Need to determine the output

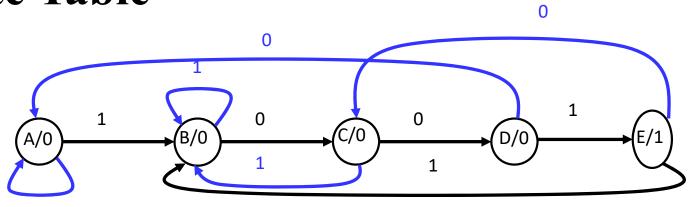


State Table



| Current | | Next | |
|---------|-------|-------|--------|
| State | Input | State | Output |
| A | 0 | A | 0 |
| A | 1 | В | 0 |
| В | 0 | С | 0 |
| В | 1 | В | 0 |
| C | 0 | D | 0 |
| C | 1 | В | 0 |
| D | 0 | Α | 0 |
| D | 1 | Е | 1 |
| Е | 0 | С | 0 |
| Е | 1 | В | 0 |

State Table



| Current | | Next | |
|---------|-------|-------|--------|
| State | Input | State | Output |
| Α | 0 | Α | 0 |
| A | 1 | В | 0 |
| В | 0 | С | 0 |
| В | 1 | В | 0 |
| С | 0 | D | 0 |
| C | 1 | В | 0 |
| D | 0 | Α | 0 |
| D | 1 | Е | 1 |
| Е | 0 | С | 0 |
| F | 1 | В | 0 |

Anext =
$$Ax' + Dx'$$

$$Bnext = Ax + Bx + Cx + Ex$$

$$Cnext = Bx' + Ex'$$

$$Dnext = Cx'$$

$$Enext = Dx$$