DEVENDRA KRISHNAKALVA

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PROFESSIONAL ABRIDGEMENT

Aspiring VLSI engineer with a strong foundation in digital design, RTL coding, and SoC architecture. Proficient in Verilog, FPGA, and ASIC design, with hands-on experience in advanced verification methodologies and simulation tools. Passionate about contributing to cutting-edge semiconductor technologies and driving innovation in the VLSI domain.

TECHNICAL SKILLS

Hardware Languages : Verilog HDL, VHDL, System Verilog,
VLSI Front End Tools : Verification : UVM, Functional Coverage, Testbench Dev,
Synthesis : Xilinx Vivado, Xilinx ISE (XST),
Simulation : QuestaSim, ModelSim, EDA Playground.
FPGA Development Boards : Spartan 3E, Virtex 7, Spartan 6.
Scripting Languages : Python.
Tools & Text Editors : GVim, Visual Studio Code, Sublime Text.
Operating System : Windows 11, Red Hat Enterprise Linux 9
Additional Skills : Server Development/Administration – Windows, Linux (Automated tools)

EXPERIENCE

Assistant Systems Engineer **TCS | March 2025 – Present**

- Completed ILP training in the domains of Windows 11, Windows Server 2019, Networking Basics, and Red Hat Enterprise Linux 9.
- Obtained Xceed Certification in advanced domain training in Linux Server Administration with a 92% score, standing in the top 2% of the batch.
- Worked on patching activities for the Windows and Linux servers on a monthly, bimonthly, and quarterly basis.
- Monitoring and resolving the server-related incidents in real time.
- Building, updating, and decommissioning the Linux and Windows servers on a regular basis.

Advanced Design and Verification Trainee **VLSI Guru, Bangalore | June 2024 – February 2025**

- Completed 30+ practical assignments to strengthen fundamentals of digital electronics.
- Designed and verified 5 projects, achieving 95% functional coverage in simulations.
- Mastered Object-Oriented Programming (OOP) principles in System Verilog through 3 mini-projects.
- Developed reusable UVM components, enhancing verification efficiency by 20%.

Collaborated with peers to troubleshoot and optimize RTL designs, reducing simulation time by 15%.

PROJECTS

Project 1:

Title	**SmartMat Alarm System (Final Year Project)**
Duration	Dec 2024 - May 2024
Team size	3

Responsibility	• Engineered an innovative alarm system using piezoelectric sensors. • Achieved 90% signal accuracy and reduced production costs by 20%. • Delivered comprehensive documentation, earning recognition from the department committee.

Project 2:

Title	**Memory Module Design**
Duration	2 Weeks
Team size	1
Responsibility	• Designed a 16 MB memory module using Verilog HDL. • Verified functionality with a 100% functional coverage testbench. • Optimized power efficiency by 10%. • Documented the module's verification strategy for peer learning.

Project 3:

Title	**FIFO Design**
Duration	2 Weeks
Team size	1
Responsibility	• Created synchronous and asynchronous FIFO designs in Verilog HDL. • Conducted 10+ test cases, reducing latency by 15% in asynchronous designs. • Analyzed FIFO applications for effective data buffering. • Implemented corner case testing to ensure robustness under varied conditions.

Project 4:

Title	**SPI Controller Design**
Duration	4 Weeks
Team size	2
Responsibility	• Implemented a modular SPI controller in Verilog HDL, reducing verification time by 20%. • Simulated functionality with 20+ corner cases for robust performance. • Demonstrated SPI protocol communication between peripherals in simulations. • Implemented corner case testing to ensure robustness under varied conditions.

ACADEMIC PROJECTS

RTL development Projects

Title	**RTL Design of a 4-bit ALU:**
Duration	1 Week
Team size	1
Responsibility	• Designed and implemented a 4-bit ALU using Verilog, performing functional simulation and timing analysis.
Title	**FPGA-based Traffic Light Controller:**
Duration	1 Week

Team size	1
Responsibility	• Developed a traffic light controller system using FPGA, implementing state machines and timing sequences.

EDUCATION / QUALIFICATIONS

Bachelor of Technology in Electronics and Communication **2020 - 2024**
JNTUA College of Engineering, Pulivendula
CGPA: 8.88 | Top 10% of the class
Relevant coursework: Digital Logic Design, Microprocessor's, ASIC Design and VLSI Technology

Intermediate (XII) in MPC Stream **2017 - 2019**
AP Residential Junior College, Gyarampalle
CGPA: 10 | Secured 1st rank in district-level academic performance

CERTIFICATIONS

- Xceed Certification (E1 competency) in Linux Server Administration (iEvolve | TCS, 2025)
- Timing Analysis for Digital Systems Certification (Cadence Training, 2024)
- Certified in Advanced VLSI Design and Verification Techniques (Udemy, 2023)
- FPGA Design and Implementation using Verilog (Coursera, 2023)

LEADERSHIP

- Directed a team of 15 volunteers for the E-Samagra 2k23 college fest, organizing 10+ competitions and attracting 200+ participants.
- Enhanced event planning efficiency by 25%, ensuring seamless execution.
- Introduced a task management system to streamline volunteer coordination.

HOBBIES & INTERESTS

- Exploring and prototyping FPGA and ASIC applications using open-source tools.
- Staying updated on VLSI industry trends and participating in online forums and hackathons.
- Automating workflows with Python, successfully developing 3 productivity tools.
- Reading technical blogs and papers on semiconductor technologies.

ADDITIONAL INFORMATION

- Strong work ethics with innovative thinking.
- Effective communicator and team collaborator.
- Quick learner, adept at mastering new technologies and methodologies.
- Certified in advanced VLSI design tools and timing analysis through industry-recognized training programs.

(K Devendra)