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Register No.									

# BE Degree Examination November 2014

#### Third Semester

# Electronics and Communication Engineering

#### 11EC301 - DIGITAL ELECTRONICS

(Regulations 2011)

Common to Computer Science and Engineering and BTech Information Technology

Time: Three hours

Maximum: 100 marks

# Answer all Questions

$$Part - A (12 \times 2 = 24 \text{ marks})$$

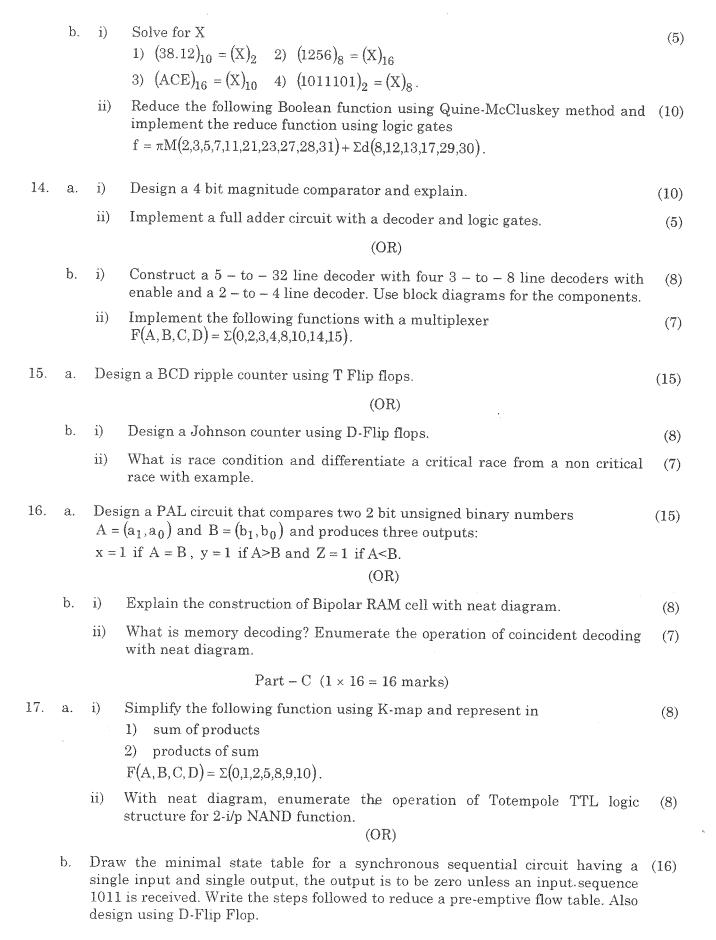
- 1. Convert (22.64), to hexa decimal number.
- 2. Perform the subtraction with the following binary numbers using 2's complement 11010 1101.
- 3. Simplify the following Boolean function xyz + x'y + xyz'.
- 4. Draw the CMOS logic structure for 2 i/p NAND gate.
- 5. Design a half subtractor using logic gate.
- 6. Draw the logic diagram for Four-to-one multiplexer.
- 7. Distinguish between combinational logic and sequential logic circuits.
- 8. Convert JK flip flop into a T flip flop.
- 9. Compare volatile memory and non-volatile memory.
- 10. What is PLA? And how it differs from ROM?
- 11. The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and data lines are needed for the memory  $8K \times 8$ .
- 12. What is Hazards? How it can be eliminated?

$$Part - B (4 \times 15 = 60 \text{ marks})$$

- 13. a. i) Convert the binary number into its decimal equivalent 1100101011.1110. (5)
  - ii) Simplify the following Boolean function F, together with the don't care (10) condition of using K-Map. Also Implement using NOR gates.

$$F(A, B, C, D) = \Sigma(2,4,6,10,12)$$

$$d(A, B, C, D) = \Sigma(0,8,9,13).$$



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