R–11491

Register No. | | | | | | | | |

BE Degree Examination November 2014

Third Semester

Electronics and Communication Engineering

11EC301 – DIGITAL ELECTRONICS

(Regulations 2011)

Common to Computer Science and Engineering and BTech Information Technology

Time: Three hours Maximum: 100 marks

Answer all Questions

Part – A (12 × 2 = 24 marks)

1. Convert $(22.64)_{10}$ to hexa decimal number.
2. Perform the subtraction with the following binary numbers using 2's complement
   11010 – 1101.
3. Simplify the following Boolean function
   $xyz + x'y + xyz'$.
4. Draw the CMOS logic structure for 2 i/p NAND gate.
5. Design a half subtractor using logic gate.
6. Draw the logic diagram for Four-to-one multiplexer.
7. Distinguish between combinational logic and sequential logic circuits.
8. Convert JK flip flop into a T flip flop.
9. Compare volatile memory and non-volatile memory.
10. What is PLA? And how it differs from ROM?
11. The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and data lines are needed for the memory $8K \times 8$.
12. What is Hazards? How it can be eliminated?

Part – B (4 × 15 = 60 marks)

13. a. i) Convert the binary number into its decimal equivalent 1100101011.1110. (5)

    ii) Simplify the following Boolean function F, together with the don't care condition of using K-Map. Also Implement using NOR gates. (10)

    $F(A, B, C, D) = \Sigma(2,4,6,10,12)$

    $d(A, B, C, D) = \Sigma(0,8,,9,13)$.

(OR)

b. i) Solve for X (5)

1) $(38.12)_{10} = (X)_2$ 2) $(1256)_8 = (X)_{16}$

3) $(ACE)_{16} = (X)_{10}$ 4) $(1011101)_2 = (X)_8$.

ii) Reduce the following Boolean function using Quine-McCluskey method and implement the reduce function using logic gates (10)

$f = \pi M(2,3,5,7,11,21,23,27,28,31) + \Sigma d(8,12,13,17,29,30)$.

14. a. i) Design a 4 bit magnitude comparator and explain. (10)

ii) Implement a full adder circuit with a decoder and logic gates. (5)

(OR)

b. i) Construct a 5 – to – 32 line decoder with four 3 – to – 8 line decoders with enable and a 2 – to – 4 line decoder. Use block diagrams for the components. (8)

ii) Implement the following functions with a multiplexer (7)
$F(A,B,C,D) = \Sigma(0,2,3,4,8,10,14,15)$.

15. a. Design a BCD ripple counter using T Flip flops. (15)

(OR)

b. i) Design a Johnson counter using D-Flip flops. (8)

ii) What is race condition and differentiate a critical race from a non critical race with example. (7)

16. a. Design a PAL circuit that compares two 2 bit unsigned binary numbers (15)
$A = (a_1, a_0)$ and $B = (b_1, b_0)$ and produces three outputs:
$x = 1$ if $A = B$, $y = 1$ if A>B and $Z = 1$ if A<B.

(OR)

b. i) Explain the construction of Bipolar RAM cell with neat diagram. (8)

ii) What is memory decoding? Enumerate the operation of coincident decoding with neat diagram. (7)

Part – C ($1 \times 16 = 16$ marks)

17. a. i) Simplify the following function using K-map and represent in (8)

1) sum of products

2) products of sum

$F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10)$.

ii) With neat diagram, enumerate the operation of Totempole TTL logic structure for 2-i/p NAND function. (8)

(OR)

b. Draw the minimal state table for a synchronous sequential circuit having a single input and single output, the output is to be zero unless an input sequence 1011 is received. Write the steps followed to reduce a pre-emptive flow table. Also design using D-Flip Flop. (16)