Q.25 Write a VHDL. Code for 8:1 multiplexer using case statement.

Q.26 Distinguish between combinational and sequential circuit.

Q.27 What is the concept of overloading?

Q.28 Write a VHDL code for full adder using dataflow method.

Q.29 What is a process statement? Write its syntax.

Q.30 Differentiate between ROM & RAM.

Q.31 Discuss the internal architecture of FPGA.

Q.32 Design and implement, A-4 bit binary to excess-3, code converter using case statement.

Q.33 Write a short note on PEEL.

Q.34 What are PLD's? What are its types.

Q.35 Write down the VHDL code for following logical expression.

$F(A, B, C, D) = m(1,4,8,9,13,14)$

Section D

Note: Long answer Questions. Attempt any two Questions out of three Questions. (2x10=20)

Q.36 Explain different styles of modelling using VHDL taking an example of 4:1 multiplexer.

Q.37 Design a sequential circuit of 4-bit up counter in VHDL code.

Q.38 Write a short note on any two of the following

a) PLA
b) Block statement
c) Distinguish between signal & variable

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Roll No.....

121061B

Eltx. Engg.

Subject : VLSI

Time : 3 Hrs. **M.M. : 100**

SECTION-A

Note : Multiple choice questions. All questions are compulsory. (10x1=10)

Q.1 CAD in VLSI stands for _____

a) Computer aided device
b) Computer aided draft.
c) Computer aided design
d) Computer animated design

Q.2 VLSI is an acronym for _____.

a) Very large-scale integration
b) Varying large scale integration
c) Varying large scale integrity
d) None of the above

Q.3 Among the VHDL features, which language statements are executed at the same time in parallel flow?

a) Concurrent b) Sequential
c) Test bench d) All of the above

Q.4 In VHDL, which object is used to connect entities together for the model formation?

a) Constant b) Variable

c) Signal d) None of the above

Q.5 In composite data type of VHDL, the record type comprises the elements of _____ data types.

a) Same d) Different

c) Both A & B d) None of the above

Q.6 The simple programmable logic device (SPLDs) are also regarded as _____.

a) PAL b) GAL

c) PLA d) All of the above

Q.7 Which of the following is not a type of modelling style in VHDL?

a) Behavioral style b) Complex style

c) Dataflow style d) Structural style

Q.8 Which of the following is a class of object declaration?

a) Constant b) Variable

c) File d) All of the above

Q.9 Which of the following is not an example of integer data type?

a) Type WORD is range 31 downto O,

b) Type CURRENT is range 2 to 24;

c) Type is VOLTAGE range 2.5 to 24.5;

d) Type TEMPERATURE is range 200 to 400;

Q.10 Which of the following is not a type of logical operator?

a) And b) Mod

c) Nor d) Xor

Section B

Note: Objective types Questions. All Questions are compulsory. (10x1=10)

Q.11 What are keywords?

Q.12 What do you mean by an entity?

Q.13 Name different types of delays used in VHDL.

Q.14 What is a clock signal?

Q.15 Define the term 'Variable" with syntax.

Q.16 Name any two combinational circuits.

Q.17 What is a difference between bit and boolean?

Q.18 What is the full form of GAL?

Q.19 Give the syntax of for loop statement.\

Q.20 What is a PAL?

Section C

Note: Short answer type Questions. Attempt any twelve Questions out of fifteen Questions. (12x5=60)

Q.21 What are the basic design units in VHDL?

Q.22 What are the different types of data types used in VHDL?

Q.23 Give the classification of modelling structures used in VHDL?

Q.24 Explain in briefly the evolution of VHDL. Language.