Q.28 What is the difference between array and records. Give example.

Q.29 Write VHDL code for 4-bit gray to binary code converter.

Q.30 Implement 4:1 multiplexer using dataflow style of modeling.

Q.31 What do you mean by delay? Explain types of delay used in VHDL.

Q.32 Write a short note on :

a) VHDL model b) Overloading

Q.33 What is the difference between PLA and PAL.

Q.34 Draw structure of CPLD.

Q.35 Explain about physical design of FPGA.

SECTION-D

Note: Long answer type questions. Attempt any two questions out of three questions. (2x10=20)

Q.36 Explain difference between behavioural, data flow and structural modelling with examples of each.

Q.37 Explain the structural difference between ROM and PLA.

Q.38 Write a VHDL code using behavioural style of modelling for SIPO.

Roll No. .....

6th Sem / Branch : Eltx.

Sub.: V.L.S.I. System Design

Time : 3Hrs. M.M. : 100

SECTION-A

Note: Multiple choice questions. All questions are compulsory (10x1=10)

Q.1 VLSI technology uses_____ to form integrated circuit.

a) Transistor b) Switches

c) Diodes d) Buffers

Q.2 Medium scale integration has

a) 10 Logic gates b) 50 Logic gates

c) 100 Logic gates d) 1000 Logic gates

Q.3 Gate minimization technique is used to simplify logic

a) True b) False

Q.4 The correct syntax for using EXIT in a loop is _____

a) EXIT loop label WHEN condition

b) EXIT WHEN condition loop label

c) Loop label WHEN condition EXIT

d) EXIT WHEN loop label condition

Q.5 The most basic form of behavioral style of modeling in VHDL is

a) IF statement

b) LOOP statement

c) ASSIGNMENT statement
d) WAIT statement

Q.6 SIGNED and UNSIGNED data types are defined in which package?
a) std_logic_1164 package
b) std_logic package
c) std_logic_arith package
d) standard package

Q.7 Use of constants is to _____
a) Represent wires
b) Represent local information
c) Represent default value
d) Pass value between entitles

Q.8 Which of the following can't be declared in an architecture?
a) Signal b) Constant
c) Variable d) BIT_VECTOR

Q.9 Once a PAL has been programmed
a) It cannot be reprogrammed
b) Its output are only active HIGHs
c) Its output are only active LOWs
d) Its logic capacity is lost

Q.10 The content of a simple PLD consists of
a) fuse-link array
b) advanced sequential logic functions
c) Thousands of basic logic gates
d) Thousands of basic logic gates and advanced sequential logic functions

SECTION-B

Note: Objective type questions. All questions are compulsory. (10x1=10)

Q.11 Define Entity.
Q.12 What do you mean by package declaration.
Q.13 Define variable.
Q.14 Describe the structure of a package.
Q.15 What is an array?
Q.16 Write full form of ROM.
Q.17 Name any two logical operators.
Q.18 Perform srl3 shift operation on bit vector :1000101".
Q.19 Write syntax of case statement.
Q.20 Write full form of FPGA.

SECTION-C

Note: Short answer type questions. Attempt any twelve questions out of fifteen questions. (12x5=60)

Q.21 Explain design units of an entity in VHDL.
Q.22 What do you mean by data objects and data types?
Q.23 Explain structural style of modeling with example.
Q.24 Give classification of operators used in VHDL.
Q.25 List the various scalar data types and explain with example.
Q.26 Compare software and hardware description language.
Q.27 With one example compare STD_LOGIC and STD_ULOGIC.