

Roll no. _____

ID: 180945/170945

Semester: 4th
Branch: Electrical
Subject Name: Digital Electronics

Time Allowed : 3 Hrs.

MM:100

Section -A

Note: Multiple Choice questions. All questions are compulsory.

$$10 \times 1 = 10$$

Section-B

Note: Objective type questions. All questions are compulsory.

$$10 \times 1 = 10$$

- Q.11** Define term K-MAP.

Q.12 What is Logic Gate?

Q.13 Write any two applications of A/D converters.

Q.14 Name different types of Shift Registers.

Q.15 Define Min term.

Q16. Prove that $A + A.B = A$

Q.17 Draw the symbol of EX-OR gate

Q.18 What is Counter?

Q.19 Define Analog Signal.

Q.20 Write full form of ASCII and EBCDIC.

Section -C

Note: Short answer type Questions. Attempt any twelve questions out of fifteen questions. $12 \times 5 = 60$

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- Q.21** What do you mean by Digital Signal? Explain advantages and application of Digital signal.

- Q.22 Multiply the following Binary Numbers:
 (i) 110110×0110 (ii) 10101×101
- Q.23 What is Error Correcting Coded? How it can be corrected by using parity?
- Q.24 Do the subtraction by using 2's complement method of subtraction:
 (i) $1001 - 1110$ (ii) $11011 - 01101$
- Q.25 Explain Block diagram, Logical expression, Truth Table of Decimal to BCD Encoder.
- Q.26 Design Block diagram, Truth Table, Logical Expression of 8 : 1 MUX.
- Q.27 Differentiate between Synchronous Counter and Asynchronous Counter
- Q.28 Draw the symbol, logical expression, truth table and pulse operation of EX-NOR gate.
- Q.29 Solve the following Boolean expression:
 (i) $ABC + AB\bar{C}D + A\bar{B}\bar{C} + A\bar{B}D + A\bar{D}$
 (ii) $XY + X(Y+Z) + Y(Y+Z)$
- Q.30 State and explain Demorgan's Theorems.
- Q.31 Why NAND and NOR gates are known as universal gates?.
- Q.32 Explain the working of PIPO shift register with the help of pulse diagram.
- Q.33 Discuss truth table, logic diagram and logical expression of a Full Adder.
- Q.34 What do you mean by DEMUX? Design a 1 : 8 DEMUX by using truth table, logical expression and logical circuit.
- Q.35 What is the difference between Latch and Flip-Flop?

Section-D

Note: Long answer questions. Attempt any two questions out of three questions.

2x10=20

- Q.36 Minimize the following Boolean expression using K-Map and realize the logic Circuit using NAND gates only.
 $F(A,B,C,D) = \Sigma M(1,3,5,7,9,15) + d(4,6,12,13)$
- Q.37 Explain the Logic Diagram, Truth Table and Operation of a J-K flip flop with neat Diagram.
- Q.38 Write short note on following:
 a. Binary Weighted Digital to Analog Converter
 b. Ring Counter