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4th Sem / Branch : Computer/IT
Subject:- Computer Organization

Time : 3Hrs. M.M. : 100

SECTION-A

Note: Multiple choice questions. All questions are compulsory (10x1=10)

Q.1 Which of the following is an input device (Co1)
a) Plotter b) Printer
c) LED Monitor d) Keyboard

Q.2 Both CISC and RISC architecture have been developed to reduce the_____ (CO1)
a) Time delay b) Semantic gap
c) Cost d) All of the above

Q.3 Which of the following allows simultaneous read and write operations (CO2)
a) ROM b) EROM
c) RAM d) None of the above

Q.4 Using a_____buffer the instruction fetch segment is implemented. (CO2)
a) FIFO b) LIFO
c) MIFO d) SIFO

Q.5 Cache memory is located between_____and____ (CO2)
a) CPU and main memory
b) HDD and RAM
c) RAM and ROM
d) There is no such memory

Q.6 MIPS stands for (CO3)
a) Mandatory instructions / sec
b) Millions of instructions /sec
c) Most of instructions / sec
d) Many instructions /sec

Q.7 Each stage in pipelining should be completed within_____cycle (CO4)
a) 1 b) 2
c) 3 d) 4

Q.8 The address generated by CPU is generally referred to as_____ (CO4)
a) Physical address b) Associative address
c) Referral address d) Logical address

Q.9 The DMA transfers are performed by a control circuit called as_____ (CO3)
a) Device interface b) DMA controller
c) Data controller d) Overlooker

Q.10 Virtual memory consists of (CO2)
a) Dynamic RAM b) Static RAM
c) Magnetic memory d) none of these

SECTION-B

Note: Objective type questions. All questions are compulsory. (10x1=10)

Q.11 The addressing mode, where you directly specify the operand value is_____ (CO1)

Q.12 Cache memory is the on board storage. (True/False) (CO2)

Q.13 Storage which stores or retains data after power off is called_____ (volatile/non volatile memory) (CO2)

Q.14 Parallel computers are either_____or MIMD. (CO4)

Q.15 Each stage in pipelining should be completed within_____cycle. (CO4)

Q.16 After the completion of the DMA transfer, the processor is notified by____(interrupt signal/HDD) (CO3)

Q.17 Three basic parts of the CPU are_____,_____ and _____ (CO1)

Q.18 The program counter points at the_____of the next instruction in the program (CO1)

Q.19 Static Ram is made up of_____ (CO2)

Q.20 Access time=_____+_____ (CO2)

SECTION-C

Note: Short answer type questions. Attempt any twelve questions out of fifteen questions. (12x5=60)

Q.21 What do you mean by CPU? Explain the general register organization. (CO1)

Q.22 Explain one address instruction. (CO1)

Q.23 Give the differences between microprogrammed and hard wired control. (CO1)

Q.24 Explain the differences between RISC and CISC. (CO1)

Q.25 Give the differences between direct mapping and associative mapping (CO2)

Q.26 Explain Vritual memory. (CO2)

Q.27 What is address mapping? Explain. (CO2)

Q.28 Explain hit rate in context of cache memory (CO2)

Q.29 What are the major functions of BIOS (CO3)

Q.30 What is the role of DMA in data transfer (CO3)

Q.31 What is BIOS POST test. (CO3)

Q.32 Explain the interrupt initiated mode of data transfer. (CO3)

Q.33 Explain the types of parallel processing. (CO4)

Q.34 Explain multistage switching network. (CO4)

Q.35 Write a note on multiprocessor organization. (CO4)

SECTION-D

Note: Long answer type questions. Attempt any two questions out of three questions. (2x10=20)

Q.36 Explain DMA and DMA controller (CO3)

Q.37 Write a short note on (CO2)

a. Memory hierarchy

b. Memory connections to CPU

c. Time shared common bus

Q.38 What is addressing modes? Explain the types of addressing modes? (CO1)