Q.27 Explain data flow style of modeling with example.
Q.28 Implement 4:1 multiplexer using data flow style of modeling.
Q.29 List different types of operators used in VHDL.
Q.30 Explain features of CPLD.
Q.31 Write a short note on:
a) VHDL model
b) Types of delay
Q.32 What is the difference between array and records give example.
Q.33 Write a VHDL code to design 4-bit BCD to gray code converter.
Q.34 Draw and Explain internal structure of ROM.
Q.35 List difference between PAL and PLA.

SECTION-D

Note: Long answer type questions. Attempt any two questions out of three questions. (2x10=20)

Q.36 Explain with example different style of modeling used in VHDL.
Q.37 Write a VHDL code using behavioral style of modeling for SISO.
Q.38 Explain in detail about physical design of FPGA.

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Sub. : V.L.S.I. system design

Time : 3Hrs. M.M. : 100

SECTION-A

Note: Multiple choice questions. All questions are compulsory (10x1=10)

Q.1 An MSI chip contains _____components embedded on it.
a) Lesser than 10
b) Greater than 10 and less than 100
c) Lesser than 1000 and greater than 100
d) Greater than 10000

Q.2 Gate minimization technique is used to simplify logic.
a) True b) False

Q.3 For any concurrent assignment statements, which of the following is true.
a) The statement is executed once
b) The statement is executed twice
c) The value of left operand is assigned to right operand
d) The statement is executed as many as value changes

Q.4 An UNSIGNED type is always greater than zero

a) True b) False

Q.5 Where do we declare the loop index of a FOR loop?

a) Entity
b) Architecture
c) Library
d) It doesn't have to be declared

Q.6 One can't define an array without any constraints in VHDL

a) True b) False

Q.7 A SUBTYPE can be defined as _____.

a) A TYPE under a TYPE (nested)
b) A TYPE of INTEGER data type
c) A TYPE with some constraints
d) A TYPE without any constraints

Q.8 What is the use of variable

a) To represent local value
b) To represent default value
c) To set default value
d) To declare a subprogram

Q.9 PLAs, CPLDs and FPGA are which type of device?

a) SLD b) EPROM
c) PLD d) SRAM

Q.10 Which types of PLD should be used to program basic logic function

a) PLA b) CPLD
c) PAL d) SLD

SECTION-B

Note: Objective type questions. All questions are compulsory. (10x1=10)

Q.11 Define signal.
Q.12 Define variable.
Q.13 What do you mean by entity declaration.
Q.14 What do you mean by data objects.
Q.15 Name any two relational operators.
Q.16 Name two types of identifiers.
Q.17 Expand RAM.
Q.18 Name any two data types.
Q.19 Write full form of GAL.
Q.20 Expand EPGA.

SECTION-C

Note: Short answer type questions. Attempt any twelve questions out of fifteen questions. (12x5=60)

Q.21 List different steps involved in VLSI design flow.
Q.22 What are design units of VHDL?
Q.23 Write a VHDL code to design full adder using half adder using structural style of modeling.
Q.24 What do you mean by statement? Explain wait statement with syntax.
Q.25 Explain various data objects used in VHDL language.
Q.26 What do you mean by hardware description language?