A Reconfigurable Digital Filter Chip For Image Processing

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Abstract :

The scope of this paper is to present a Programmable Digital Filter (PDF) design. This architecture can be programmed to implement any eight order Infinite Impulse Response (IIR) or Finite Impulse Response (FIR) filters. The coefficient, input and output data word lengths are coded on 16 bit, internal results are on 32 bit. A first low cost VLSI implementation of this architecture was validated and tested successfully in a 0.7 µm CMOS technology, with an area of 27 mm² and a maximum clock frequency of 40Mhz. The migration in a 0.25 µm CMOS process allows us to reach a 150 MHz clock frequency with an area of 5mm². A specific board has been developed for fast prototyping of real time image processing applications.

I – Introduction :

In digital signal and image processing algorithms, a key step consists of using digital filters (IIR or FIR) [1],[2],[3],[4]. The filter implementation can be realized with specific cores or with programmable devices [5].

Advances in field programmable gate arrays technology have enabled FPGA's to be used in a variety of applications. However, the design of a high order digital filter in a SRAM-FPGA is possible only if the filter coefficients are fixed [6].

The ATMEL programmable filter (AT76C002) [7] is able to implement a 16 taps programmable digital filters with a maximum clock frequency of 33 Mhz, but this one is limited to FIR filters.

Software solution, as specific DSP processors could be considered [8] , but data rate obtained doesn't reply to real time image processing constraints.

For these reasons, a reconfigurable architecture "PDF" (Programmable Digital filter) dedicated to IIR and FIR digital filters and for fast real time image processing prototyping is proposed.

This paper is organized as follows : in section II the PDF architecture and the programmation steps are presented. In section III, the performances obtained are described. Section IV describes a new version of this architecture, PDF1.

II – PDF : Programmable Digital Filter architecture

In Figure 1 the PDF architecture designed with eight cascaded first order cells is described. Each cell implements a 16x16 bit Booth multiplier [9], a 32 bit Carry-Select adder[10], a 32 bit register and a 16 bit programmable register.

With a set of multiplexers, the designer is able to choose the filter architecture datapath (FIR or RII).

X[n] and Y[n] are respectively the input and the output of the filter. Two classes of registers are defined, the first one (R1) is a register with multiplexers on the D input of the flip-flop. It allows to choose directly the input (for FIR filter) or the feedback of Y[n] (for IIR filter). The control of these multiplexers is realized by the $Ai_{i=1,\dots,7}$ data.

The second register (R2) is classical 32 bit registers which allow us to save the intermediate results. The $Fi_{i=0,\dots,7}$ are the filter coefficients coded in a 16 bit format.

A 32 bit internal data accuracy bus is used. To respect the 16 bit data coding of the multiplier, added which allow us to choose 16 bit among the 32 bit coming from the last adder.

To increase the flexibility of the PDF, an additional multiplexer (R[n]) is added, enabling us to cascade others FIR or IIR filters.

Mathematical equation of the filter could be represented by the following equation :

$$y[n]=F_0x[n-8]+\sum_{i=1}^{i=7}F_i\left(\begin{array}{l}A_ix[n-(8-i)]+\\ \quad \overline{A}_i\left(C_iy[n-(8-i)]+\overline{C}R[n-(8-i)]\right)\end{array}\right) \quad (I)$$

The Fi, Ai and C values mean that we program the filter equation wanted, section II.2 gives a practical example.

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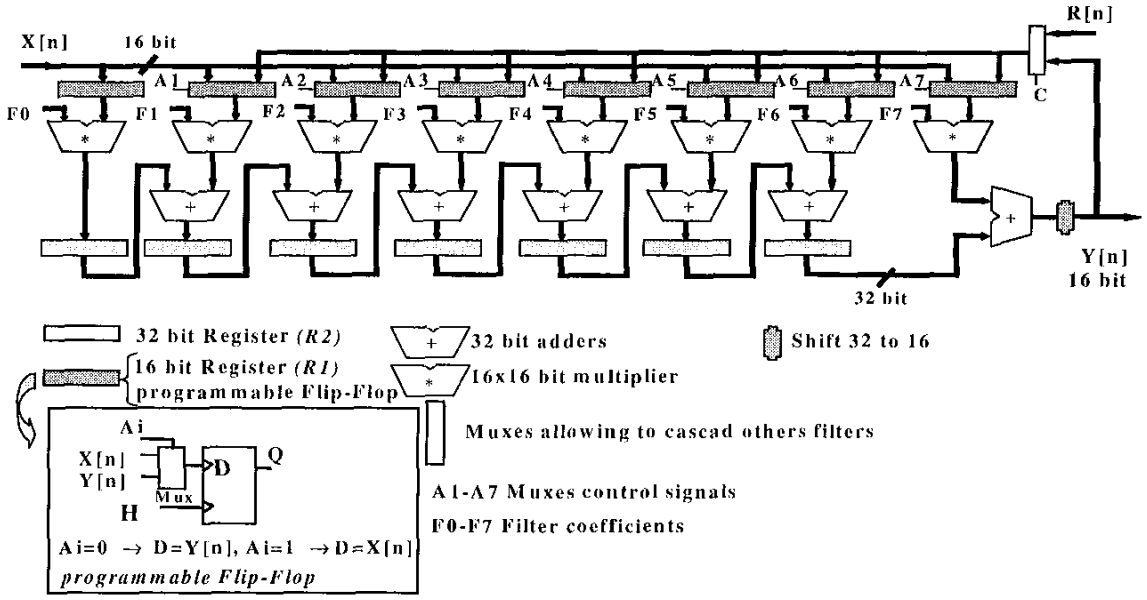

Figure 1 : Programmable Digital Filter architecture

II.1 – Example of programmation

This architecture is able to implement any seven order recursive filter, or a height order non recursive filter A third order recursive filter, corresponding to the optimized Canny_Deriche filter for ramp edge detection in noisy and blurred images [11] is proposed as an example. The recursive equation to implement is the following :

$$y(n) = b_1 x(n-1) + b_2 x(n-2) + b_3 y(i-1) - b_4 y(n-2) + b_5 y(n-3)$$

Where the $bi_{i=1,\ldots,5}$ are the filter coefficients. (2)

The muxes control signal respect the following rules :

- Ai = 1 : x[n] as input of the multiplier register (R1),
- Ai = 0 : y[n],the feed back loop, as input of the multiplier register (R1),

By using the equation eq1.1, the ordering signals to configure the P.F.A are :

- The coefficient F0 to F2 equal to zero, F3= b_2; F4=b_1; F5=b_5; F6=b_4 and F7=b_3.
- A3 and A4 are equal to zero, and A5 to A7 and C are equal to one.

In this way, the obtained datapath is represented in figure 2.

III – Chip design

This section presents the chip design of the PDF, and some results achieved on silicon.

III.1 - Global Architecture

Three main blocks composed the testchip achieved with the PDF core (given in Figure 3). To configure the PDF, a shift register is used where all the coefficients and control signals are loaded in serial mode. A state machine synchronizes the shift register and the PDF.

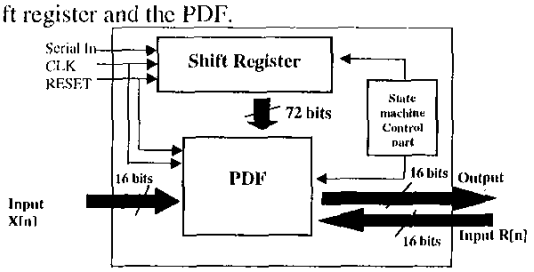

Figure 3 : Global architecture of the PDF circuit

III.2 Silicon implementation

A first implementation has been achieved using a cell-based approach in a CMOS 0.7 µm (ATMEL ES2), with the CAD tool OPUS (Cadence Design Framework II). In our cell based approach the choice of a 32 bit Carry Select Adder [10] and a compiled 16x16 bit booth multiplier [9] gives the best speed/area compromise [12].

The maximum clock frequency is about 40 MHz, in this way, the PDF can be configured in less than 3.2 microseconds

-Internal precision : 32 bit

-Coefficient Coding :
16 bit in two's complement notation

-Internal precision :
32 bit in two's complement notation

- Programmation time 3.2 µs

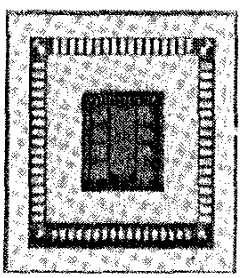

Figure 4 : The programmable filter chip.

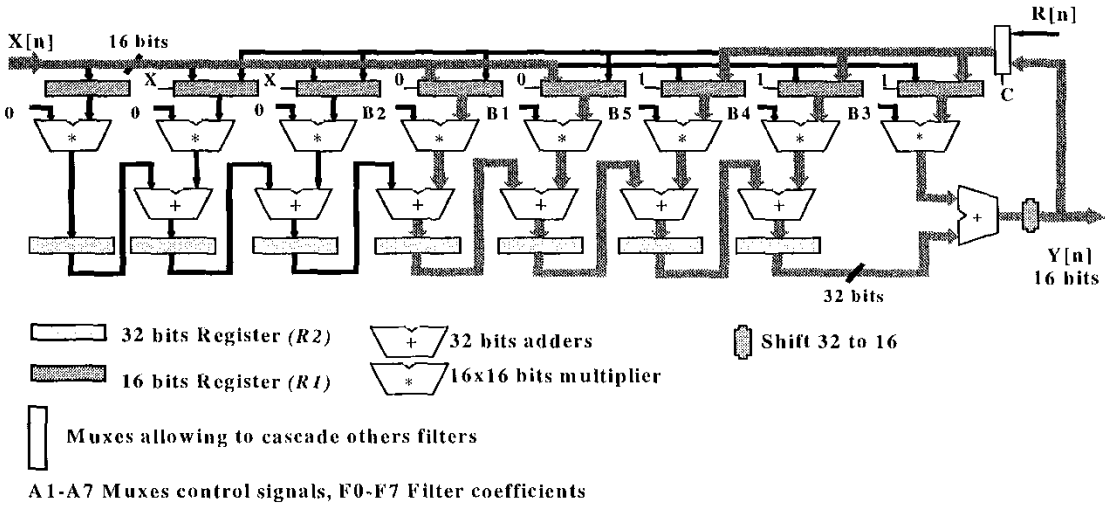

Figure 2 : PDF programmation example

III.3 Board development

This testchip is used to develop fast prototyping image processing applications. The board designed is presented in figure 5.

This board is composed of an image acquisition platform, and the testchip board with the associate memories. A specific compiler has been developed and interfaced by the PC with the platform.

To validate this platform and the testchip, a real time application has been implemented : an edge detection algorithm using the Shen & Castan digital filter [13].

The clock frequency of the platform depends on the image format. For an 512x512 pixel images the clock frequency is about 10Mhz. For 1024x1024 pixel images 40 MHz is needed and could be attained by the system.

IV - PDF1 architecture

Taking into account our test results and the feed back of this core's users, a new version of this core has been developed, PDF1. This version which re-uses the PDF core, described in previous sections, includes new features.

IV.1 PDF1 architecture

The additional main features are the following :

- Two 16 bit data width input buses X1 and X2 (in two's complement format)
- Two 16 bit data width output buses Y1 and Y2 (in two's complement format)
- 2 RAM 1024x16 bit, could be configured in FIFO LIFO mode
- Dynamically reconfiguration mode, 100 ns to reconfigure entirely the PDF1 architecture
- Clock frequency for the PDF1 : 150 MHz
- Clock frequency to download coefficients : 300 MHz

Multipliers' coefficients are coded on 16 bit. Global architecture is described in Figure 6.

Four different parts must be distinguished :

- Mux inputs : we can choose between X1, X2, Y2 (in case of IIR filter), samples of RAM1. Two independent inputs can treat 2 different functions on the same architecture (of course the order of the 2 functions have to be in adequacy with the global order of PDF1).
- Mux outputs : we can select the filter order. Bypass muxes mode is available in the case of IIR filters (to avoid poles' insertion in the feedback loop). Furthermore, RAM2 can be chosen to memorize sample results.
- Filter module : Composed as before in the PDF core, by a 16x16 bit Booth multiplier, 32 bit Carry-Select adder, 32 bit register, 16 bit programmable register.
- RAMs : The chip implements two RAMs which can be used in FIFO or LIFO mode. Other advantages of these RAMs are that they can be configured to treat pictures of 256, 512 and 1024 pixels

IV.2 Silicon implementation

This new implementation has been done using a cell-based approach in a CMOS 0.7 µm (ATMEL ES2), with the CAD tool OPUS (Cadence Design Framework II). As before, in our cell-based approach the choice of a 32 bit Carry Select Adder [10] and a compiled 16x16 bit booth multiplier [9] gives the best speed/area compromise [11].

The circuit complexity is about 150 000 transistors with a total layout area of 55 mm2 including 100 pads (figure 7). It has been successfully simulated

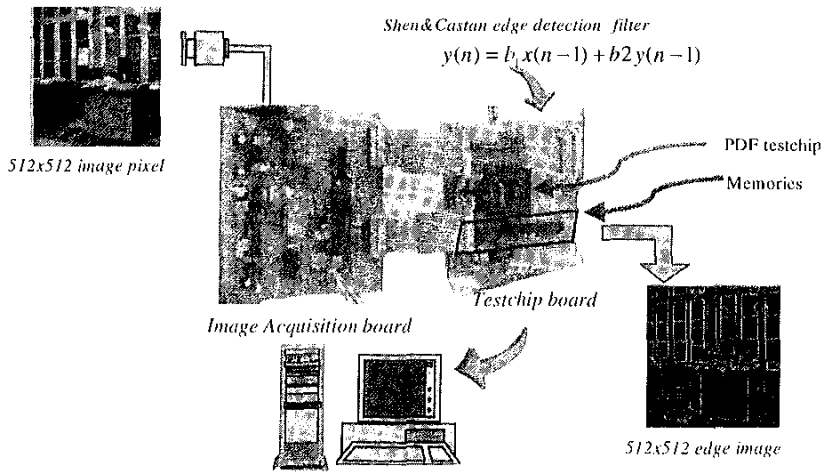

Figure 5 : Prototyping

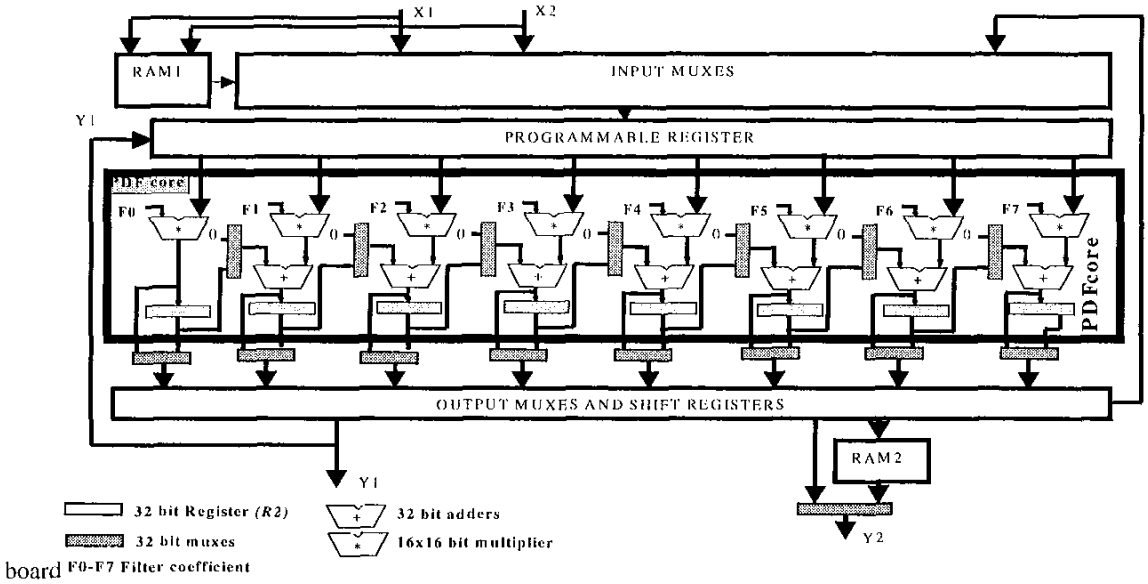

Figure 6 : PDF1 architecture

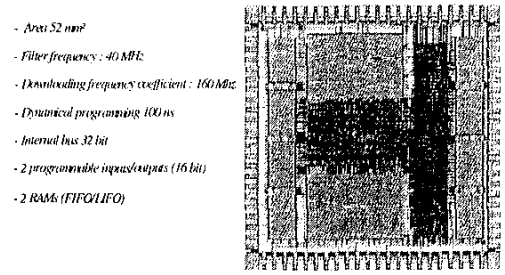

Figure 7 : PDF1 layout

We are looking to transfer this new reconfigurable filter core in a CMOS 0.25µm process. First estimation gives a clock frequency about 150 Mhz for an area of 5 mm^2.

IV.3 Filters architecture configuration

Figure 8 shows how the new chip can be used to implement different filter architecture configurations.

A 8 tap FIR or IIR filter (Figure 8a), two separate cascaded filters (Figure 8b) can be directly implemented. Line memories (figure 8c,8d) can be inserted between filters which is useful in image processing for convolution [2].

V – CONCLUSION

The PDF ASIC allows fast prototyping of digital signal processing applications. An implementation of this architecture in real time image processing has been tested successfully and shows the interest and the flexibility of this approach. Comparisons between our circuits and different

standard products (AT76C002 programmable filter from ATMEL, DSP C6x from Texas Instrument) shows the interest of our PDF cores. Comparison is given for an 8 order FIR filter with 100 samples on the filter input.
Trade-off between flexibilty and performances has been reached with the PDF cores design. An array of 3x3 PDF core is under development in a CMOS 0.25 µm technology.

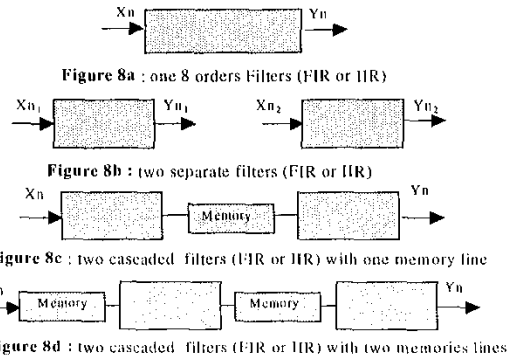

Figure 8a : one 8 orders Filters (FIR or IIR)

Figure 8b : two separate filters (FIR or IIR)

Figure 8c : two cascaded filters (FIR or IIR) with one memory line

Figure 8d : two cascaded filters (FIR or IIR) with two memories lines

Figure 8 : Main configurations of the PDF1 core.

Table 1 : comparison of different devices for 100 samples on the filter inputs.

	FIR	IIR	# multiplier	Cascade	Memory	Data width	# Cycles	Cycle time	Delay
DSP TI C6x	Yes	Yes	2 mult 16x16	No	512 Kbit	16 bit	810	5 ns	4 us
AT76C002	Yes	No	16 mult 12x16	Yes, FIR only	192 bit	16 bit	108	30 ns	3.2 us
PDF core	Yes	yes	8 mult 16x16	Yes, FIR and IIR	156 bits	16 bit	108	25 ns	2.7 us
PDF1 core (0.25 µm)	Yes	Yes	8 mult 16x16	Yes, FIR and IIR	32 Kbit	16 bit	108	7 ns	0.8 us

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