VLSI Architecture for Exciter, Governor, and Stabilizer in Fast Power System EMT Simulation

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***Abstract*—In the modern power system, fast and accurate simulation tools are needed for transient analysis such as electro-magnetic transients program (EMT). In our previous paper, we proposed a computational framework to model, convert, and accelerate the grid-level EMT simulations based on full custom VLSI (very large scale integration) techniques that runs orders of magnitudes faster than software or FPGA approaches. However, due to the complexity of exciters, power system stabilizers and governors, these components were omitted and the corresponding values are assumed to be constant. In this paper, we propose an efficient VLSI architecture for exciters, power system stabilizers and governors, and implement the architecture using the 45nm process. Circuit simulation results show that the proposed VLSI circuits can solve the system significantly faster than real time without sacrificing accuracy.**

Keywords—electro-magnetic transients program (EMT), exciter, on-chip simulation, very large scale integration (VLSI)

I. INTRODUCTION

In the power industry, the electro-magnetic transients program (EMT) simulations are typically performed through two types of commercial simulation tools. The first type of tools contains the offline EMT simulation software such as PSCAD [1] and EMT-RV [2]. The second type of tools contains real-time digital simulators such as RTDS [3] and OPAL-RT [4]. Some of the simulators [3][4] perform the real-time simulation of fast power electronics dynamics on a generic field-programmable gate array (FPGA)-based solver. These FPGA-based simulators are shown to have much faster computation performance compared to software-based simulators. In our previous paper, we developed a full customized and highly parallel very large scale integration (VLSI) hardware architecture which much faster than the FPGA-based solver of the EMT simulation for large power systems [5].

To further and better simulate the behavior of synchronous machines in power system stability studies, it is essential to model the excitation system including exciters, power system stabilizers (PSS) and governors. Traditionally in EMT programs, excitation systems are modeled using control block diagrams in a frequency domain. Some excitation systems are also modeled as an actual electrical circuit for analysis of its performance. However, these approaches are all hard to map into the hardware-accelerated methods solvers such as FPGA-based.

This paper proposed a highly-parallel VLSI hardware architecture for exciters, PSS and governors. Combine with our previous EMT simulation circuit[5], our approach builds an advanced synchronous machine model and substantially improve the speed of EMT simulation for large power systems. Once successful, this could potentially transform the industry's practice in a conducting faster-than-real-time simulation.

The rest of the paper is organized as follows. Section II describes the detailed excitation system model and the coupled relationship between different modules. Section III presents the system architecture and the hardware implementation of the excitation system. Section IV verifies the result of VLSI circuit against MATLAB. Conclusions are given in Section V.

II. SYSTEM MODEL

This section presents the entire EMT model used in this paper. Fig. 1 shows the overall structure of a 2-bus system. In this system, bus 1 is connected to a synchronous generator with the control system, and bus 2 is connected to a synchronous motor without the control system, and two buses are connected through a three-phase transmission line. Detailed models for the synchronous machines and the transmission line are described in [5]. In this paper, we focus on synchronous generator control system which consists of exciters, PSS and governors.

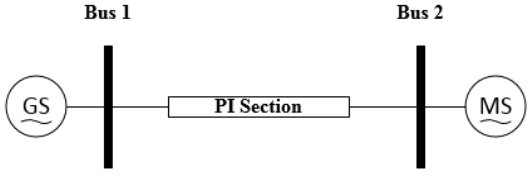

Figure 1. Structure of the 2-bus system.

A. Exciter

Exciters are used to control the synchronous machine field voltage and current. There are three types of exciters based on different excitation power source: DC, AC, and static. In this paper, we illustrate our approach using BPA EA model which is a typical continuously acting DC excitation system model [6]. Other types of models can be solved by the same approach.

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The block diagram of BPA EA is shown in Fig. 2. In the figure, V_T is the magnitude of bus terminal voltage, V_{REF}, V_{STB}, V_{MIN}, V_{MAX} and E_{FD} are the voltage reference set point, the power system stabilizer output signal which is zero in this case, upper voltage limitation, lower voltage limitation and generator field voltage respectively, T_R, T_A, T_{A1}, T_E and T_F are time constants, and S_E is the saturation function in terms of the generator field voltage E_{FD}.

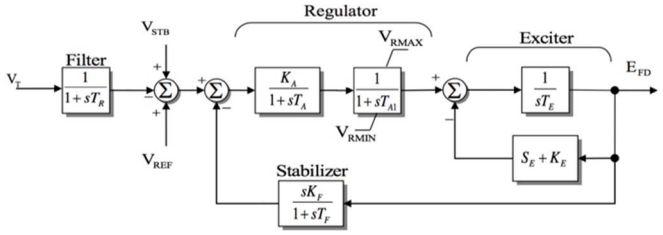


Figure 2. Exciter BPA EA - Continuously acting DC rotating excitation system model.

B. Power System Stabilizer

A PSS is used to enhance damping of power system oscillations through excitation control. The block diagram of type PSS1A [6] which is one typical single-input stabilizer model is shown in Fig. 3. Other types have similar representation.

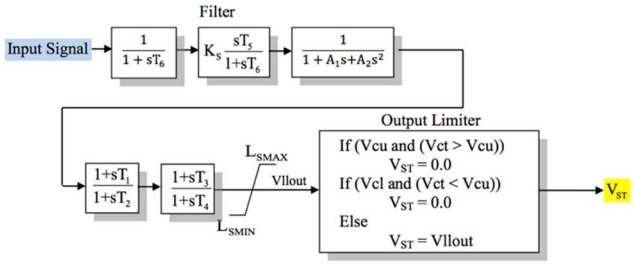


Figure 3. Stabilizer PSS1A - Single-input stabilizer model.

C. Governor

A governor is a device used to measure and regulate the rotor angle speed of a synchronous machine. The block diagram of type BPA GG [6] which is one typical WSCC Type G governor model is shown in Fig. 4. In the figure, $\Delta\omega$ is the rotor speed difference, and P_M is the mechanical power applied to the synchronous machine. Other types have similar representation.

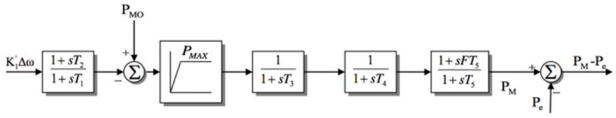


Figure 4. Governor BPA GG - WSCC Type G governor model.

D. System Coupling Relationship

Due to the similar model representations of exciters, PSS and governors, we only solve the exciter in the synchronous generator model at Bus 1. The exciter model we selected is BPA EA. The coupling among different subsystems is shown in Fig. 5. Since the turbine governor model is not included in this study, the mechanical torque T_m is considered to be constant.

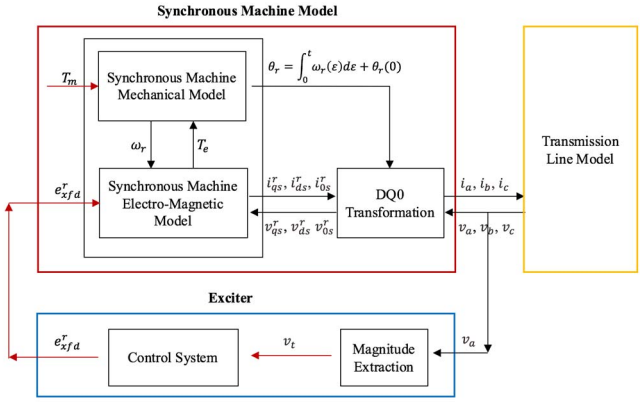


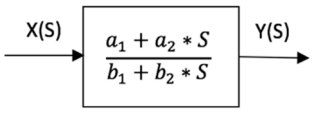
Figure 5. Coupling relationship among different subsystems

III. System Architecture

A. Exciter

According to the model representation, the exciter is divided into three parts: magnitude extraction from the input voltage, the control system which consists of multiple transfer functions, and the limiter.

In the transfer function part, we break down the entire function which from the input to the output into multiple blocks. Each block represents one simple transfer function. Generally, transfer functions used in excitation system are integrator blocks, first order lag blocks, derivative blocks and lead-lag blocks. These blocks share one similar function formula shown below. Given different coefficients, the formula can map into different functions.



We discretize the transfer function according to the Euler rule. In the time domain, the relationship between x and y is shown in (1).

$$y(t+\Delta t) = \frac{b_2 - b_1 * \Delta t}{b_2} * y(t) + \frac{a_2}{b_2} * x(t+\Delta t) + \frac{-a_2 + a_1 * \Delta t}{b_2} * x(t) \quad (1)$$

B. Hardware Implementation

1) Design Hierarchy.

The entire system architecture is divided into three levels as shown in Fig. 6. The bottom level consists of three basic modules. The upper level is sub modules level, consisting of the generator cell, the transmission line model and the exciter. The top level connects all components together.

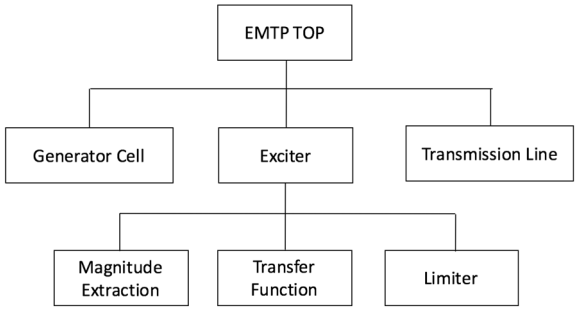


Figure 6. Design hierarchy of our VLSI system.

2) Generator Cell & Transmission line

Detailed designs of these two parts are described in [5].

3) Exciter

The exciter consists of three sub modules. Magnitude extraction is to extract the voltage magnitude, transfer function module is to implement each transfer function block in the control system and the limiter is to limit input values in a specific range.

- *Magnitude Extraction*.

The input of excitation system is the generator terminal voltage from the transmission line. Once we get the terminal voltage, we need to extract the voltage magnitude. To avoid the high frequency noises from varies sources, we add a digital low pass finite impulse response (FIR) filter at the beginning to make sure we catch the magnitude of voltage with 60HZ. The FIR filter structure is shown in Fig. 7.

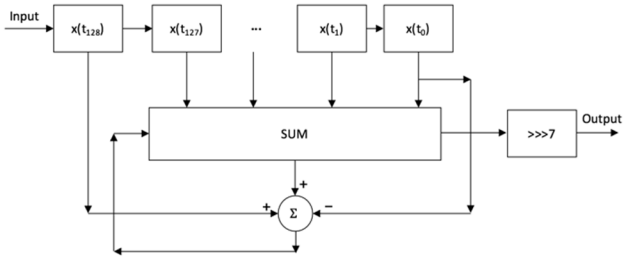


Figure 7. Hardware design of the FIR filter.

The filter is built by adders and a shifter. We store the initial 128 values of inputs first, then put the sum of the 128 values into a register. When a new value comes, update the sum register by adding the new value and subtract the oldest value. The signal processing result between input and output is shown in Fig. 8. As shown, the filter successfully keeps the low frequency and filter the high frequency noise.

After we filter the original input, we do magnitude extraction. The magnitude extraction algorithm is described below:

First, initial registers, where V_pre, V_cur are the previous value and current value of input respectively; dV_pre, dV_cur are the previous value and current value of the derivation value of the input respectively; Peak_old and Peak_new are the old peak value and new peak value respectively, t_new and t_old are the old peak corresponding time and new peak corresponding time respectively.

Repeat following at each time step t,

1. V_pre ← V_new; V_cur ← input;
2. Compare V_pre and V_cur,
   if V_pre < V_cur , then dV_cur =1;
   else if V_pre = V_cur, then dV_cur = 0;
   else dV_cur = –1
3. Compare dV_pre with dV_cur,
   if dV_pre != dV_cur, then
   Peak_old←Peak_new;
   t_old← t_new;
   Peak_new← | V_pre |;
   t_new← t - Δt;
4. Use a linear interpolation to estimate the magnitude
   Magnitude ← Peak_old + (Peak_new-Peak_old)* (t-t_old)/(t_new- t_old));

end

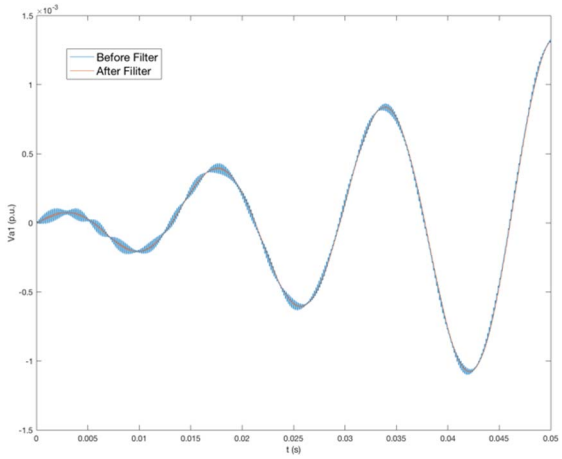


Figure 8. Signal before and after FIR filter.

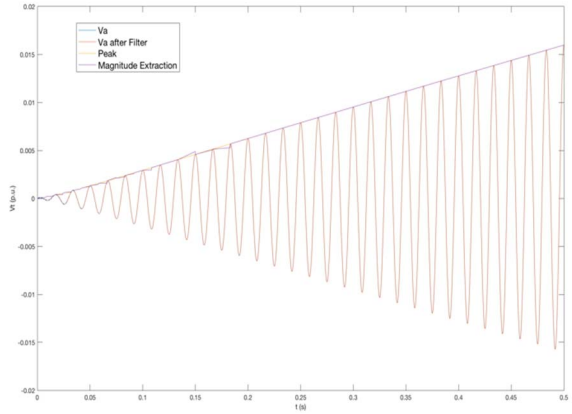


Figure 9. Magnitude extraction result.

Fig. 9 is the result of magnitude extraction with FIR filter. The time step is fixed at 1e-6. As shown in the figure, the magnitude extraction has a quite small error.

4) Transfer Function

With different constant coefficients, all transfer function modules are mapped into one formula (1). The implementation is shown in Fig. 10. In the figure, all coefficients are constants fixed before simulation.

The implementation of exciters uses a parallel scheme where all state variables are updated concurrently using previous and current state variables, while in the traditional scheme state variables are updated sequentially. Instead of using a trapezoidal rule of integration [7] which needs multiple clock cycles, each transfer function block update is done in only one clock cycle.

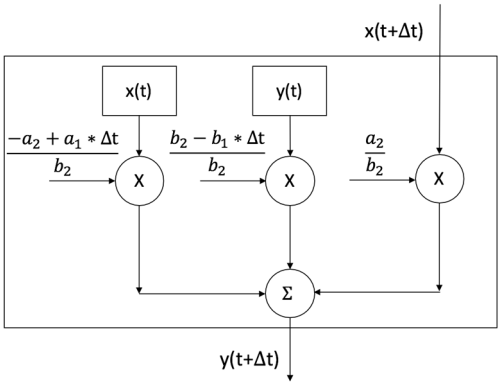


Figure 10. Hardware design of a transfer function.

5) Limiter

In this paper, we use digital comparators to implement the limiter. If the input value is larger than the pre-set upper limitation, output the upper value, else if the input value is less than pre-set lower limitation, output the lower value, else directly output the input value.

6) Saturation Function

In this paper, an exponential approach is used to represent the saturation function in Fig. 2, which is now quite common. The function is shown in (2)

$$S_E = M * e^{N*E_{FD}}, \tag{2}$$
$$M = \frac{S_{e1}}{4\log(S_{e1}/S_{e2})},$$
$$N = \frac{4\log(S_{e1}/S_{e2})}{EVset},$$

where S_{e1}, S_{e2} and $EVset$ are constants.

We use an incremental method to update S_E, which means only the differences between current and previous value is calculated in each iteration.

$$S_{E_{cur}} = M * e^{N*(E_{FD}+\Delta E_{FD})} = S_{E_{pre}} * e^{N*\Delta E_{FD}}$$

Due to ΔE_{FD} is close to zero and N is less than 1, we use Taylor series to approximate the exponential function,

$$e^{N*\Delta E_{FD}} \approx 1 + N * \Delta E_{FD}.$$

7) Initialization

The EMT system parameters such as upper limitation, lower limitation, time constants, voltage references are loaded into the registers at the start of the simulation.

Once the system parameters and initial values are ready, these external data are written into the registers through a scan chain at the initialization.

8) Logic and Layout Synthesis

The system is designed in Verilog HDL. The logic and layout synthesis is done by Synopsis Design Vision and Cadence Encounter. Post-layout timing analysis is performed by Synopsys PrimeTime. The silicon realization is for 45nm technology.

The data width of all variables is 64 bits fixed-point, with 1 bit sign, 31 bits for integer and 32 bits for fraction.

The silicon layout of the exciter is shown in Fig. 11. The entire circuit size is 0.036mm^2. The number of standard cells used in the design is 7968.

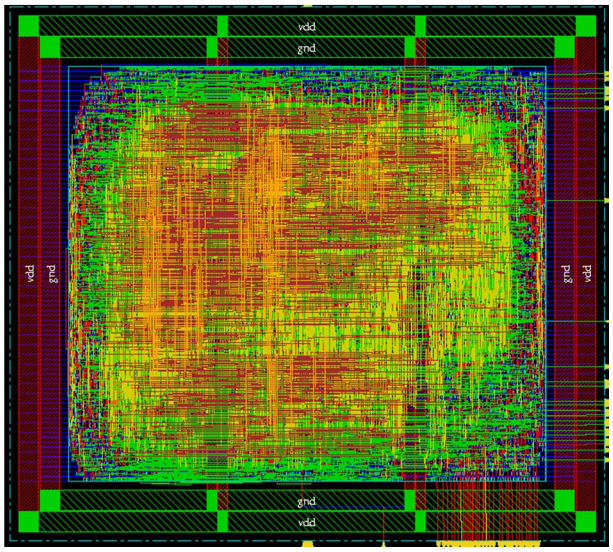


Figure 11. Exciter layout using a 45nm process.

IV. Simulation Results

In the excitation system, the initial values of all variables are 0 and the time step is fixed at 10us. The exciter circuit can simulate each time step of the power system in 8ns, more than 1000 times faster than real time.

The Verilog results compared with MATLAB and Simulink are shown in Fig. 12. The corresponding error between Verilog and MATLAB is shown in Fig. 13. As shown, the error reaches a stable value around 5.5e-4 per unit.

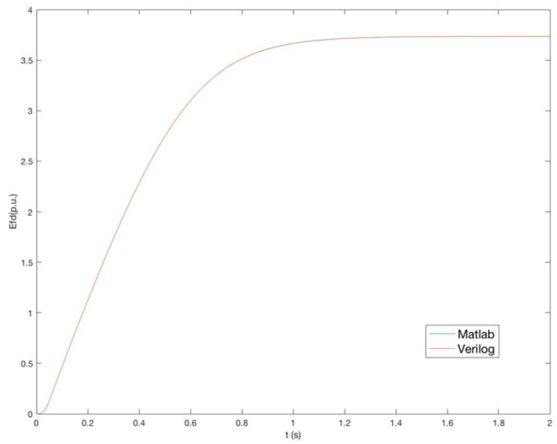


Figure 12. Comparison of E_{FD} for the generator. Our results match exactly with MATLAB reference results.

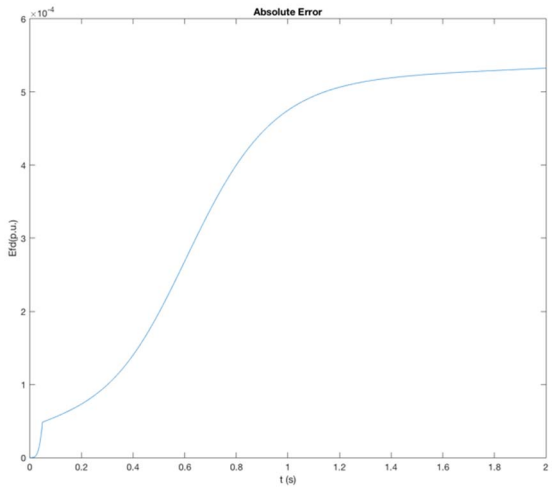


Figure 13. Absolute error of E_{FD} for the generator.

V. Conclusion

In this paper, a customized and parallel VLSI circuit for exciters is developed. Due to the similar representation with exciters, PSS and governors are solved by our approach as well. A fixed time-step approach is utilized. Compared with MATLAB, our proposed simulator is highly accurate, and the error is within 6e-5. With 45nm process technology, our exciter circuit can simulate more than 1000 faster than real time.

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