Design

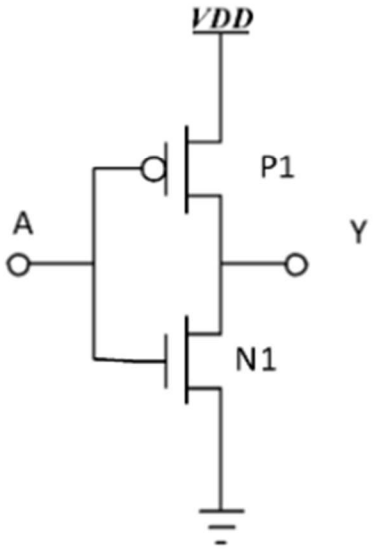


Figure 1: CMOS Inverter Schematic

Euler's Path

PMOS	NMOS
A	A
COMMON PATH: A	

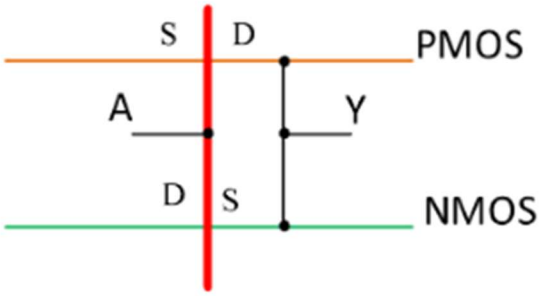


Figure 2: Inverter Stick Diagram

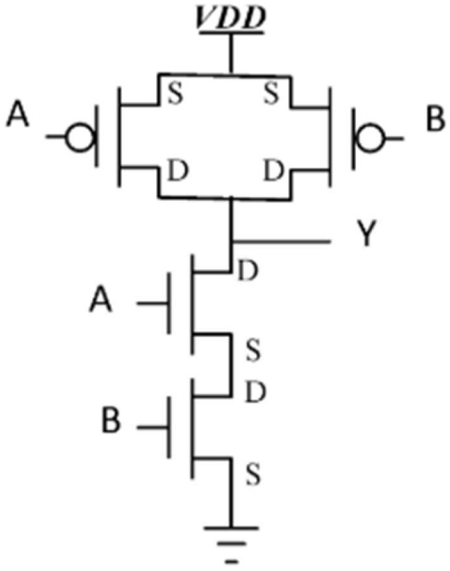


Figure3: 2-input NAND Gate Schematic

Euler's Path	
PMOS	NMOS
A B	A B
COMMON PATH: A – B	

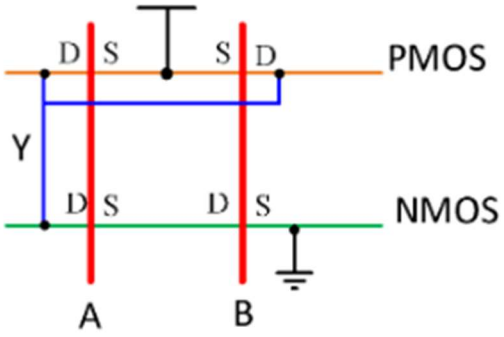
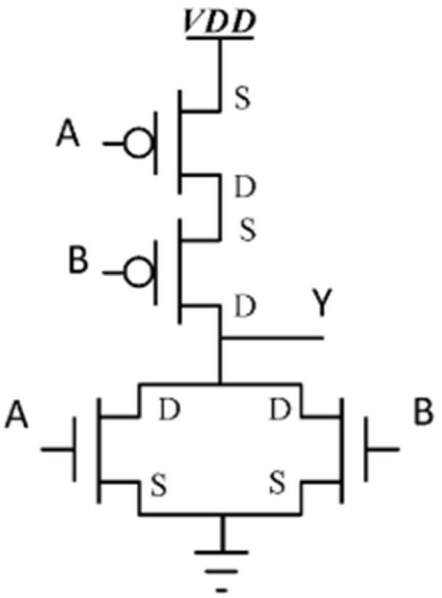
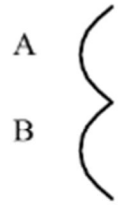
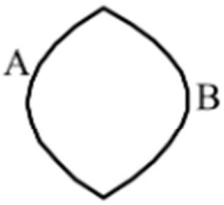
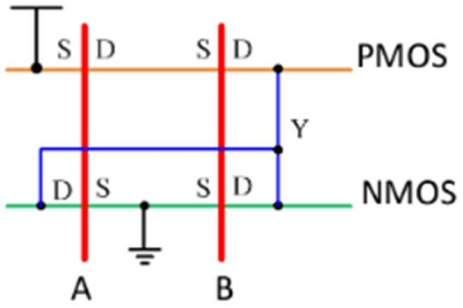


Figure 4: Stick Diagram for 2-input NAND Gate Schematic



Euler's Path	
PMOS	NMOS
	
COMMON PATH: A – B	

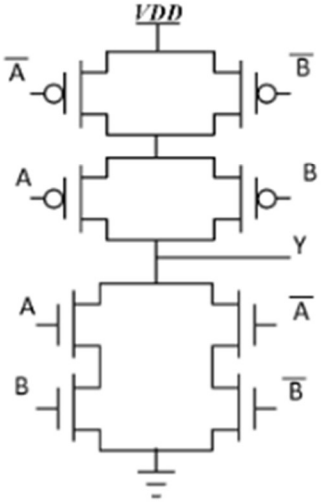


Half Adder

$SUM = A \oplus B = A \oplus \bar{B} = \overline{A}$

$CARRY = AB = A\bar{B} = \overline{\overline{A} +$

SUM



CARRY

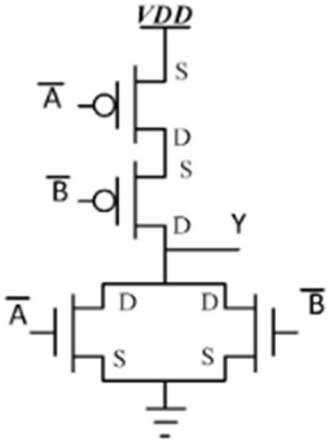
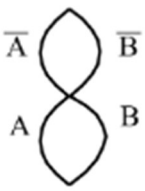


Figure 1: Boolean Equations for 2-input Half-Adder

Figure 2: CMOS Logic for "SUM"

Figure 3: CMOS Logic for "CARRY"

Euler's Path for **SUM** Logic	
PMOS	NMOS
	
COMMON PATH: $A - B - \overline{B} - \overline{A}$	

COMMON PATH: $\overline{B} - \overline{A}$	

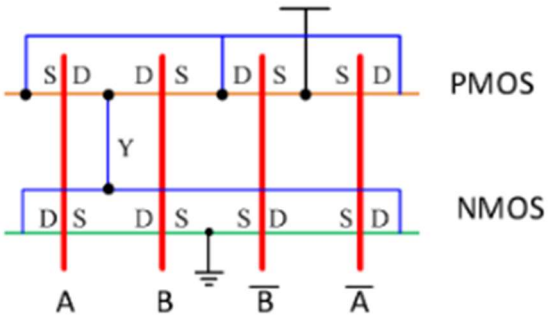
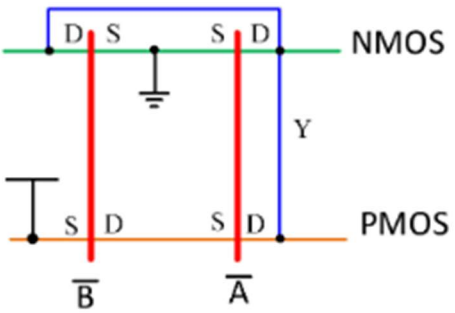
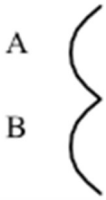
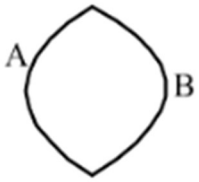

	

Figure 4: Stick Diagram for SUM Logic	*Figure 5: Stick Diagram for CARRY Logic*

Euler's Path for **CARRY** Logic	
PMOS	NMOS
	

Design

1) Using Logic Gates

$$Y = A\cdot\overline{S} + B\cdot S$$

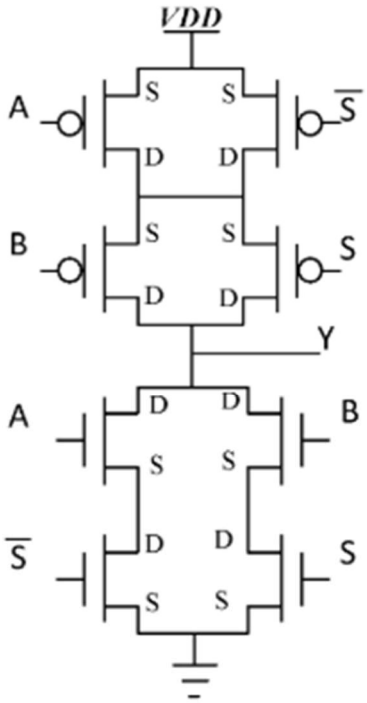


Figure 1: Schematic for 2:1 MUX using Logic Equation

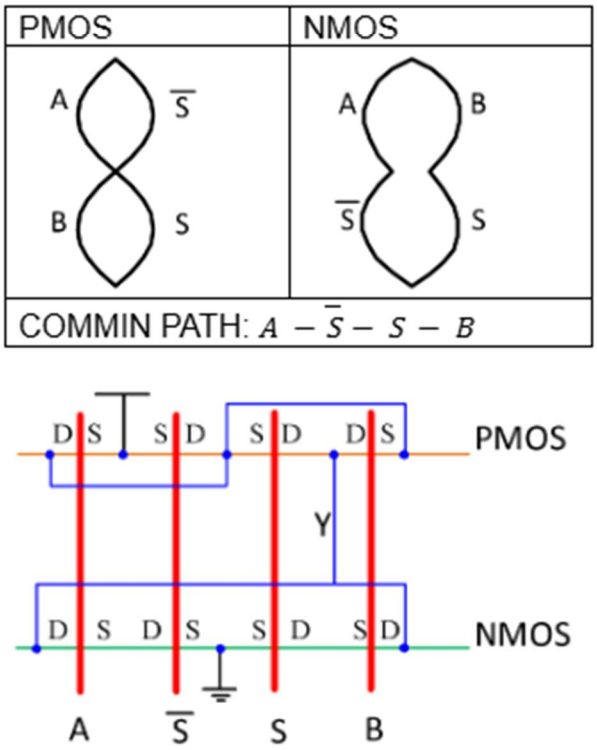


Figure 2: Stick Diagram for 2:1 MUX

2) Using Transmission Gates

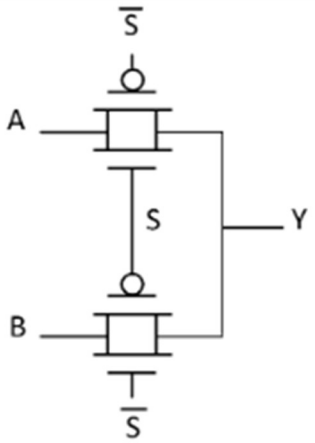


Figure 3 Schematic for 2:1 MUX using Transmission Gates

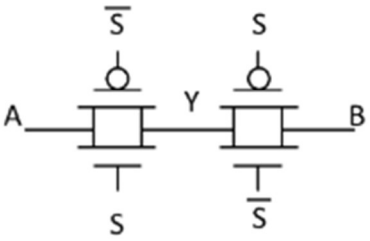


Figure 4 Alternative Form of Figure 18

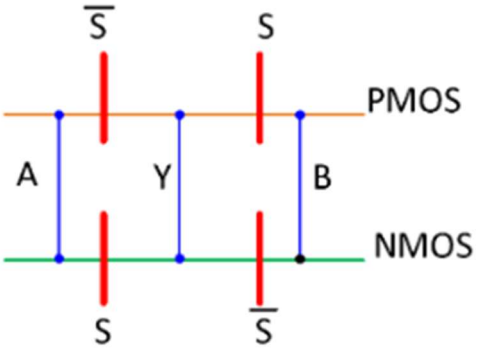


Figure 5 Stick Diagram for 2: 1 MUX