MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

COURSE PLAN

Department	**Computer Science and Engineering**		
Course Name	COMPUTER ORGANIZATION AND ARCHITECTURE	Course Code	CSE 2151
Semester	THIRD	Curriculum	2018
Name of the faculty	SHWETHA RAI	Academic year	2022-23
No. of Contact Hours/Week	L T P C: 3 1 0 4		

COURSE OUTCOMES (CO'S) & COURSE LEARNING OUTCOMES (CLO'S)

At the end of this course, the student should be able to:		**No. of Hours**	**Marks**
CO1	Describe the functionalities of the various units of computers and the instruction set architecture.	10	20
CO2	Appreciate the hardware implementation of addition, subtraction, multiplication, and division and perform arithmetic operations.	7	16
CO3	Design the control unit for simple algorithms.	10	20
CO4	Explain basics of memory system such as cache memories, mapping functions, replacement algorithms and virtual memory concept and design simple memory systems.	10	20
CO5	Outline the I/O handling techniques and realize the improvement in performance using the concepts of pipelining and parallel processing.	11	24
Total hours/ Marks		**48**	**100**

LESSON PLAN

Lecture No.	Topic	CO's addressed
L0	Introductory class(Introduction between teacher & students. Overview of the subject).	-
L1	BASIC STRUCTURE OF COMPUTERS: COMPUTER TYPES, FUNCTIONAL UNITS	CO1
L2	BASIC OPERATIONAL CONCEPTS, NUMBER REPRESENTATION	CO1
L3	ARITHMETIC OPERATIONS	CO1
L4(T1)	Tutorial 1 on Number representation and Arithmetic Operations	CO1
L5	CHARACTER REPRESENTATION, FLOATING POINT REPRESENTATION, IEEE STANDARD FLOATING POINT REPRESENTATION	CO1
L6	FLOATING POINT ARITHMETIC- ADDITION, SUBTRACTION	CO2
L7	FLOATING POINT ARITHMETIC- MULTIPLICATION, DIVISION, GUARD BITS AND TRUNCATION	CO2
L8(T2)	Tutorial 2 on Floating point arithmetic	CO2
L9	INSTRUCTION SET ARCHITECTURE: MEMORY LOCATIONS AND ADDRESSES, MEMORY OPERATIONS	CO1
L10	INSTRUCTIONS AND INSTRUCTION SEQUENCING	CO1
L11	ADDRESSING MODES, CISC INSTRUCTION SETS, RISC AND CISC STYLES	CO1
L12	EXAMPLE PROGRAMS	CO1
L13(T3)	Tutorial 3 on Memory addressing , Addressing modes, RISC and CISC	CO1
L14	ARITHMETIC AND LOGIC UNIT: HARDWARE FOR ADDITION AND SUBTRACTION MULTIPLICATION-HARDWARE IMPLEMENTATION-UNSIGNED MULTIPLICATION	CO2
L15	SIGNED MULTIPLICATION, -BOOTHS ALGORITHM	CO2
L16	DIVISION	CO2
L17(T4)	Tutorial 4 on Addition, Subtraction and Multiplication and Division in ALU	CO2
L18	CONTROL UNIT: BASIC CONCEPTS-REGISTER TRANSFER NOTATION, HARDWARE IMPLEMENTATION, BASIC RWM UNIT, BUSES-BIDIRECTIONAL, SINGLE BUS, 2 BUS, 3 BUS ORGANIZATION	CO3
L19	DESIGN METHODS-COMPARISON OF HARDWIRED AND MICROPROGRAMMED APPROACH, HARDWIRED CONTROL DESIGN-BOOTHS MULTIPLIER DESIGN	CO3
L20	PROCESSING SECTION DESIGN OF BOOTHS MULTIPLIER	CO3
L21(T5)	Tutorial 5 on Processing section Design	CO3
L22	BOOTHS MULTIPLIER CONTROLLER, SEQUENCE COTROLLER DESIGN	CO3

L23	PLA CONTROL UNIT ORGANIZATION OF BOOTH MULTIPLIER	CO3
L24(T6)	Tutorial 6 on Controller Design	CO3
L25	MICROPROGRAMMED CONTROL UNIT:WILKE'S DESIGN, MICROPROGRAMMED CONTROL ORGANIZATION	CO3
L26	MICROPROGRAMMED MULTIPLIER CONTROL UNIT FOR BOOTHS MULTIPLIER	CO3
L27(T7)	Tutorial 7 on Microprogrammed Control Unit	CO3
L28	MEMORY SYSTEMS: BASIC CONCEPTS, RAM MEMORIES, INTERNAL ORGANIZATION OF MEMORY CHIPS	CO4
L29	STRUCTURE OF LARGER MEMORIES, MEMORY HIERARCHY	CO4
L30	CACHE MEMORIES- MAPPING FUNCTIONS	CO4
L31	PLACEMENT STRATEGIES, REPLACEMENT ALGORITHMS	CO4
L32(T8)	Tutorial 8 on Organization of Larger memories, Replacement Algorithms	CO4
L33	EXAMPLE OF MAPPING TECHNIQUES	CO4
L34	PERFORMANCE CONSIDERATIONS, HIT RATE AND MISS PENALTY, CACHES ON THE PROCESSOR CHIP	CO4
L35	VIRTUAL MEMORY, ADDRESS TRANSLATION	CO4
L36(T9)	Tutorial 9 on Mapping functions, Hit rate and Miss penalty, Address translation	CO4
L37	MAGNETIC HARD DISKS	CO4
L38	INPUT/OUTPUT ORGANIZATION: ACCESSING I/O DEVICES, I/O DEVICE INTERFACE, PROGRAM-CONTROLLED I/O, INTERRUPTS, ENABLING AND DISABLING INTERRUPTS	CO5
L39	HANDLING MULTIPLE DEVICES, CONTROLLING I/O DEVICE BEHAVIOR, PROCESSOR CONTROL REGISTERS, DMA	CO5
L40(T10)	Tutorial 10 on Interrupts	CO5
L41	INTRODUCTION TO PARALLEL ARCHITECTURE: PIPELINING CONCEPTS, PIPELINE ORGANIZATION, ISSUES, DATA DEPENDENCIES	CO5
L42	OPERAND FORWARDING, HANDLING DATA DEPENDENCIES IN SOFTWARE, MEMORY DELAYS	CO5
L43	BRANCH DELAYS, UNCONDITIONAL BRANCHES, CONDITIONAL BRANCHES, BRANCH DELAY SLOT	CO5
L44(T11)	Tutorial 11 on Data Dependencies, Branching and Pipelining	CO5
L45	HARDWARE MULTITHREADING, VECTOR (SIMD) PROCESSING	CO5
L46	GRAPHICS PROCESSING UNITS (GPUs), SHARED MEMORY MULTIPROCESSORS, INTERCONNECTION NETWORKS	CO5
L47	CACHE COHERENCE, WRITE-THROUGH PROTOCOL, WRITE-BACK PROTOCOL, SNOOPY CACHES, DIRECTORY BASED CACHE COHERENCE	CO5
L48(T12)	Tutorial 12 on multithreading, SIMD, Multiprocessors, Cache coherence	CO5

References:

References	
1	Carl Hamacher, ZvonkoVranesic and SafwatZaky, “Computer Organization and Embedded Systems”, Sixth edition, McGraw Hill Publication, 2012.
2	William Stallings, “Computer Organization and Architecture – Designing for Performance”, 9th edition, PHI, 2015.
3	Mohammed Rafiquzzaman and Rajan Chandra, “Modern Computer Architecture”, Galgotia Publications Pvt. Ltd., 2010.
4	D.A. Patterson and J.L.Hennessy, "Computer Organization and Design-The Hardware/Software Interface", Fifth Edition, Morgan Kaufmann, 2014.
5	J.P.Hayes, "Computer Architecture and Organization", McGraw Hill Publication, 1998.

Submitted by:
Shwetha Rai

(Signature of the faculty)

Date: 29/07/2022

Approved by:
(Signature of HOD)

Date: 29/07/2022

FACULTY MEMBERS TEACHING THE COURSE (IF MULTIPLE SECTIONS EXIST):

FACULTY NAME	SECTION	FACULTY NAME	SECTION
Ms. Shwetha Rai	A	Ms. Shwetha Rai	C
Dr. N Gopalakrishna Kini	B	Mr. Sivaselvan	D