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MANIPAL INSTITUTE OF TECHNOLOGY
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III SEMESTER B.Tech (COMPUTER SCIENCE AND ENGINEERING) DEGREE
END SEMESTER EXAMINATION—NOV/DEC 2014
SUBJECT: COMPUTER ORGANIZATION AND DESIGN (CSE-201)
DATE: 26-11-2014

TIME: 3 HOURS MAX.MARKS: 50

Instructions to Candidates

- **Note:** Answer any **FIVE** full questions.

1.A. Define the term computer. Write short notes on computer types
1.B. Explain the Program counter relative , Base with index and offset, Auto increment addressing modes with syntax and an example
1.C. Write in detail about the five functionally independent parts of a computer with a neat diagram **(2+3+5)**

2.A. Consider the summation Z=A+B+C+D+E+F+G+H+I where A,B,C,D,E,F,G,H,I are 3-bit 2's complement numbers. The summation is done using carry save addition. Draw the Wallace tree structure for this 9-operand summation and write the formula to calculate the time required to add 9 operands.
2.B. What is the range of values for 4-bit binary format in two's complement system? Take the second smallest negative number and largest positive number from the above range of values in 2's complement form in registers M and Q (4-bit registers) respectively. Multiply them using 4*4 unsigned sequential multiplier. Show your calculations stepwise and compute the final product
2.C. Using a 4-bit parallel adder with inputs A, B, $C_{in,}$ outputs F and C_{out}, one selection bit S_0, design an arithmetic circuit as shown in table Q.2C

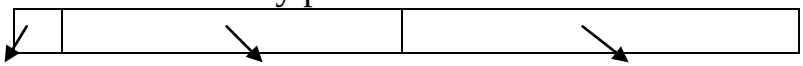
S_0	**Function to be performed**
0	A'+1
1	B plus A

Table Q.2C **(4+4+2)**

3.A. With a neat sketch, explain the 2-bus organization and compute the

number of clock cycles for the operation R0←R0+R1 if this organization is used.

3.B. Consider that the floating point numbers are represented in 19-bit format as shown in Fig.Q.3.B. The 10-bit mantissa is normalized with an implied 1 to left of binary point



1 bit for sign 8 bits for biased exponent 10 bits for mantissa

Fig.Q.3.B

Divide -5.75 by 1.5. Represent the answer (quotient) in the above format in normalized form. Use rounding technique when producing the final normalized 10-bit mantissa for the quotient.

3.C. List any 4 differences between Hardwired and Microprogrammed approach. **(3+5+2)**

4.A. For the register transfer description shown in Fig.Q.4.A, design the processing section and write the description for control points

4.B. Design a Microprogrammed Control unit for the processing section designed in Q.4.A

4.C. Show the memory contents of control memory (ROM address in decimal, Condition Select, Branch Address fields only) in the form of table for the control unit designed in Q.4.B

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Declare registers  M[4], A[4], Q[5], L[2], C[1];
Declare buses  inbus[4], outbus1[4], outbus2[4];

Start:  A<-0, C<-0, M<-inbus, L<-2; clear A, C and transfer M
        Q[4:1]<-inbus, Q[0]<-0; Transfer Q

Loop: If Q[2:0]=001 then goto Add;
      If Q[2:0]=010 then goto Add;
      If Q[2:0]=011 then goto dAdd;
      If Q[2:0]=100 then goto dSub;
      If Q[2:0]=101 then goto Sub;
      If Q[2:0]=110 then goto Sub;
      Goto Rshift

dAdd: A<-A+M;
Add:  A<-A+M;
      C<-Cout; Transfer Cout(carry out) to C
      Goto Rshift

dSub: A<-A-M;
Sub:  A<-A-M;
      C<-Cout;

RShift: ASR(C$A$Q);
        ASR(C$A$Q), L<-L-1;

If L<>0 then goto Loop
outbus1=A, outbus2=Q[4:1];

Halt: Goto Halt
```

Fig.Q.4.A. **(5+3+2)**

5.A. Write in detail about how address translation happens in virtual memory with a neat diagram

5.B. What is Set-Associative mapping? Write one good advantage of this mapping over associative mapping. With an example problem, discuss how number of bits in each of the TAG, SET, WORD fields are determined in a block-set associative cache

5.C. Write short notes on

(i) Flash memory

(ii) RAID levels **(3+3+(2+2))**

6.A. Define the term port. How parallel and serial ports transfer data? With a neat sketch, explain the hardware components needed to connect a keyboard to a processor using input interface

6.B. Discuss in detail the DMA approach with a neat diagram

6.C. Answer the following

. (i) List the steps that are performed when an interrupt occurs

(ii) Describe Priority based interrupt handling using Daisy chain with a neat sketch **(4+3+(1+2))**

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