C, (2e), Cengage Learning India Pvt. Ltd, India , 2009.
2. Tenenbaum Aaron M., Langsam Yedidyah, Augenstein Moshe J., *Data structures using C*, Pearson Prentice Hall of India Ltd., 2007.
3. Debasis Samanta, *Classic Data Structures*, (2e), PHI Learning Pvt. Ltd., India, 2010.

DIGITAL SYSTEM DESIGN
[Revised Credit System]
(Effective from the academic year 2021 onwards)
SEMESTER - III

Subject Code	**CSE_ 2153**	**IA Marks**	**50**
Number of Lecture Hours/Week	**04**	**Exam Marks**	**50**
Total Number of Lecture Hours	**48**	**Exam Hours**	**03**

CREDITS - 04

Course objectives: This course will enable students to

- Understand logic functions and circuits, simplify logical expressions, implement using logic gates, and simulate any logic circuit in Verilog.
- Design and analyze arithmetic, sequential and combinational circuits, relate them to real world applications.
- Understand implementation technology and simple system design.

Module -1	**Teaching Hours**
OVERVIEW OF LOGIC GATES AND BOOLEAN ALGEBRA Brief overview of Logic gates, Truth Tables: AND OR, NOT, NAND, NOR, XOR gates, Sum-of-Products and Product-of-Sums forms, K-Map Simplification, NAND and NOR Implementation, Introduction to Verilog HDL, Incompletely Specified Functions, Fan in, Factoring, Functional decomposition, Multilevel NAND and NOR Circuits. **Text Book 1:** Chapter 2: 2.3, 2.5, 2.6.1, 2.7, 2.10, 2.11-2.14, Chapter 8: 8.1, Appendix A (brief overview of all the topics except Verilog code).	**05 Hours**

Module -2	
ARITHMETIC CIRCUITS Addition of unsigned numbers- Half Adder, Full Adder, Ripple Carry Adder, Signed Numbers – Adder/Subtractor, Arithmetic Overflow, BCD Adder, Fast adder - Carry-Lookahead Adder, Array multiplier, Design of Arithmetic Circuits Using Verilog **Text 1: Ch 3: 3.2 (except 3.2.3), 3.3.3, 3.3.5, 3.4, 3.5 (except3.5.1), 3.6.1, 3.7.3**	**07 Hours**
Module – 3	
COMBINATIONAL CIRCUIT BUILDING BLOCKS Multiplexer, Decoder, Encoder, Code converter, Arithmetic comparison circuits, Verilog for Combinational Circuits. **Text 1: Ch 4**	**07 Hours**
Module-4	
SYNCHRONOUS SEQUENTIAL CIRCUITS Flip-Flops, Using Verilog Constructs for Storage Elements, Design of Synchronous Sequential Circuits- state assignment, state reduction, Moore-Mealy machines, design of synchronous counters, Ripple Counters, Registers, Shift Registers, Ring and Johnson Counters, Using Verilog Constructs for Registers and Counters. Algorithmic State Machine (ASM) Charts **Text 1: Ch 5: 5.12 (except 5.12.1), 5.13, 6.1 – 6.3(Selected topics), 6.10** **Text 2: Ch 6 (Selected topics), Ch 7 (up to 7.5)**	**17 Hours**
Module-5	
IMPLEMENTATION TECHNOLOGY Transistor Switches, NMOS, CMOS Logic Gates, Programmable Logic Devices, Noise Margin, Power dissipation, Transmission Gates, Fan-in, Fan-out in logic gates, Tri-state drivers. **Text 1: Selected topics from Appendix B**	**2 Hours**

Module-6

DIGITAL SYSTEM DESIGN	**10 Hours**
Bus Structure, Using Tri-State Drivers to Implement a Bus, Using Multiplexers to Implement a Bus, Verilog Code for Specification of Bus Structures, Simple Processor, A Bit-Counting Circuit. **Text 1: Ch 7: 7.1, 7.2, 7.3**	

Course outcomes:

After studying this course, students will be able to:

1. Explain the operations of basic logic gates and implementation technology, apply k-map to simplify logical expressions, implement and analyse the performance of logic functions in various forms.
2. Design and analyse arithmetic circuits and combinational circuits using multiplexers, encoders, and decoders.
3. Discuss about the types of flip-flops and construct Algorithmic State Machine (ASM) charts
4. Design synchronous and asynchronous sequential circuits for different applications.
5. Design systems like simple processor, bit counting circuit

Text Books:

1. Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design* (3e), Tata McGraw Hill 2014.
2. Morris Mano M., *Digital Design* (2e), PHI Learning 2000.

Reference Books:

1. Donald D. Givone, *Digital Principles and Design*, Tata McGraw Hill 2003.
2. John F. Wakerly, *Digital design - Principles and practice* (4e), Pearson Education, 2013.