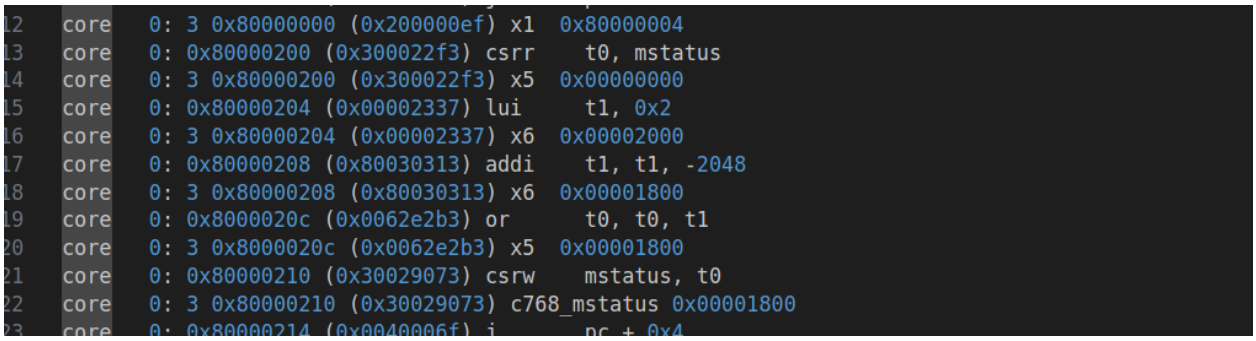
RISC-V arch test
Module: Privileged spec
Task 5

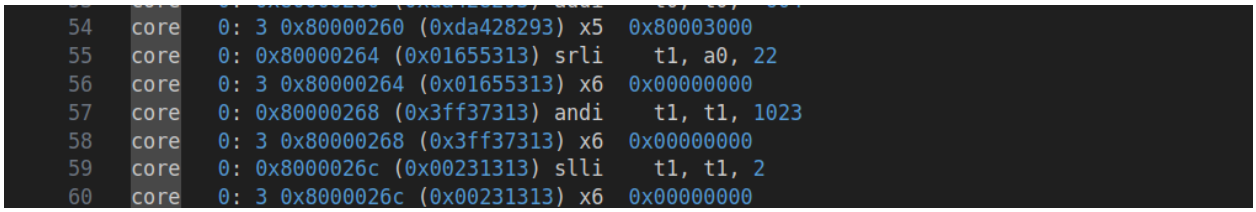
Test Description:

This test is configuring the the virtual memory for risc-v virtual memory mode sv32 in spike. I have enables the translation mechanism of sv 32 by setting the MSB bit of satp register to 1. First I have implemented a function to set up a page table entry “setup_pte”. This function has four arguments: virtual address, physical address, permission bits and level bit. Virtual address is the address to whom we want to map physical address and physical address is the one which maps to virtual address. Set the permission bits for the PTE address and check the behaviour according to the permissions specified while setting the PTE.

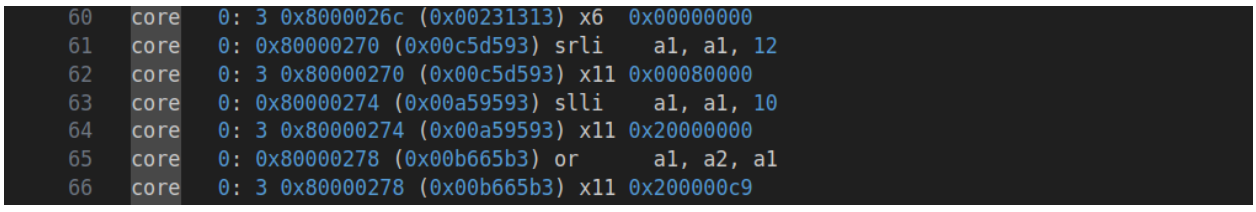
SnapShots:



Starting the test in Machine mode



Extract the VPN1, by discarding the offset bits by shifting it to the right by 22 bits and then and that with 0x3ff to get only 10 bits as VPN is of 10 bits



Extract the physical page number from physical address and add the permission bits

```
core   0: 0x80000278 (0x00b665b3) or      a1, a2, a1
core   0: 3 0x80000278 (0x00b665b3) x11 0x200000c9
core   0: 0x8000027c (0x006282b3) add     t0, t0, t1
core   0: 3 0x8000027c (0x006282b3) x5  0x80003000
core   0: 0x80000280 (0x00b2a023) sw      a1, 0(t0)
core   0: 3 0x80000280 (0x00b2a023) mem 0x80003000 0x200000c9
core   0: 0x80000284 (0x00008067) ret
```

Calculated the PTE address by adding the base page table address with the address calculated using VPN and stored the PPN and permission bits to the PTE address

```
core   0: 0x80000230 (0x00004297) auipc   t0, 0x4
core   0: 3 0x80000230 (0x00004297) x5  0x80004230
core   0: 0x80000234 (0xdd028293) addi    t0, t0, -560
core   0: 3 0x80000234 (0xdd028293) x5  0x80004000
core   0: 0x80000238 (0x00c55313) srli    t1, a0, 12
core   0: 3 0x80000238 (0x00c55313) x6  0x00000000
core   0: 0x8000023c (0x3ff37313) andi    t1, t1, 1023
core   0: 3 0x8000023c (0x3ff37313) x6  0x00000000
core   0: 0x80000240 (0x00231313) slli    t1, t1, 2
core   0: 3 0x80000240 (0x00231313) x6  0x00000000
core   0: 0x80000244 (0x00c5d593) srli    a1, a1, 12
core   0: 3 0x80000244 (0x00c5d593) x11 0x00080000
core   0: 0x80000248 (0x00a59593) slli    a1, a1, 10
core   0: 3 0x80000248 (0x00a59593) x11 0x20000000
core   0: 0x8000024c (0x00b665b3) or      a1, a2, a1
core   0: 3 0x8000024c (0x00b665b3) x11 0x200000c3
core   0: 0x80000250 (0x006282b3) add     t0, t0, t1
core   0: 3 0x80000250 (0x006282b3) x5  0x80004000
core   0: 0x80000254 (0x00b2a023) sw      a1, 0(t0)
core   0: 3 0x80000254 (0x00b2a023) mem 0x80004000 0x200000c3
```

Set up the PTE for level 0, by calculating the address for PTE using base address and address calculated using VPN and then stored the PPN on that PTE

```
core   0: 3 0x80000258 (0x00008067)
core   0: 0x80000038 (0x00003297) auipc   t0, 0x3
core   0: 3 0x80000038 (0x00003297) x5  0x80003038
core   0: 0x8000003c (0xfc828293) addi    t0, t0, -56
core   0: 3 0x8000003c (0xfc828293) x5  0x80003000
core   0: 0x80000040 (0x00c2d293) srli    t0, t0, 12
core   0: 3 0x80000040 (0x00c2d293) x5  0x00080003
core   0: 0x80000044 (0x80000337) lui     t1, 0x80000
core   0: 3 0x80000044 (0x80000337) x6  0x80000000
core   0: 0x80000048 (0x0062e2b3) or      t0, t0, t1
core   0: 3 0x80000048 (0x0062e2b3) x5  0x80080003
core   0: 0x8000004c (0x18029073) csrw    satp, t0
core   0: 3 0x8000004c (0x18029073) c384_satp 0x80080003
```

Enable sv32 translation mechanism by setting the MSB of satp register to 1

```
135   core   0: 0x8000006c (0x300022f3) csrr    t0, mstatus
136   core   0: 3 0x8000006c (0x300022f3) x5  0x00001800
137   core   0: 0x80000070 (0xffffe337) lui     t1, 0xffffe
138   core   0: 3 0x80000070 (0xffffe337) x6  0xffffe000
139   core   0: 0x80000074 (0x7ff30313) addi    t1, t1, 2047
140   core   0: 3 0x80000074 (0x7ff30313) x6  0xffffe7ff
141   core   0: 0x80000078 (0x0062f2b3) and     t0, t0, t1
142   core   0: 3 0x80000078 (0x0062f2b3) x5  0x00000000
143   core   0: 0x8000007c (0x00001337) lui     t1, 0x1
144   core   0: 3 0x8000007c (0x00001337) x6  0x00001000
145   core   0: 0x80000080 (0x80030313) addi    t1, t1, -2048
146   core   0: 3 0x80000080 (0x80030313) x6  0x00000800
147   core   0: 0x80000084 (0x0062e2b3) or      t0, t0, t1
148   core   0: 3 0x80000084 (0x0062e2b3) x5  0x00000800
149   core   0: 0x80000088 (0x30029073) csrw    mstatus, t0
150   core   0: 3 0x80000088 (0x30029073) c768_mstatus 0x00000800
```

Switch to supervisor mode

```
151   core   0: 0x8000008c (0x30200073) mret
152   core   0: 3 0x8000008c (0x30200073) c784_mstatush 0x00000000 c768_mstatus 0x00000080
153   core   0: 0x00000090 (0x00005697) auipc   a3, 0x5
154   core   0: 1 0x00000090 (0x00005697) x13 0x00005090
155   core   0: 0x00000094 (0xf7068693) addi    a3, a3, -144
156   core   0: 1 0x00000094 (0xf7068693) x13 0x00005000
157   core   0: 0x00000098 (0x0006a303) lw      t1, 0(a3)
158   core   0: exception trap_load_page_fault, epc 0x00000098
159   core   0:           tval 0x00005000
```

Load page fault because permission are not set for read in PTE

Reference:

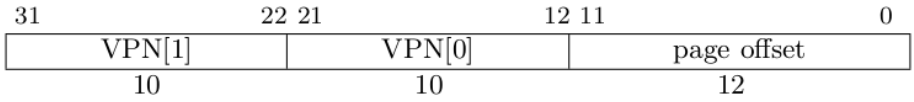


Figure 4.16: Sv32 virtual address.

Got the VPN by using this virtual address specifications

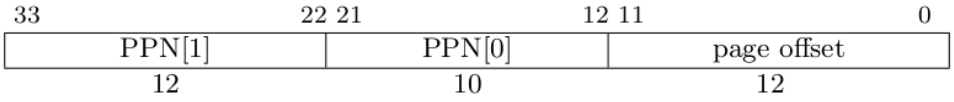


Figure 4.17: Sv32 physical address.

Got the PPN to be stored in PTE using this physical address specifications

Figure 4.17: Sv32 physical address.

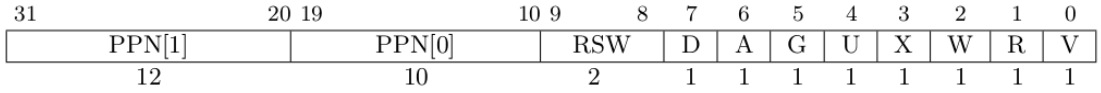


Figure 4.18: Sv32 page table entry.

Setup the complete PTE using this

X	W	R	Meaning
0	0	0	Pointer to next level of page table.
0	0	1	Read-only page.
0	1	0	*Reserved for future use.*
0	1	1	Read-write page.
1	0	0	Execute-only page.
1	0	1	Read-execute page.
1	1	0	*Reserved for future use.*
1	1	1	Read-write-execute page.

Table 4.5: Encoding of PTE R/W/X fields.

Permissions encoding for PTE