RISC-V arch test
Module: Privileged spec
Task 3

Test Description:

This test sets up the trap handler and stores the address of trap handler in stvec register and delegates the exceptions to s mode. Then sets the mstaus register to move to the user mode and then jumps to the user mode where there is an illegal instruction and so the exception will be raised and since trap handler has been set to the supervisor mode the exception will be handled in supervisor mode.

Snapshots:

```
0: 0x0000000080001030 (0x00000297) auipc   t0, 0x0
0: 3 0x0000000080001030 (0x00000297) x5  0x0000000080001030
0: 0x0000000080001034 (0x01028293) addi    t0, t0, 16
0: 3 0x0000000080001034 (0x01028293) x5  0x0000000080001040
0: 0x0000000080001038 (0x34129073) csrw    mepc, t0
0: 3 0x0000000080001038 (0x34129073) c833_mepc 0x0000000080001040
0: 0x000000008000103c (0x30200073) mret
0: 3 0x000000008000103c (0x30200073) c768_mstatus 0x0000000a00000080
0: >>>>  switch_to_machine
0: 0x0000000080001040 (0x00008067) ret
0: 3 0x0000000080001040 (0x00008067)
0: 0x0000000080001004 (0x00000297) auipc   t0, 0x0
0: 3 0x0000000080001004 (0x00000297) x5  0x0000000080001004
0: 0x0000000080001008 (0x04028293) addi    t0, t0, 64
0: 3 0x0000000080001008 (0x04028293) x5  0x0000000080001044
0: 0x000000008000100c (0x10529073) csrw    stvec, t0
0: 3 0x000000008000100c (0x10529073) c261_stvec 0x0000000080001044
0: 0x0000000080001010 (0x00400293) li      t0, 4
0: 3 0x0000000080001010 (0x00400293) x5  0x0000000000000004
0: 0x0000000080001014 (0x30229073) csrw    medeleg, t0
0: 3 0x0000000080001014 (0x30229073) c770_medeleg 0x0000000000000004
0: 0x0000000080001018 (0x0500006f) j       pc + 0x50
```

Start in Machine

```
0: 3 0x000000008000100c (0x10529073) c261_stvec 0x0000000080001044
0: 0x0000000080001010 (0x00400293) li      t0, 4
0: 3 0x0000000080001010 (0x00400293) x5  0x0000000000000004
0: 0x0000000080001014 (0x30229073) csrw    medeleg, t0
0: 3 0x0000000080001014 (0x30229073) c770_medeleg 0x0000000000000004
0: 0x0000000080001018 (0x0500006f) j       pc + 0x50
0: 3 0x0000000080001018 (0x0500006f)
0: >>>>  switch
0: 0x0000000080001068 (0x300022f3) csrr    t0, mstatus
```

Added the address of trap handler in stvec and delegated the exception for illegal instr to s mode using medeleg register

```
7 core   0: 0x0000000080001018 (0x00000293) li      t0, 0
8 core   0: 3 0x0000000080001018 (0x00000293) x5  0x0000000000000000
9 core   0: 0x000000008000101c (0x30029073) csrw    mstatus, t0
0 core   0: 3 0x000000008000101c (0x30029073) c768_mstatus 0x0000000a00000000
1 core   0: 0x0000000080001020 (0x00000297) auipc   t0, 0x0
2 core   0: 3 0x0000000080001020 (0x00000297) x5  0x0000000080001020
3 core   0: 0x0000000080001024 (0x01028293) addi    t0, t0, 16
4 core   0: 3 0x0000000080001024 (0x01028293) x5  0x0000000080001030
5 core   0: 0x0000000080001028 (0x34129073) csrw    mepc, t0
6 core   0: 3 0x0000000080001028 (0x34129073) c833_mepc 0x0000000080001030
7 core   0: 0x000000008000102c (0x30200073) mret
8 core   0: 3 0x000000008000102c (0x30200073) c768_mstatus 0x0000000a00000080
9 core   0: >>>>  $d
```

Sets the mstatus to be in user mode and moved to the user mode using mret

```
re   0: 3 0x0000000080001084 (0x34129073) c833_mepc 0x000000008000108c
re   0: 0x0000000080001088 (0x30200073) mret
re   0: 3 0x0000000080001088 (0x30200073) c768_mstatus 0x0000000a00000088
re   0: >>>>  user_mode_start
re   0: 0x000000008000108c (0x30200073) mret
re   0: exception trap_illegal_instruction, epc 0x000000008000108c
re   0:           tval 0x0000000030200073
re   0: >>>>  trap_handler
re   0: 0x0000000080001044 (0x142022f3) csrr    t0, scause
re   0: 1 0x0000000080001044 (0x142022f3) x5  0x0000000000000002
re   0: 0x0000000080001048 (0x14102373) csrr    t1, sepc
```

Illegal instruction exception in user mode

```
7 core   0: >>>>  trap_handler
8 core   0: 0x0000000080001048 (0x142022f3) csrr    t0, scause
9 core   0: 1 0x0000000080001048 (0x142022f3) x5  0x0000000000000002
0 core   0: 0x000000008000104c (0x14102373) csrr    t1, sepc
1 core   0: 1 0x000000008000104c (0x14102373) x6  0x0000000080001030
2 core   0: 0x0000000080001050 (0x00200393) li      t2, 2
3 core   0: 1 0x0000000080001050 (0x00200393) x7  0x0000000000000002
4 core   0: 0x0000000080001054 (0x00728463) beq     t0, t2, pc + 8
5 core   0: 1 0x0000000080001054 (0x00728463)
6 core   0: >>>>  handle_illegal_instruction
7 core   0: 0x000000008000105c (0x00100513) li      a0, 1
8 core   0: 1 0x000000008000105c (0x00100513) x10 0x0000000000000001
9 core   0: 0x0000000080001060 (0x00430313) addi    t1, t1, 4
0 core   0: 1 0x0000000080001060 (0x00430313) x6  0x0000000080001034
1 core   0: 0x0000000080001064 (0x14131073) csrw    sepc, t1
2 core   0: 1 0x0000000080001064 (0x14131073) c321_sepc 0x0000000080001034
3 core   0: 0x0000000080001068 (0x0040006f) j       pc + 0x4
4 core   0: 1 0x0000000080001068 (0x0040006f)
```

Trap handler in supervisor mode

```
9 core   0: 1 0x0000000080001068 (0x0040006f)
0 core   0: >>>>  trap_exit
1 core   0: 0x000000008000106c (0x10200073) sret
2 core   0: 1 0x000000008000106c (0x10200073) c768_mstatus 0x0000000a000000a0
3 core   0: >>>>  $x
4 core   0: 0x0000000080001034 (0x00a00513) li      a0, 10
```

Move out of supervisor mode trap handler using sret