Group members:

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List of control units:
For part1 we sent funsel and enable inputs to the register function and observe how to output changes according to them.

For part2a, for the clear test we sent, Enable input as 1, LH input as 0 and funsel 11 and observed that 16 bit IR register functions' output is cleared.
Also we tested the incrementation and decrementations by changing funsel and by changing LH input we checked if input puts in the right place of output or not.

For part2b, we used the same funsel in part2a and changed it to observe if it is increments or decrements, we also changed the regsel and tsel inputs to enable different registers.

For part2c, we changed the o1sel and o2sel to choose different registers and used the same funsel to change the output.

For part3, we first used a 4:16 decoder to perform 16 different operations those that defined in pdf. We changed the A, B inputs and operations and observed the flags that are on.

For part4, we implemented the circuit that's In the pdf by connecting the previous parts' modules and memory with using the appropriate multiplexers. We tried to observe how the system changes by changing the inputs.

Distribution:
Onur attended the meetings but he couldn't help much because he didn't know much Verilog. In general Ömer and I wrote the code.