SBC-RK3568-NXP1024-ARK-L2

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Revisioc History

Rev.Code	Date	By	Check	Description
V1.0	2022-11-08	HYR		Initial Version

PWB1
YYBAGG30R1

Title: 01.COVER	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd Wuke East Street, Wuhou District ,ChengDu , China 86-28-8512-3930	
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		Rev: 1.0>
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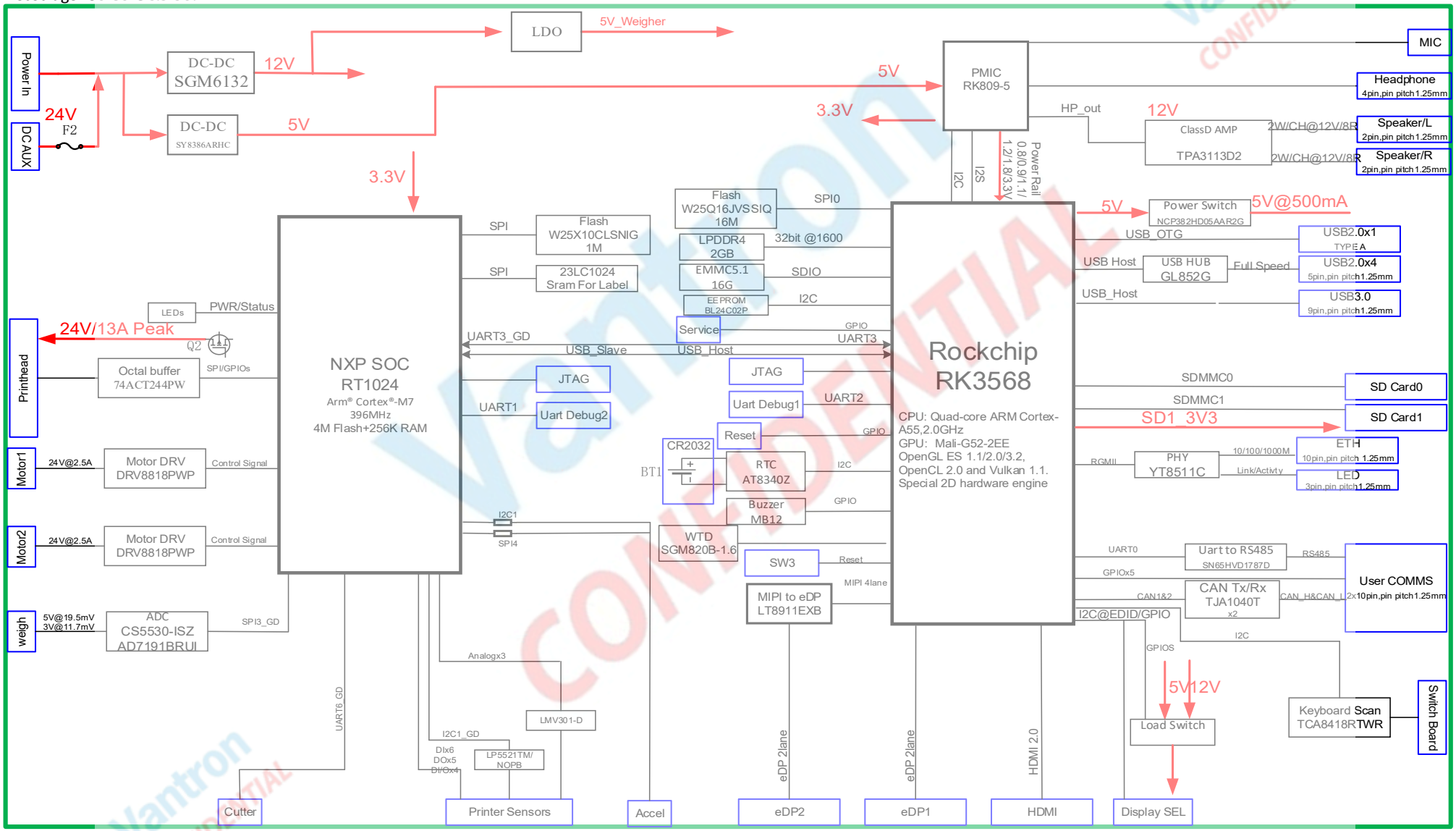
VT-SBC-RK3568-ARK_
Operating: -10-60℃&5-90%RH
Stotrage:-30-80℃&5-90%RH

: PCBA : IC : Connector



Title: 02.Block Diagram		Vantron	ChengDu Vantron Technology.LTD 6th Floor, 1st Building,No.5, 3rd Wuke East Street, Wuhou District ,ChengDu , China 86-28-8512-3930
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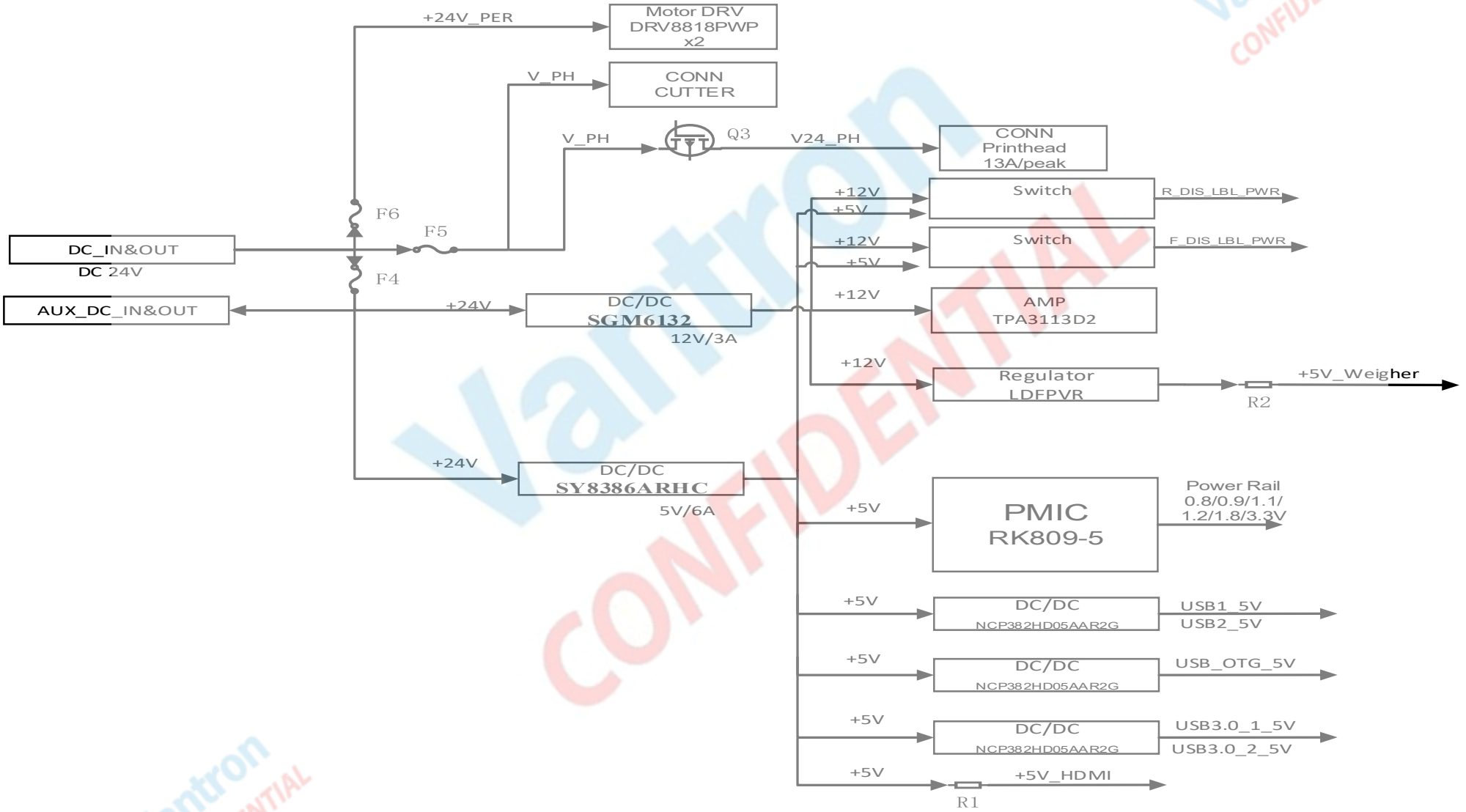
VT-SBC-RK3568-ARK_



Title: 03.Power Tree	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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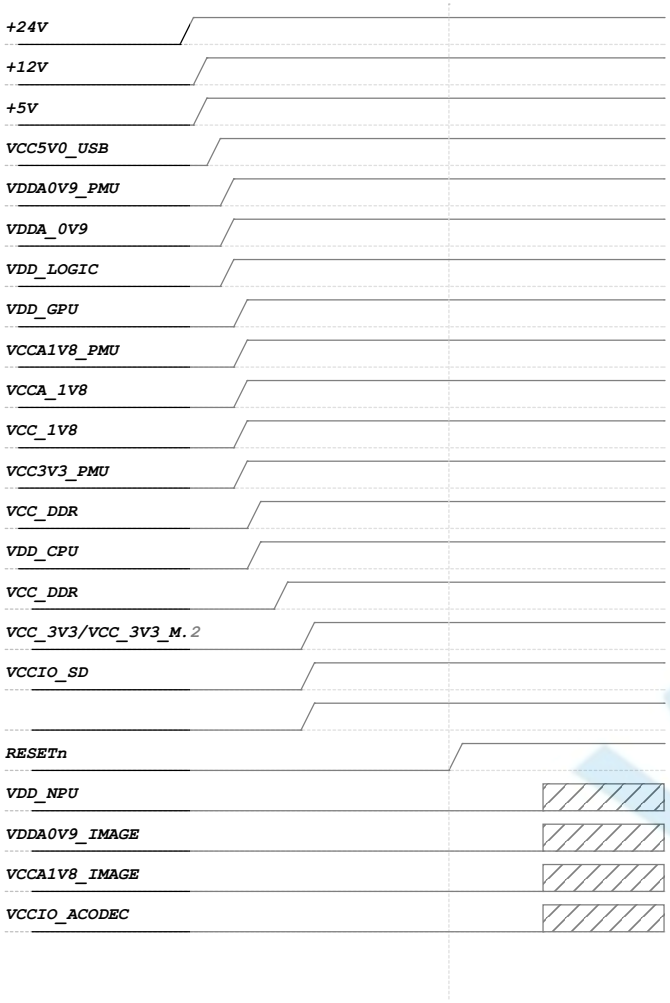
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
+5V	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
+5V	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
+5V	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.1V (DDR4X)	TBD	TBD
+5V	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
+5V	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
+5V	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
+5V	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
+5V	RK809_SW2	2.1A	VCC_3V3_M.2	Slot:4	3.3V	ON	3.3V		
+5V	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
+24V	EXT BUCK	3.0A	+12V	Slot:0	12V	ON	12V	TBD	TBD
+24V	EXT BUCK	3.0A	+5V	Slot:0	5.0V	ON	5.0V	TBD	TBD
+5V	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD

Title: 04.Power Sequence	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
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IO Power Domain Map

If IO domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

IO Domain	Pin Num	Support IO Voltage		Notes	Default IO Domain Voltage		
		3.3V	1.8V		Supply Power Net Name	Power Source	Voltage
PMUIO0 (PMUPLL_AVDD_1V8)	Pin Y21	✗	✓	PMUIO0 are fixed 1.8V level mode, which cannot be configured.	VCCA1V8_PMU	VCCA1V8_PMU	1.8V
PMUIO1	Pin Y20	✓	✗	PMUIO1 are fixed 3.3V level mode, which cannot be configured.	VCC3V3_PMU	VCC3V3_PMU	3.3V
PMUIO2	Pin W19	✓	✓	PMUIO2 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC3V3_PMU	VCC3V3_PMU	3.3V
VCCIO1	Pin H17	✓	✓	VCCIO1 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO_ACODEC	VCCIO_ACODEC	3.3V
VCCIO2	Pin H18	✓	✓	VCCIO2 supports 1.8V or 3.3V level mode Default is configured by hardware,namely PIN "FLASH_VOL_SEL" state determines which mode to work in.[1][2]	VCCIO_FLASH	VCC_1V8	1.8V
VCCIO3	Pin L22	✓	✓	VCCIO3 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2][3]	VCCIO_SD	VCCIO_SD	3.3V
VCCIO4	Pin J21	✓	✓	VCCIO4 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO4	VCCIO_SD	3.3V
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO6	VCC_3V3	3.3V
VCCIO7	Pin V12	✓	✓	VCCIO7 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO7	VCC_1V8	1.8V

*For example, **the VCCIO4 hardware has been modified to 3.3V power supply, and the corresponding DTS must be modified to 3.3V configuration, otherwise the IO of VCCIO4 will be damaged.***

If a board needs to be compatible with two voltage choices, recommended to enable BOM ID

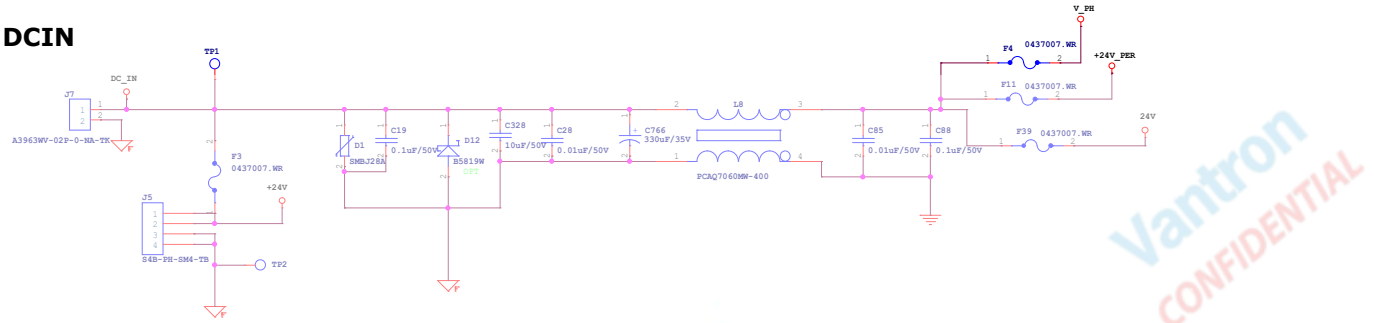
Notes

[1]:When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

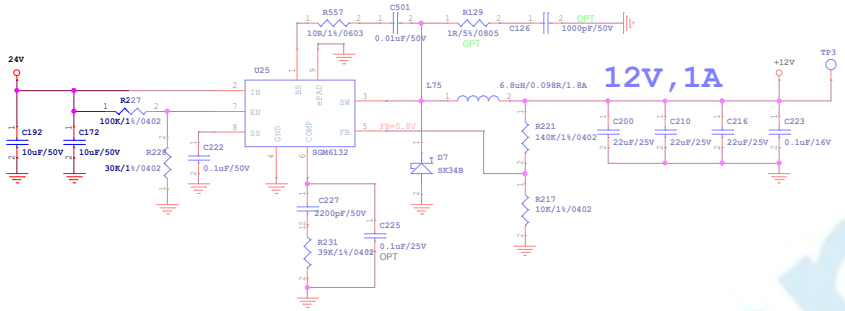
[2]:When the IO domain power supply voltage is 1.8V, the IO domain voltage configuration in DTS must be set to 1.8V mode.
If it is misconfigured to 3.3V mode, the IO function of this power domain will be abnormally;
When the IO domain power supply voltage is 3.3V, the IO domain voltage configuration in DTS must be set to 3.3V mode.
If it is misconfigured to 1.8V mode, the IO in this power domain will be in overvoltage state, and the IO will be damaged after long-term operation.

[3]:When VCCIO3 IO domain is assigned as SD card function,:
If SD3.0 mode is to be supported, VCCIO3 power supply voltage must be support configurable, 3.3V in SD2.0 mode and 1.8V in SD3.0 mode.
If only SD2.0 mode is supported (SD3.0 card only works in SD2.0 mode), VCCIO3 only needs fixed power supply of 3.3V.
When VCCIO3 IO domain is assigned as other function,:
Such as uart5 and uart6, then note [2] should be followed

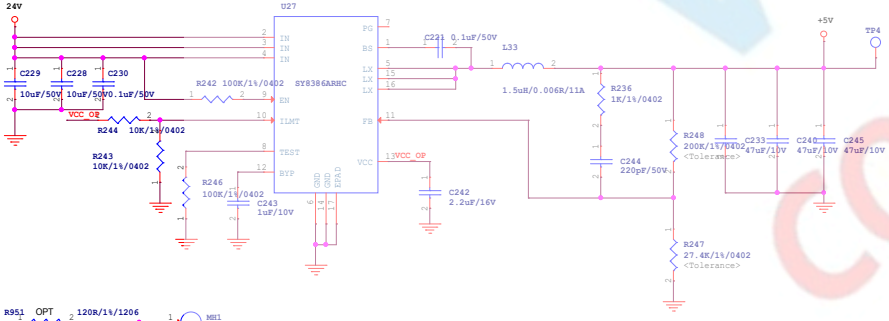
24V DCIN

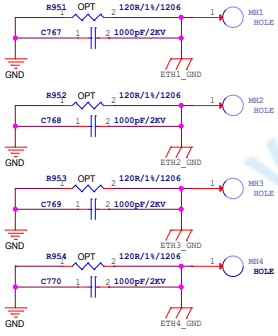


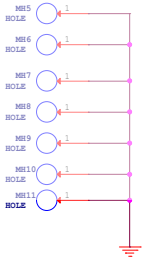
24V DC to 12V DC



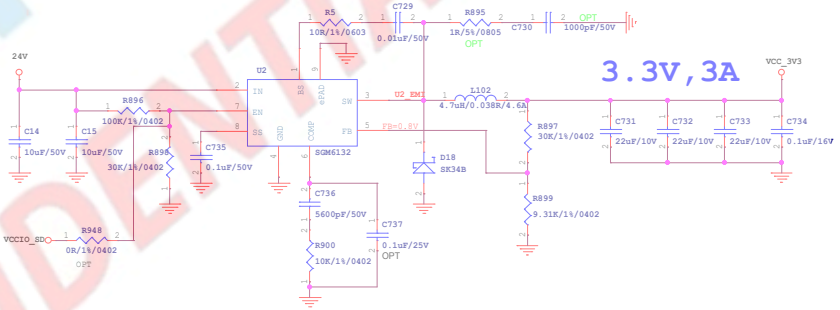
24V DC to 5V DC



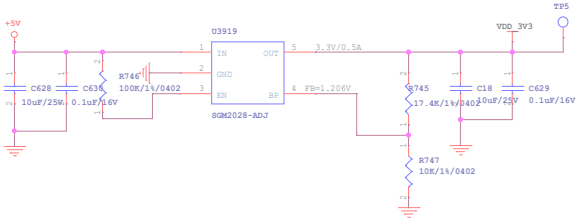




24V DC to 3.3V DC



LDO



Title: 06.Power_DC IN	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.5, 3rd Wuke East Street, Wuhou District ,ChengDu , China 86-28-6512-3930	
Size: C	Document Number: 640BBAGG3R121 SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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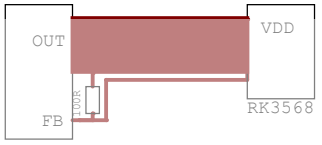
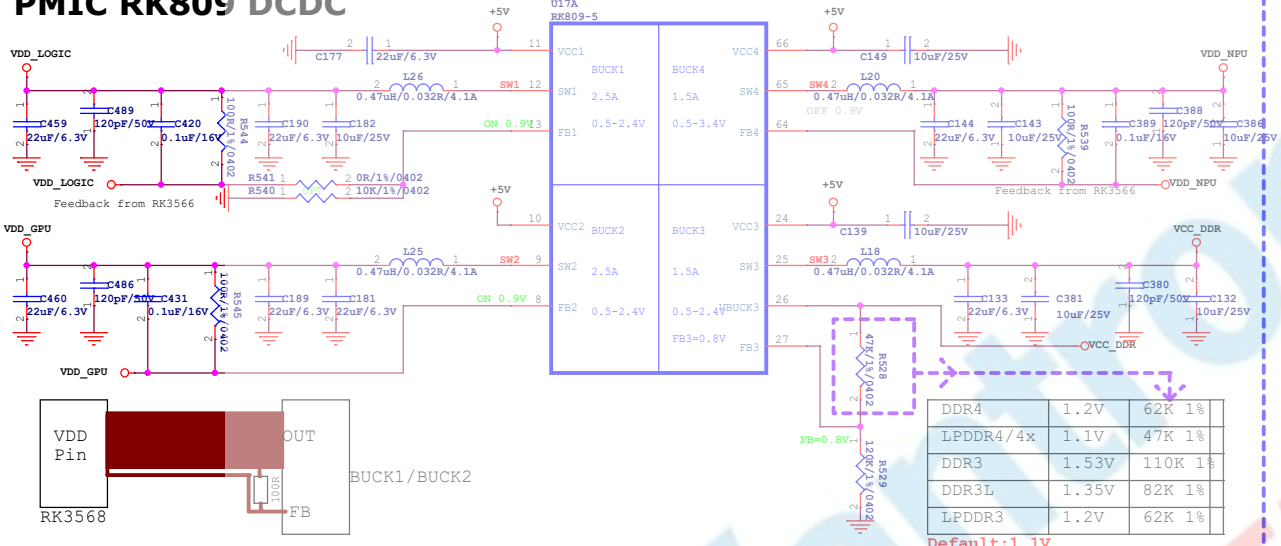
I2C0_SCL_PMIC [8,12]
I2C0_SDA_PMIC [8,12]
PMIC_INT_L [12]
PMIC_SLEEP_H [8,12]
RESETn [12,38,39]
RK809_PWRON [38]
I2S1_MCLK_M0_RK809 [19]
I2S1_SCLK_TX_M0_RK809 [19]
I2S1_LRCK_TX_M0_RK809 [19]
I2S1_SDO0_M0_RK809 [19]
I2S1_SDI0_M0/PDM_SDI0_M0_RK809 [19]
PDM_CLK0_M0_RK809 [19]
HPL_OUT [41]
HP_SNS [41]
HPR_OUT [41]
MIC1_INN [41]
MIC1_INP [41]
PMIC_32KOUT_WIFI [7]

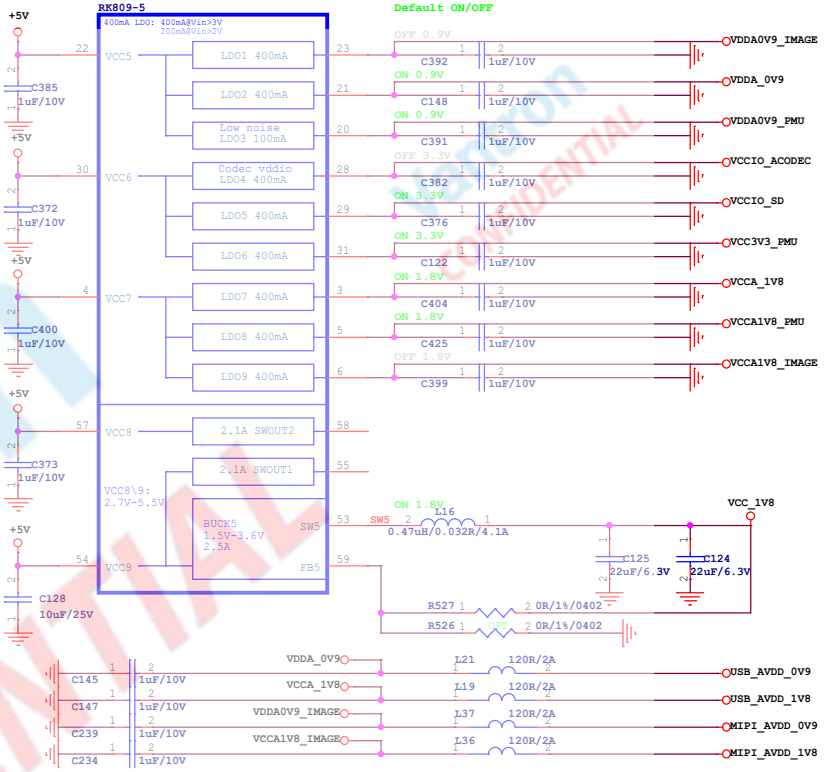


PMIC RK809 DCDC

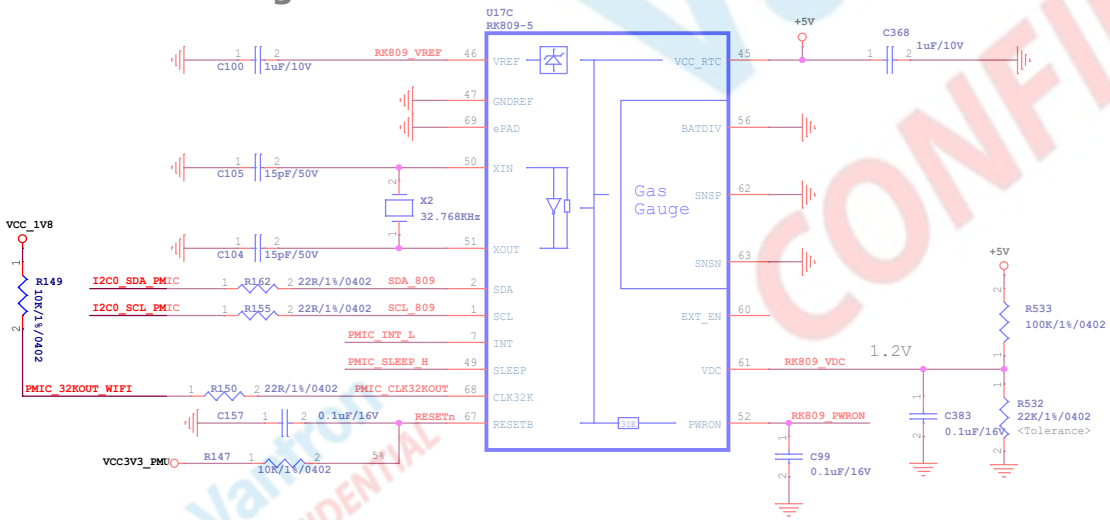


DDR4	1.2V	62K 1%
LPDDR4/4x	1.1V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.2V	62K 1%

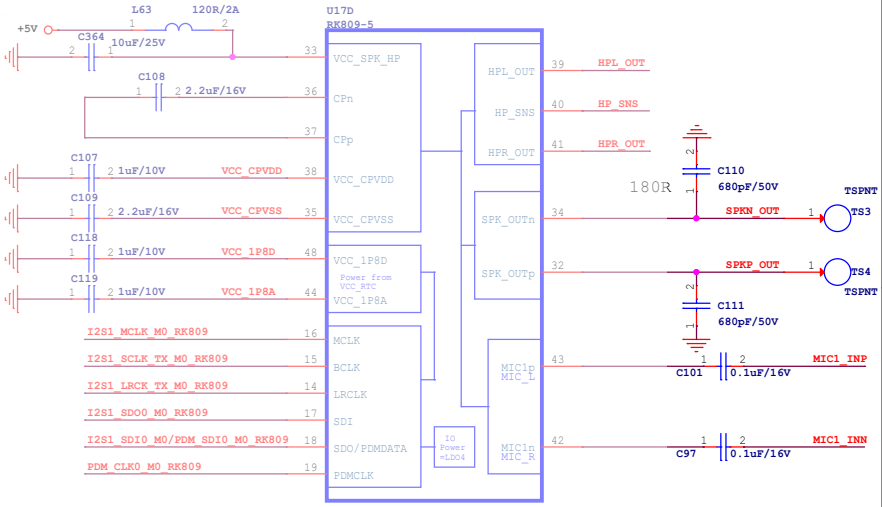
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC



Note:

If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

Title	07.Power_PMIC	Vantron	ChengDu Vantron Technology,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
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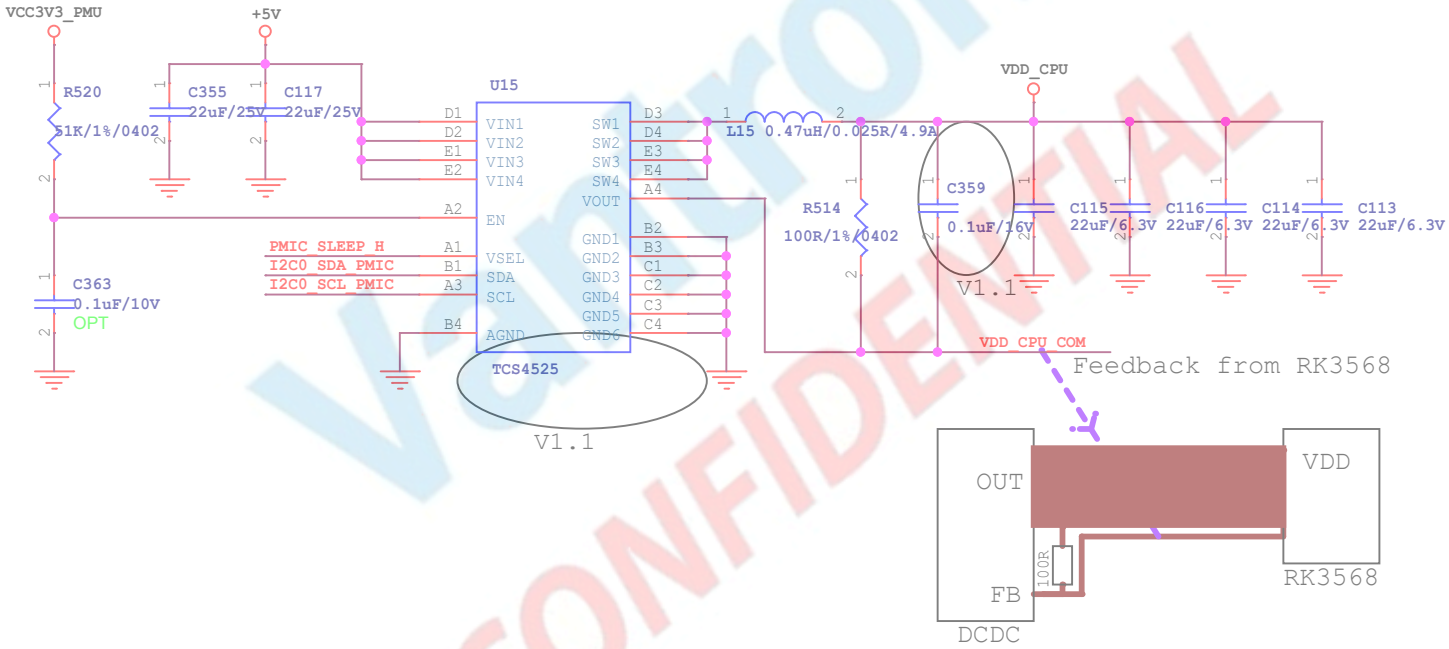
I2C0_SCL_PMIC [7,12]
I2C0_SDA_PMIC [7,12]
PMIC_SLEEP_H [7,12]
VDD_CPU_COM [10]

VDD_CPU



Title: 08.Power_VDD_CPU	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
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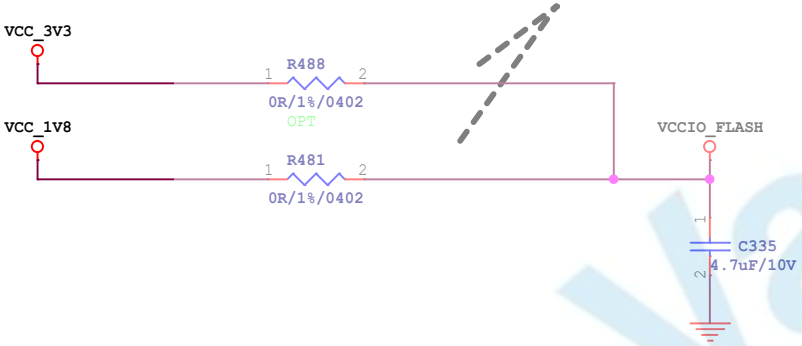
FLASH_VOL_SEL [12]

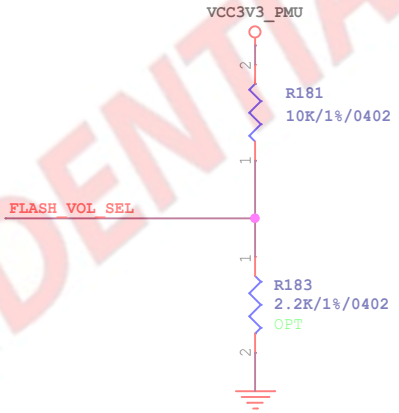
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

Title: 09.Power_Flash Power Manage	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
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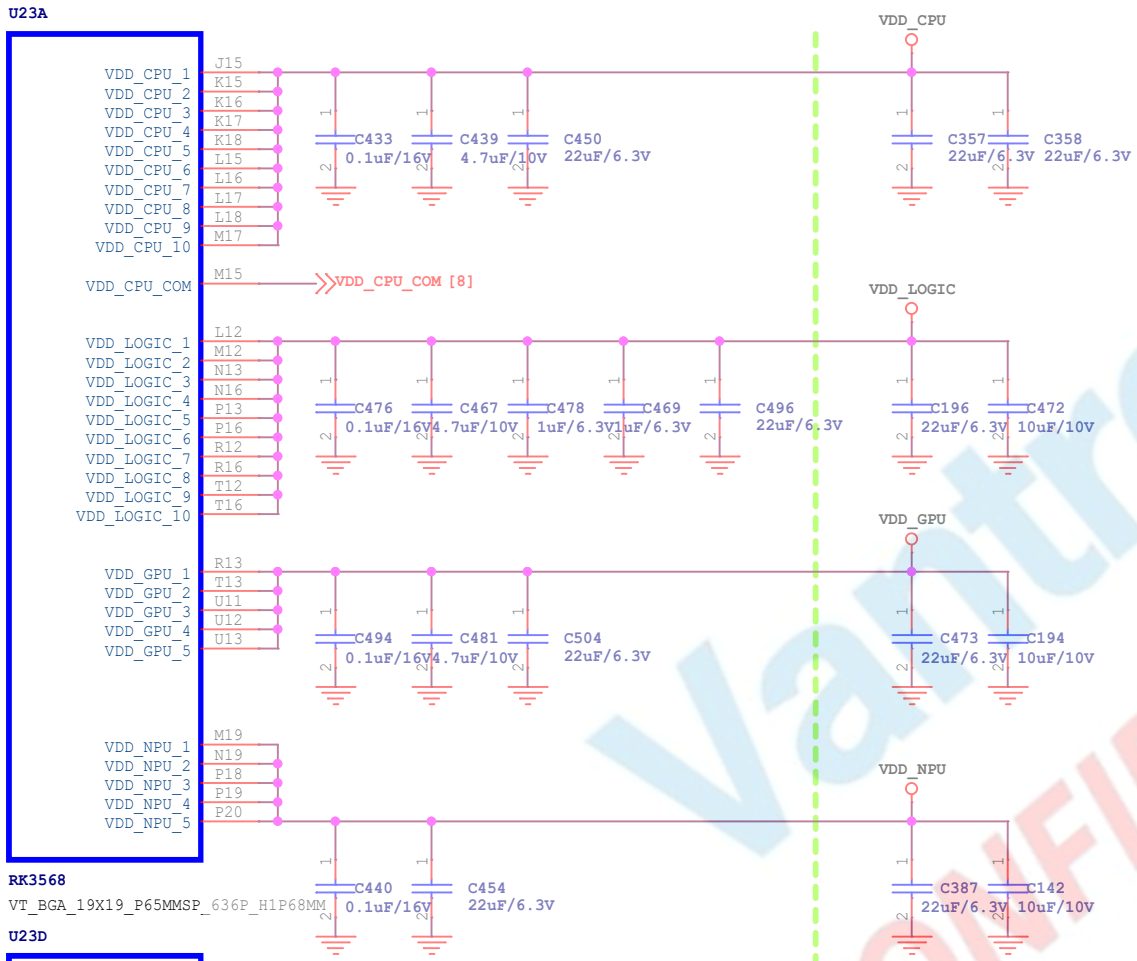
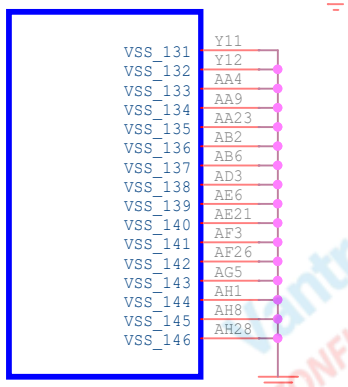
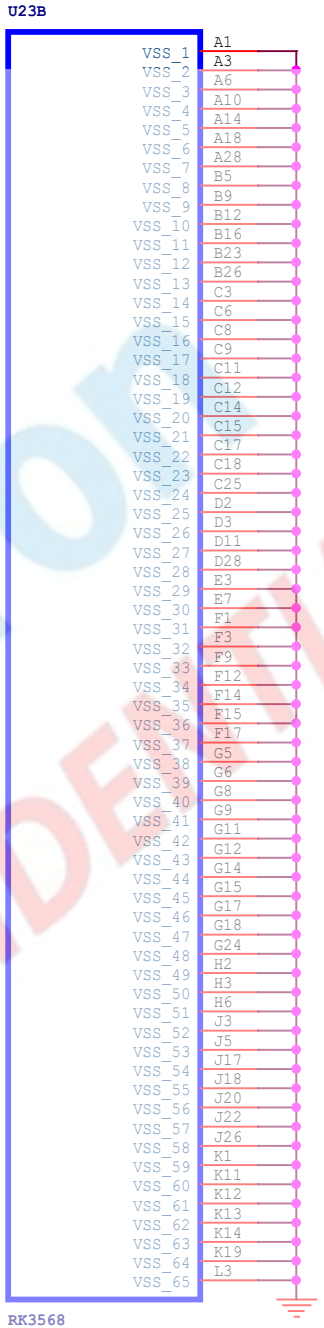
RK3568_ABCDE (Power&Gnd)

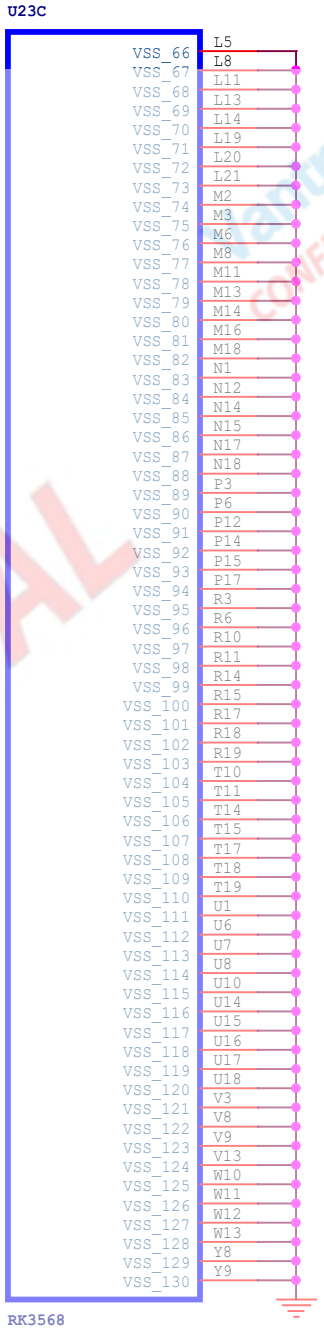


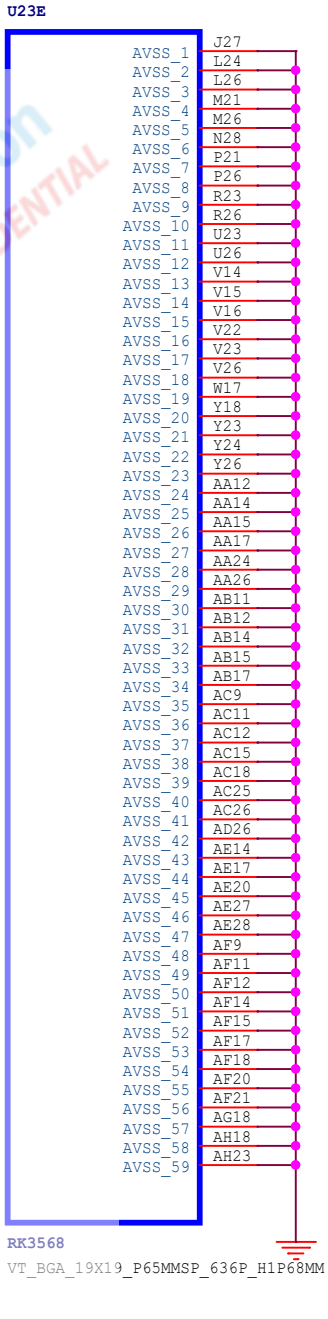
Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package









Title	10.RK3568_Power/GND	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
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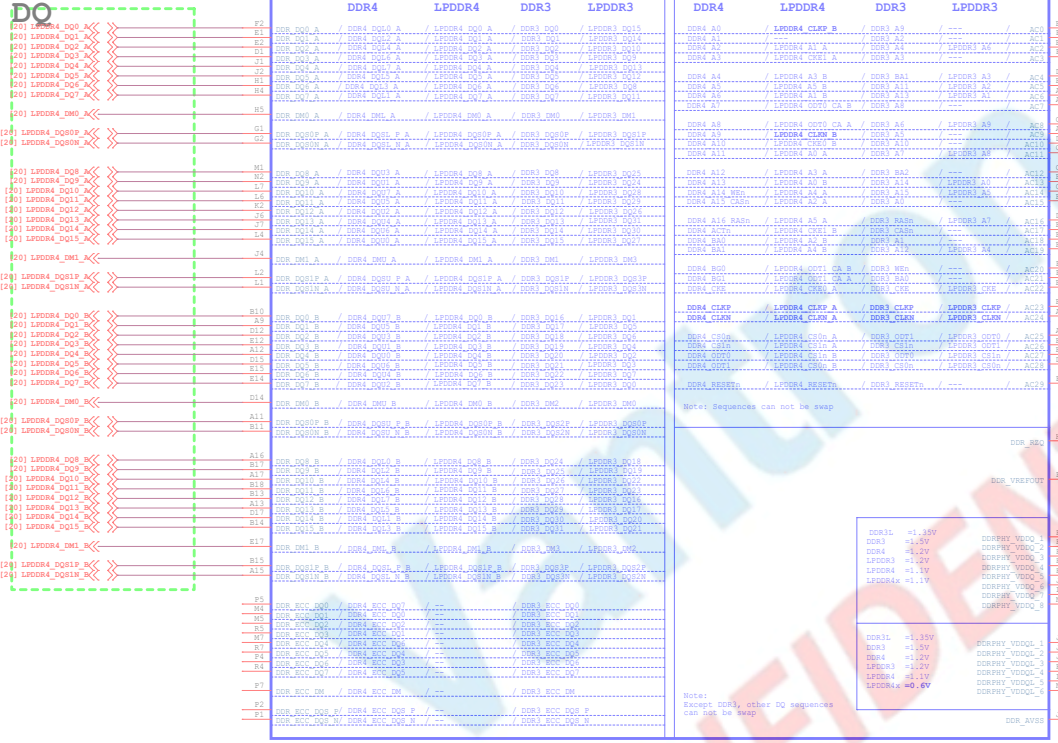
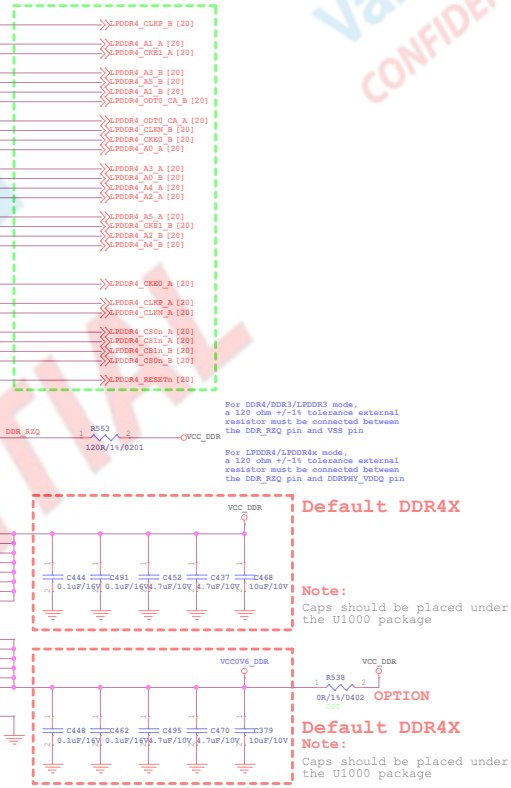
RK3568_F (DDR PHY)

LPDDR4/4x DQ



LPDDR4/4x AC



Title	11.RK3568_DDR PHY	Vantron
Size	Document Number	Rev
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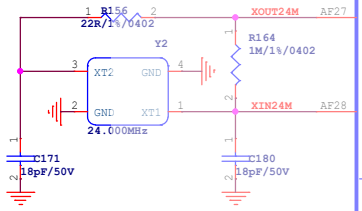
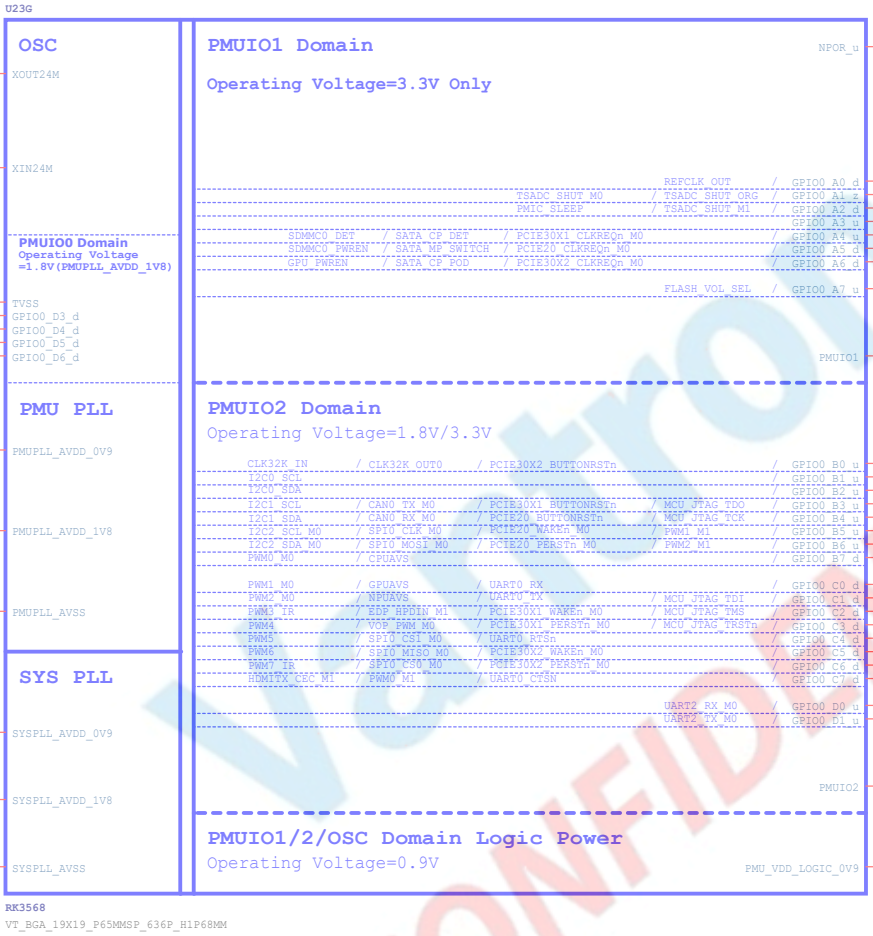
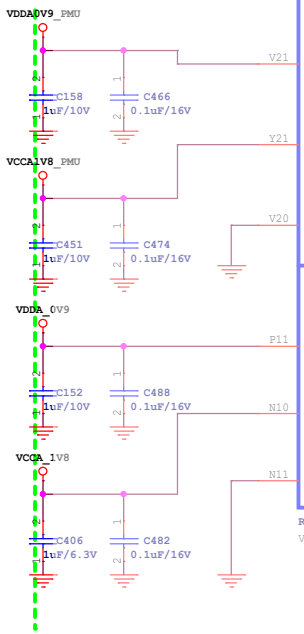
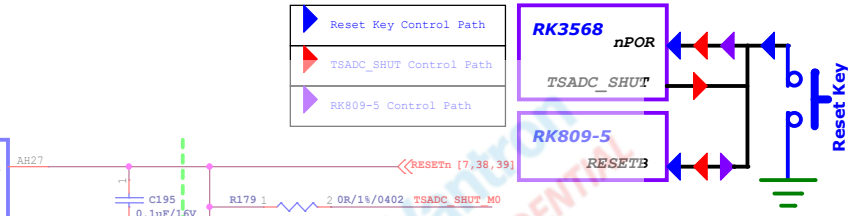
RK3568_G(OSC/PLL/PMUIO1/2)

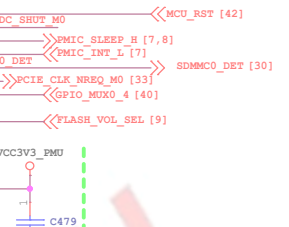
Note:
Adjusted the load capacitance according to the crystal specification.

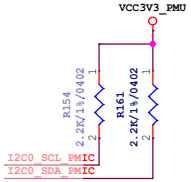


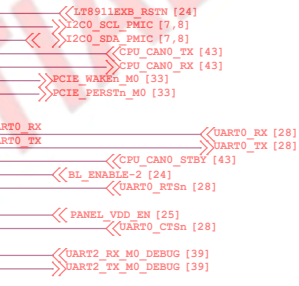


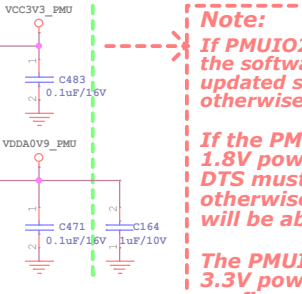












Note:
If PMUIO2 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the PMUIO2 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of PMUIO2 will be abnormally.

The PMUIO2 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of PMUIO2 will be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Title: 12.RK3568_OSC/PLL/PMUIO	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
Date: Tuesday, November 22, 2022	Sheet: 12 of 50		

RK3568_I(VCCIO2 Domain)

U23I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A24	eMMC_D0/FLASH_D0 [21]
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	C21	eMMC_D1/FLASH_D1 [21]
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B24	eMMC_D2/FLASH_D2 [21]
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	D21	eMMC_D3/FLASH_D3 [21]
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	A25	eMMC_D4/FLASH_D4 [21]
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	E21	eMMC_D5/FLASH_D5 [21]
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	E22	eMMC_D6/FLASH_D6 [21]
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	B25	eMMC_D7/FLASH_D7 [21]
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	B22	eMMC_CMD/FLASH_WRn [21]
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A23	eMMC_CLKOUT/FLASH_DQS_SOC — R130 22R/1%/0402 — eMMC_CLKOUT/FLASH_DQS [21]
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	A26	eMMC_DATA_STROBE/FLASH_CLE [21]
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	F20	eMMC_RSTn/FSPI_D2/FLASH_WPn [21]
	FSPI_CLK / FLASH_ALE	GPIO1_D0_d	A22	
	FSPI_D0 / FLASH_RDY	GPIO1_D1_u	C24	
	FSPI_D1 / FLASH_RDn	GPIO1_D2_u	D23	
	FSPI_CS0n / FLASH_CS0n	GPIO1_D3_u	C23	
	FSPI_D3 / FLASH_CS1n	GPIO1_D4_u	A27	

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 — H18

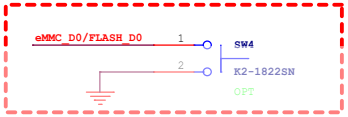
VCCIO_FLASH — C430 0.1uF/16V

RK3568
VT_BGA_19X19_P65MMSP_636P_H1P68MM

Note:

"FLASH_VOL_SEL" status and VCCIO_FLASH power supply voltage must match otherwise the IO function of VCCIO2 will be abnormally or the IO of VCCIO2 will be damaged!

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.



Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added

RK3568_J(VCCIO3 Domain)

U23J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1	/ PWM8_M1	/ GPIO1_D5_u	J25	SDMMC0_DATA0 — SDMMC0_DATA0 [30]
SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1	/ PWM9_M1	/ GPIO1_D6_u	J24	SDMMC0_DATA1 — SDMMC0_DATA1 [30]
SDMMC0_D2 / ARMJTAG_TCK / UART5_CTSn_M0		/ GPIO1_D7_u	H26	SDMMC0_DATA2 — SDMMC0_DATA2 [30]
SDMMC0_D3 / ARMJTAG_TMS / UART5_RTSn_M0		/ GPIO2_A0_u	J23	SDMMC0_DATA3 — SDMMC0_DATA3 [30]
SDMMC0_CMD / PWM10_M1 / UART5_RX_M0	/ CAN0_TX_M1	/ GPIO2_A1_u	H27	SDMMC0_CMD — SDMMC0_CMD [30]
SDMMC0_CLK / TEST_CLKOUT / UART5_TX_M0	/ CAN0_RX_M1	/ GPIO2_A2_d	H28	SDMMC0_CLK — SDMMC0_CLK [30]

VCCIO3 — L22

VCCIO_SD — C416 0.1uF/16V

RK3568
VT_BGA_19X19_P65MMSP_636P_H1P68MM

Note:

If VCCIO3 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

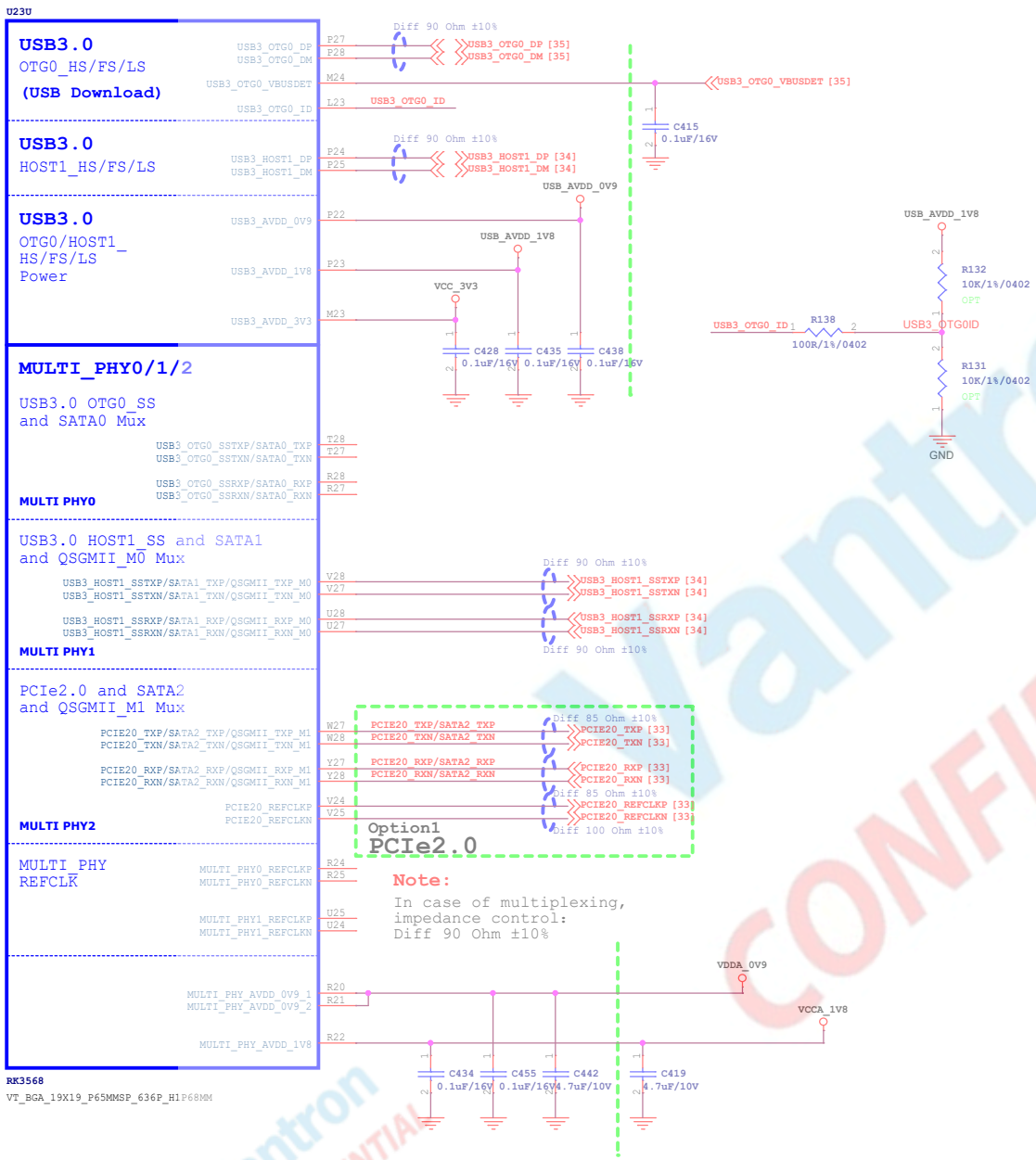
If the VCCIO3 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO3 will be abnormally.

The VCCIO3 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO3 will be damaged!

If a board needs to be compatible with two voltage choices,
recommended to enable BOM_ID

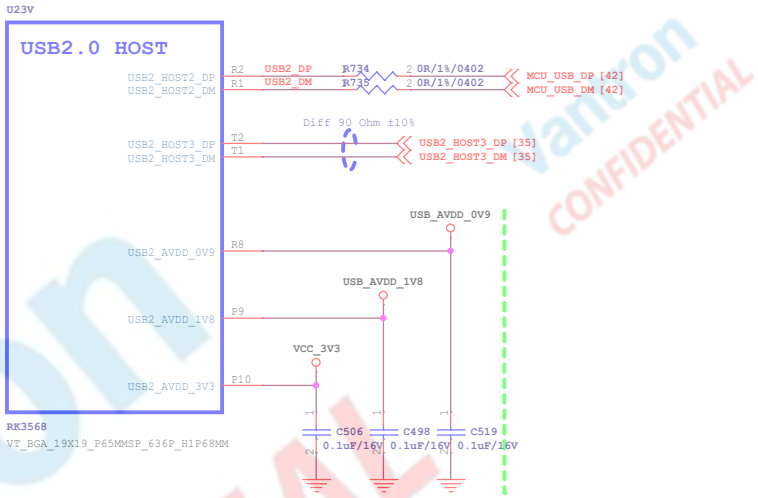
Title	13.RK3568_Flash/SD Controller	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
Size	Document Number		Rev
A3	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		<1.0>
Date:	Tuesday, November 22, 2022	Sheet 13	of 50

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)

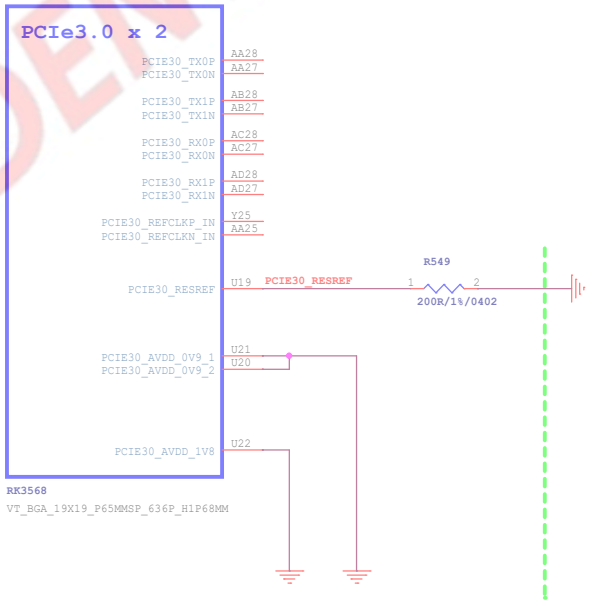


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Title: 14.RK3568_USB/PCIe/SATA PHY		ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
Date: Tuesday, November 22, 2022	Sheet: 14 of 50		

RK3568_K(VCCIO4 Domain)

Note: *If VCCIO4 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!*
If the VCCIO4 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO4 will be abnormally.
The VCCIO4 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO4 will be damaged!

U23K

VCCIO4 Domain
Operating Voltage=1.8V/3.3V

SDMMC1_D0	GMAC0_RXD2	UART6_RX_M0		GPIO2_A3_u
SDMMC1_D1	GMAC0_RXD3	UART6_TX_M0		GPIO2_A4_u
SDMMC1_D2	GMAC0_RXCLK	UART7_RX_M0		GPIO2_A5_u
SDMMC1_D3	GMAC0_TXD2	UART7_TX_M0		GPIO2_A6_u
SDMMC1_CMD	GMAC0_TXD3	UART9_RX_M0		GPIO2_A7_u
SDMMC1_CLK	GMAC0_TXCLK	UART9_TX_M0		GPIO2_B0_d
SDMMC1_PWREN	I2C4_SDA_M1	UART8_RTSn_M0	CAN2_RX_M1	GPIO2_B1_d
SDMMC1_DET	I2C4_SCL_M1	UART8_CTSn_M0	CAN2_TX_M1	GPIO2_B2_u
	GMAC0_TXD0	UART1_RX_M0		GPIO2_B3_u
	GMAC0_TXD1	UART1_TX_M0		GPIO2_B4_u
	GMAC0_TXEN	UART1_RTSn_M0	SPI1_CLK_M0	GPIO2_B5_u
	GMAC0_RXD0	UART1_CTSn_M0	SPI1_MISO_M0	GPIO2_B6_u
I2S2_SCLK_RX_M0	GMAC0_RXD1	UART6_RTSn_M0	SPI1_MOSI_M0	GPIO2_B7_d
I2S2_LRCK_RX_M0	GMAC0_RXDV_CRS	UART6_CTSn_M0	SPI1_CS0_M0	GPIO2_C0_d
I2S2_MCLK_M0	ETHU_REFCLKO_25M	UART7_RTSn_M0	SPI1_CLK_M0	GPIO2_C1_d
I2S2_SCLK_TX_M0	GMAC0_MCLKINOUT	UART7_CTSn_M0	SPI2_MISO_M0	GPIO2_C2_d
I2S2_LRCK_TX_M0	GMAC0_MDC	UART9_RTSn_M0	SPI2_MOSI_M0	GPIO2_C3_d
I2S2_SDO_M0	GMAC0_MDIO	UART9_CTSn_M0	SPI2_CS0_M0	GPIO2_C4_d
I2S2_SDI_M0	GMAC0_RXER	UART8_TX_M0	SPI2_CS1_M0	GPIO2_C5_d
CLK32K_OUT1		UART8_RX_M0	SPI1_CS1_M0	GPIO2_C6_d

VCCIO4

E27 SDMMC1_D0 [30]
E28 SDMMC1_D1 [30]
B28 SDMMC1_D2 [30]
C27 SDMMC1_D3 [30]
C28 SDMMC1_CMD [30]
D27 SDMMC1_CLK [30]
D26 CPU_CAN2_RX_M1 [43]
E25 CPU_CAN2_TX_M1 [43]
F28 CPU_UART1_RX_M0 [15]
G27 CPU_UART1_TX_M0 [15]
G28 CPU_UART1_RTS_M0 [15]
F27 CPU_UART1_CTS_M0 [15]
H25 AUDIO_OUT_select [41]
F24 USB3_HUB_RST [34]
G23 GPIO_MUX0_1 [40]
F25 CUP_IN_RESET1 [46]
H24 AUDIO_MUTE [36]
H23 HP_DET_L_GPIO3_C2 [41]
F26 GPIO_MUX0_5 [40]
E26 MIC_IN_DET [41]

VCCIO_SD2 VCCIO_SD2
J21 C412 0.1uF/16V
R534 1 2 0R/1%/0402 VCCIO_SD

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

RK3568
VT_BGA_19X19_P65MMSP_636P_H1P68MM

RK3568_N(VCCIO7 Domain)

U23N

VCCIO7 Domain
Operating Voltage=1.8V/3.3V

PWM14_M1	SPI3_CLK_M1	CAN1_RX_M1	PCIE30X2_CLKREQn_M2	I2S3_MCLK_M1 GPIO4_C2_d
PWM15_IR_M1	SPI3_MOSI_M1	CAN1_TX_M1	PCIE30X2_WAKEn_M2	I2S3_SCLK_M1 GPIO4_C3_d
EDP_HPDIN_M0	SPDIF_TX_M2	SATA2_ACT_LED	PCIE30X2_PERSTn_M2	I2S3_LRCK_M1 GPIO4_C4_d
PWM12_M1	SPI3_MISO_M1	SATA1_ACT_LED	UART9_TX_M1	I2S3_SDO_M1 GPIO4_C5_d
PWM13_M1	SPI3_CS0_M1	SATA0_ACT_LED	UART9_RX_M1	I2S3_SDI_M1 GPIO4_C6_d
HDMITX_SCL	I2C5_SCL_M1			GPIO4_C7_u
HDMITX_SDA	I2C5_SDA_M1			GPIO4_D0_u
HDMITX_CEC_M0	SPI3_CS1_M1			GPIO4_D1_u
				GPIO4_D2_d

VCCIO7

AF8 I2S3_MCLK_M1 R720 OPT 2 22R/1%/0402
AA11 I2S3_SCLK_M1 R721 2 22R/1%/0402
AH7 I2S3_LRCK_M1 R722 2 22R/1%/0402
AD8 I2S3_SDO_M1 R723 2 22R/1%/0402
AE8 I2S3_SDI_M1 R724 2 22R/1%/0402
I2S_SCK [33]
I2S_WS [33]
I2S_OUT [33]
I2S_IN [33]
AG8 HDMITX_SCL [26]
AG7 HDMITX_SDA [26]
AH6 HDMITX_CEC_M0 [26]
AB9

VCCIO7 VCC_1V8
V12 R719 1 0R/1%/0402 2
C511 0.1uF/16V

Note:
If VCCIO7 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!
If the VCCIO7 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO7 will be abnormally.
The VCCIO7 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO7 will be damaged!

RK3568
VT_BGA_19X19_P65MMSP_636P_H1P68MM

RK3568_O(SARADC/OTP)

U23O

SARADC

Recovery/ SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY	C123 1	2 1000pF/50V
SARADC_VIN1	C26	SARADC_VIN1_HW_ID	C377 1	2 1000pF/50V
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK	C395 1	2 1000pF/50V
SARADC_VIN3	E23			
SARADC_VIN4	G21			
SARADC_VIN5	F22			
SARADC_VIN6	G20			
SARADC_VIN7	F21			
SARADC_AVDD_1V8	H22			

OTP

OTP_VCC18 H20

VCCA_1V8
C410 0.1uF/16V
VCC_1V8
C417 0.1uF/16V

RK3568
VT_BGA_19X19_P65MMSP_636P_H1P68MM

Note:
Must be mounted
VCCA_1V8
R127 10K/1%/0402
SARADC_VIN0_KEY/RECOVERY

If there is no **Key requirement**, two test points **must be reserved** to facilitate **firmware update**

It is suggested **to reserve a** Key to facilitate **the** development debug

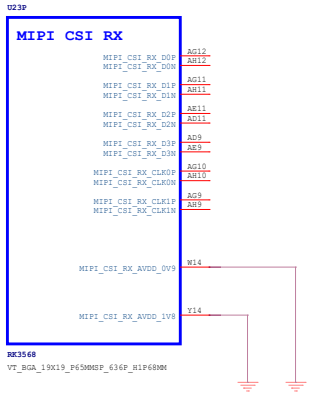
If SARADC_VIN0=**0V** at after power **on and reset**, then system will enter into loader **mode.**

SARADC_VIN0_KEY/RECOVERY [38]
SARADC_VIN1_HW_ID [38]

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

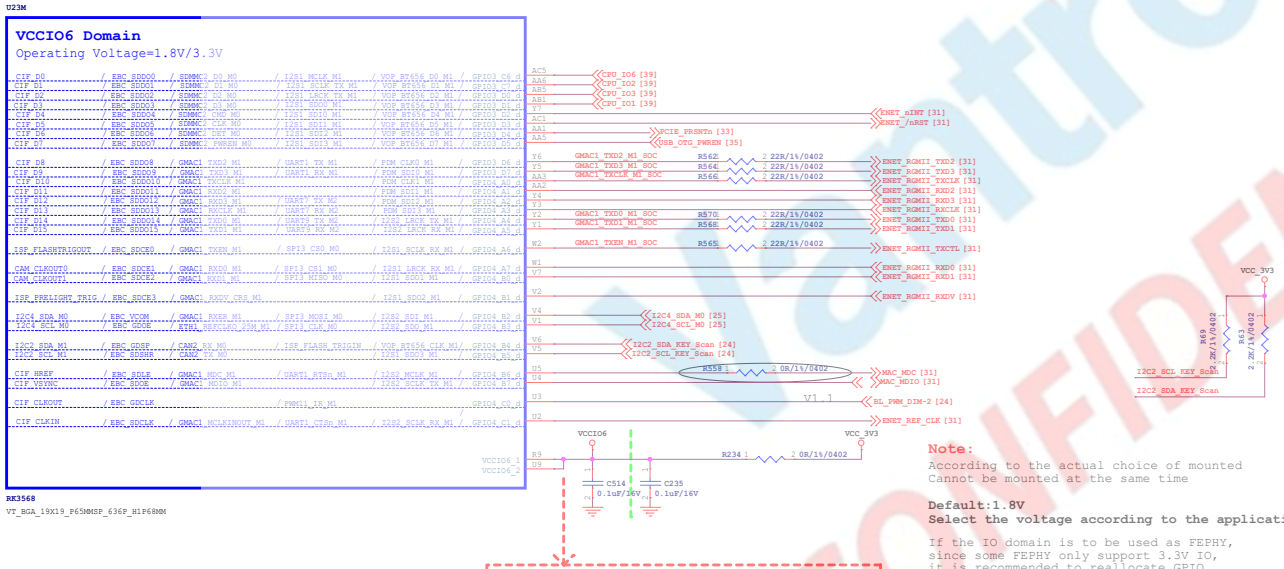
Title	15.RK3568_SARADC/GPIO	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size	Document Number		Rev
A3	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		<1.0>
Date:	Tuesday, November 22, 2022	Sheet 15 of 50	

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If VCCIO6 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO6 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO6 will be abnormally.

The VCCIO6 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO6 will be damaged!

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Default:1.8V
Select the voltage according to the application

If the IO domain is to be used as FEPHY,
since some FEPHY only support 3.3V IO,
it is recommended to reallocate GPIO
to reduce the cost of level conversion

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

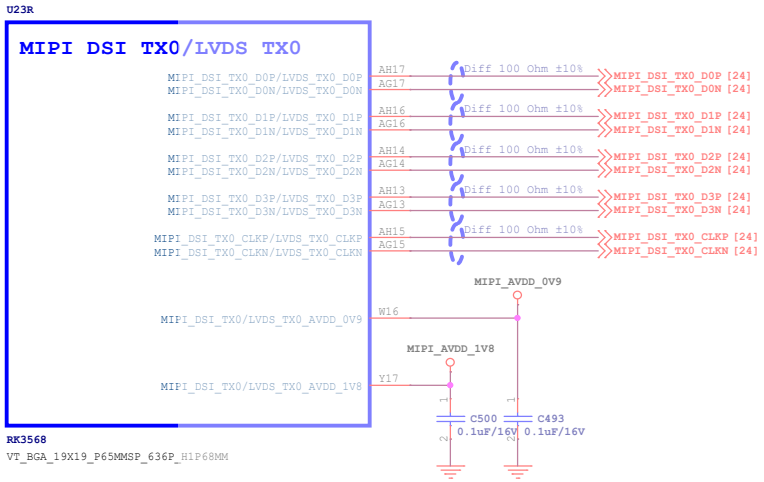
Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

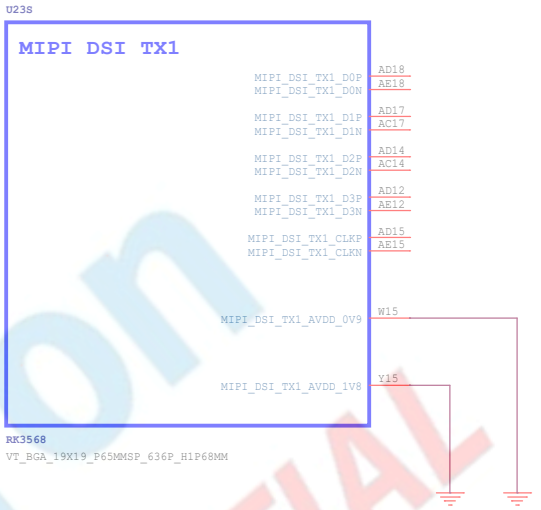
GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_CRS_DV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx OSC	ETHx_REFCLKO_25M	------->	PHYx OSC
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	<------->	PHYx_TXC
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

Title: 16.RK3568_VI Interface	Vantron	ChengDu Vantron Technology.LTD 6th Floor, 1st Building,No.5, 3rd Wuke East Street, Wuhou District ,ChengDu , China 86-28-8512-3930
Size: A2	Document Number: 640BBAGG3R121 SBC-RK3568-NXP1024-ARK-L2	Rev: <1.0>
Date: Tuesday, November 22, 2022	Sheet 16 of 50	

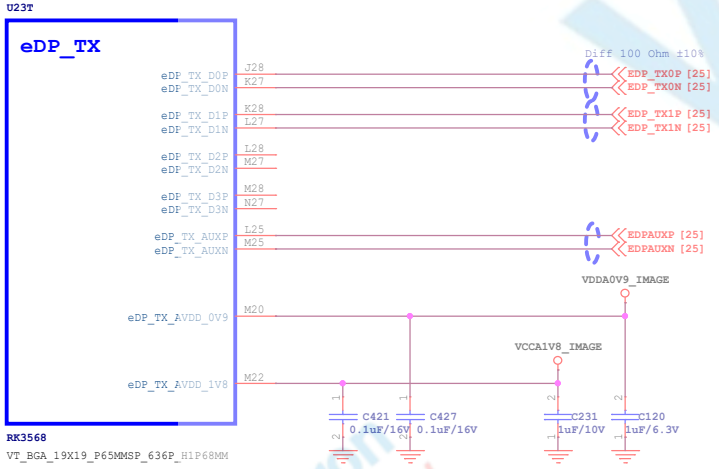
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



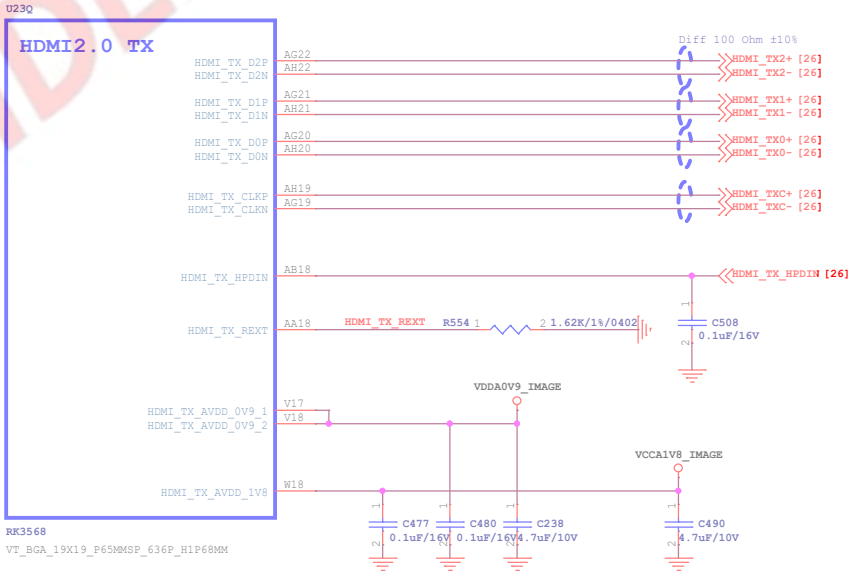
RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



RK3568_Q(HDMI2.0 TX)



Title	17.RK3568_VO Interface_1		
Size	Document Number		Rev
A3	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		<1.0>
Date:	Tuesday, November 22, 2022	Sheet 17	of 50

ChengDu Vantron Technology.,LTD
6th Floor, 1st Building,No.9,
3rd WuKe East Street,
WuHou District ,ChengDu , China
86-28-8512-3930

RK3568_L(VCCIO5 Domain)

U23L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3568

VT_BGA_19X19_P65MMSP_636P_H1P68MM

AG6 — R249 1 — 2 0R/1%/0402 — CPU_SPI0_FLASH_MISO [29]
AD7 — R250 1 — 2 0R/1%/0402 — CPU_SPI0_FLASH_MOSI [29]
AC8 — R251 1 — 2 0R/1%/0402 — CPU_SPI0_FLASH_CS [29]
AC7 — R252 1 — 2 0R/1%/0402 — CPU_SPI0_FLASH_SCK [29]
AF5 — LCD1_PWR_EN [27]
AF6 — CPU_CAN2_STBY [43]
AD6 — CPU_IO8 [39]
AH5 — LCD1_5V_12V_SEL [27]
AH4 — LCD_BL1_EN [25]
AB8 — CPU_IO4 [39]
AE5 — CPU_IO7 [39]
AG4 — LCD2_PWR_EN [27]
AF4 — LCD2_5V_12V_SEL [27]
AH3 — CPU_IO5 [39]
AG3 — SPEAKER_SD_A# [37]
AH2 — WD_SET [23]
AG2 — LCD1_EDID_LINK [25]
AG1 — Buzzer_EN_PWM [23]
AF2 — CPU_LED_status
AF1 — I2C5_SCL_M0 [22]
AE1 — I2C5_SDA_M0 [22]
AE2 — I2C3_SCL_M1 [24]
AE3 — I2C3_SDA_M1 [24]
AD4 — UART3_TX_M1
AD2 — UART3_RX_M1
AD1 — LCD2_EDID_LINK [24]
AA7 — eDP_HPD# [25]
AC4 — EEPROM_WP [22]
AC3 — LCD_BL1_PWM [25]
AC2 — WD_WDI [23]

V10 — VCCIO5_1
V11 — VCCIO5_2

VCC_3V3 — C515 0.1uF/16V

Status

VCC_3V3 — D4 LED,Red — R97 100R/1%/0402 — Q13 JMTL2N7002KS — GND

CPU_LED_status

Note:

If VCCIO5 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO5 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO5 will be abnormally.

The VCCIO5 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO5 will be damaged!

VCC_3V3 — R240 2.2K/1%/0402 — R237 2.2K/1%/0402 — I2C5_SCL_M0 — I2C5_SDA_M0

UART3_RX_M1 — R207 1 — 2 0R/1%/0402 — MCU_TO_CPU_UART5_TX [42]
UART3_TX_M1 — R208 1 — 2 0R/1%/0402 — MCU_TO_CPU_UART5_RX [42]

TO MCU

Title	18.RK3568_VO Interface_2	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size	A4	Document Number 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2	Rev <1.0>
Date:	Tuesday, November 22, 2022	Sheet 18 of 50	

RK3568_H(VCCIO1 Domain)

U23H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

RK3568

VT_BGA_19X19_P65MMSP_636P_H1P68MM

D18 PRTPWR1 [35]
E18 PRTPWR2 [35]

A19 I2S1_MCLK_M0_SOC — R1391 2 22R/1%/0402 — I2S1_MCLK_M0_RK809 [7]
B19 I2S1_SCLK_TX_M0_SOC — R1371 2 22R/1%/0402 — I2S1_SCLK_TX_M0_RK809 [7]
F18 PRTPWR4 [35]
A20 I2S1_LRCK_TX_M0_SOC — R1351 2 22R/1%/0402 — I2S1_LRCK_TX_M0_RK809 [7]
C20 PDM_CLK0_M0_SOC — R5361 2 22R/1%/0402 — PDM_CLK0_M0_RK809 [7]

B20 I2S1_SDO0_M0_RK809 [7]
D20 GPIO_MUX0_2 [40]
E20 USBHUB_RSTn [35]
A21 GPIO_MUX0_3 [40]
B21 I2S1_SDI0_M0/PDM_SDI0_M0_RK809 [7]

VCCIO_ACODEC

Default 3.3V

H17 VCCIO1

C436 0.1uF/16V

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:

If VCCIO1 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO1 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO1 will be abnormally.

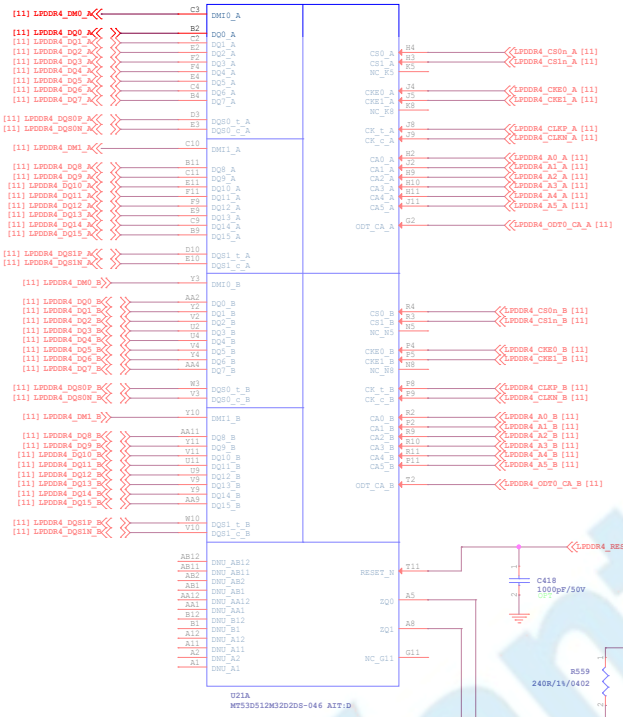
The VCCIO1 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO1 will be damaged!

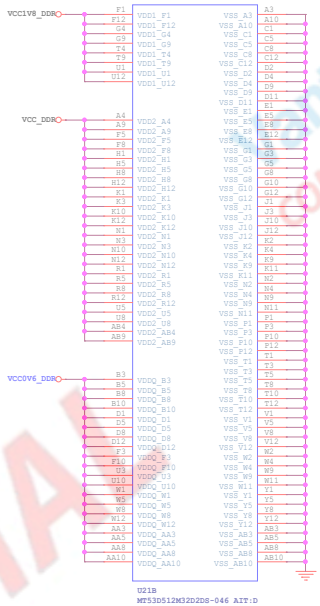
Note:

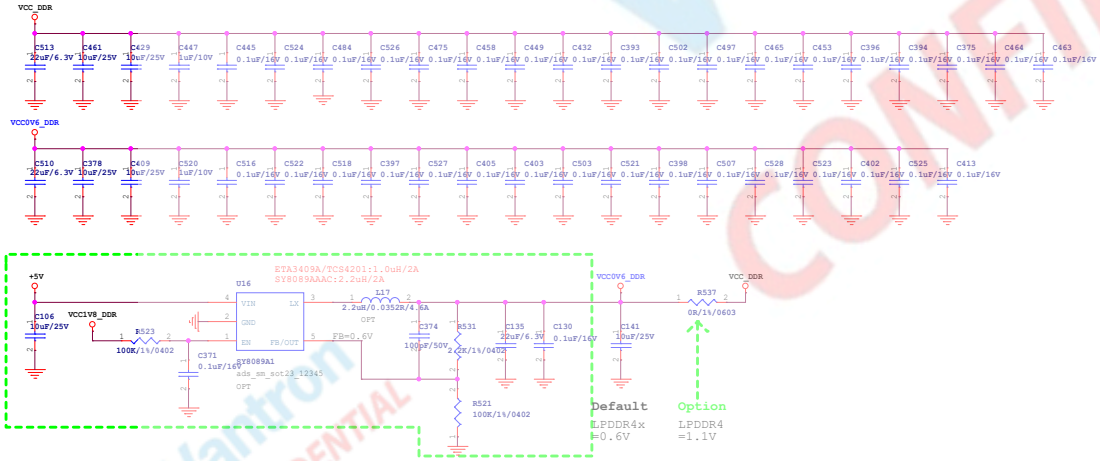
Caps of between dashed green lines and U1000 should be placed under the U1000 package

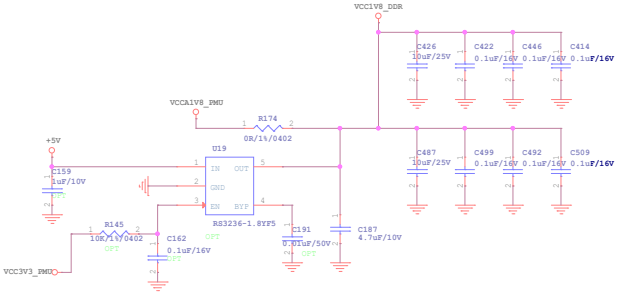
Title	19.RK3568_Audio Interface	Vantron	ChengDu Vantron Technology.,LTD 6th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
Size	A4	Document Number	640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2
Rev	<1.0>		
Date:	Tuesday, November 22, 2022	Sheet	19 of 50

LPDDR4X









Title: 20.DRAM-LPDDR4_1x32bit_200P	Vantron	ChengDu Vantron Technology,LTD 6th Flloy, 1st Building,No.9, 3rd Wuke East Street, Wuhou District ,ChengDu , China 86-28-8512-3930
Size: A2	Document Number: 6408BAGG3RL21 SRC-RK3568-NXP1024-ARK-L2	Rev: <1.0>
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Siganal & Power

eMMC_D0/FLASH_D0 [13]
eMMC_D1/FLASH_D1 [13]
eMMC_D2/FLASH_D2 [13]
eMMC_D3/FLASH_D3 [13]
eMMC_D4/FLASH_D4 [13]
eMMC_D5/FLASH_D5 [13]
eMMC_D6/FLASH_D6 [13]
eMMC_D7/FLASH_D7 [13]

eMMC_CMD/FLASH_WRn [13]

eMMC_CLKOUT/FLASH_DQS [13]

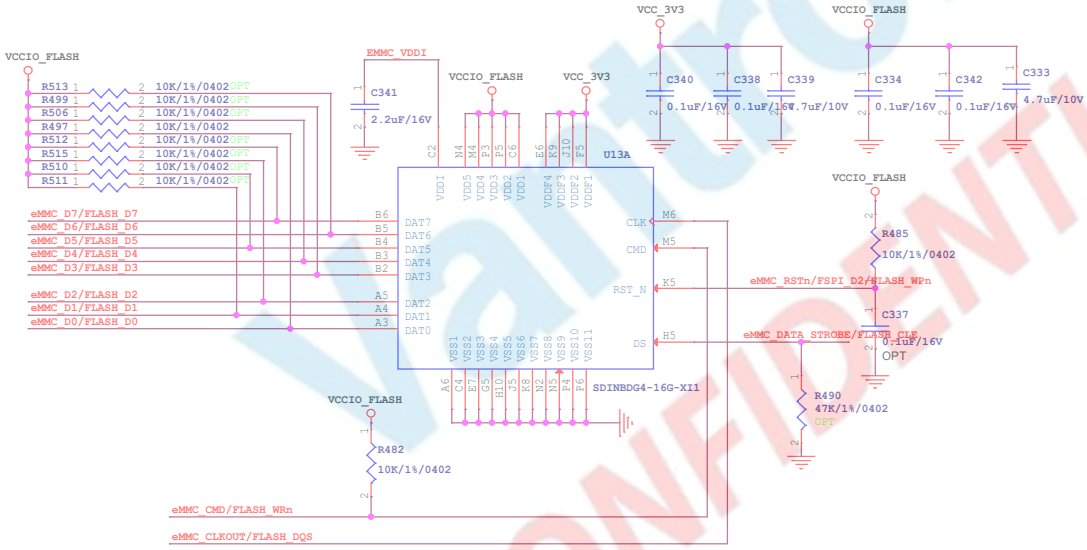
eMMC_DATA_STROBE/FLASH_CLE [13]

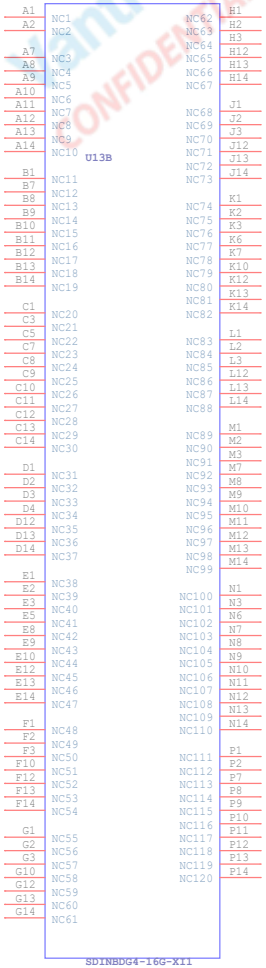
eMMC_RSTn/FSPI_D2/FLASH_WPn [13]

VCCIO_FLASH — VCCIO_FLASH

VCC_3V3 — VCC_3V3

eMMC Flash





Title: 21.eMMC	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuke East Street, Wuhou District, ChengDu , China 86-28-8512-3930
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2	Rev: <1.0>
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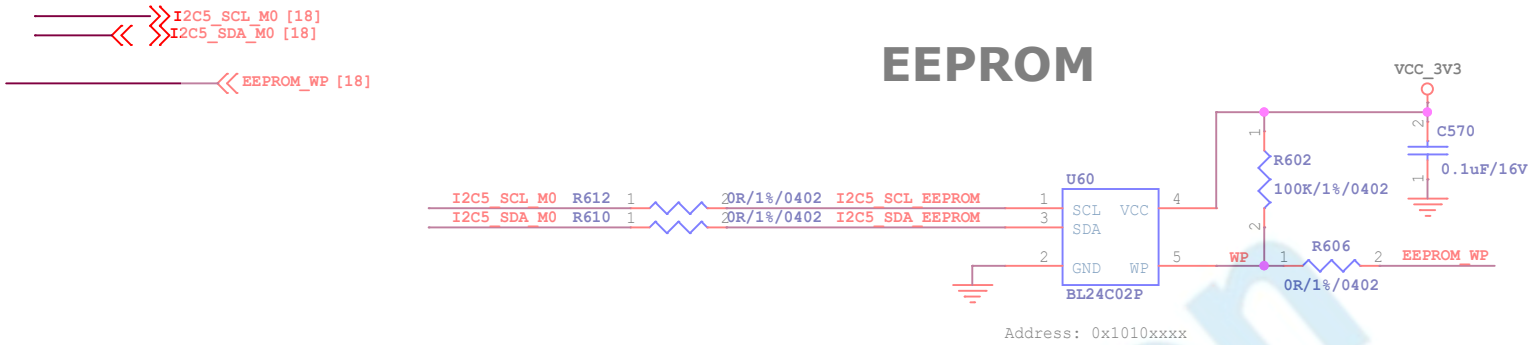
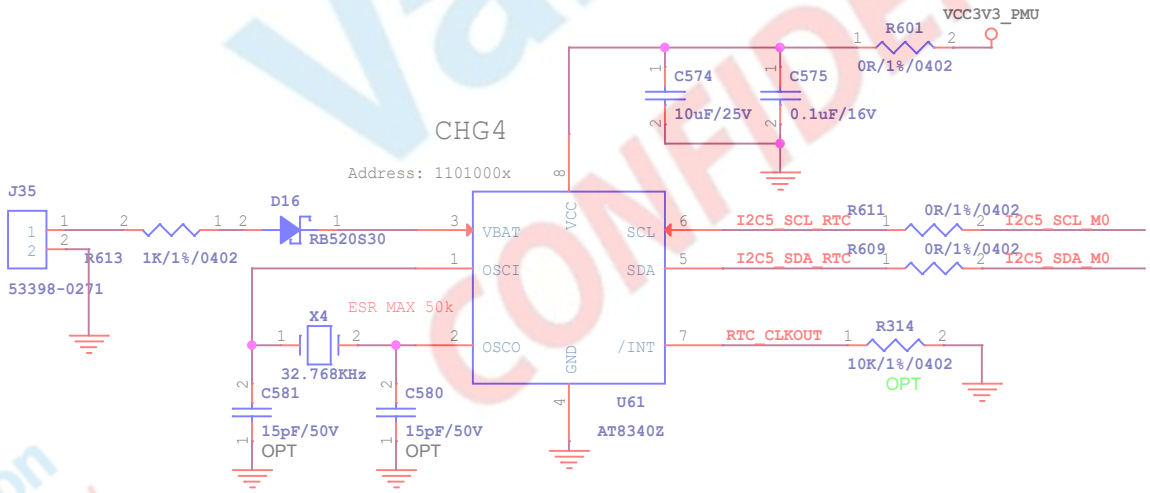


RTC IC



Title: 22.EEPROM/RTC	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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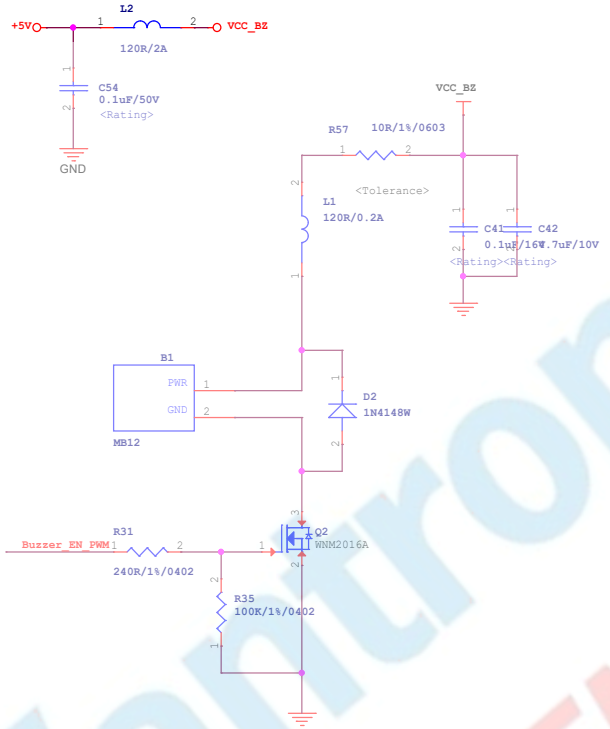
I2C5_SCL_M0 [18,22]
I2C5_SDA_M0 [18,22]

Buzzer_EN_PWM [18]

Buzzer

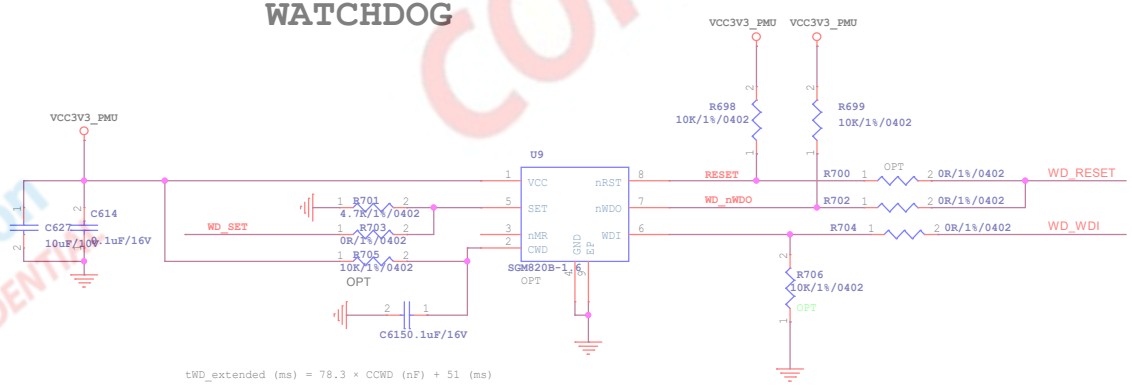


RUZZER

共振频率： 4kHz

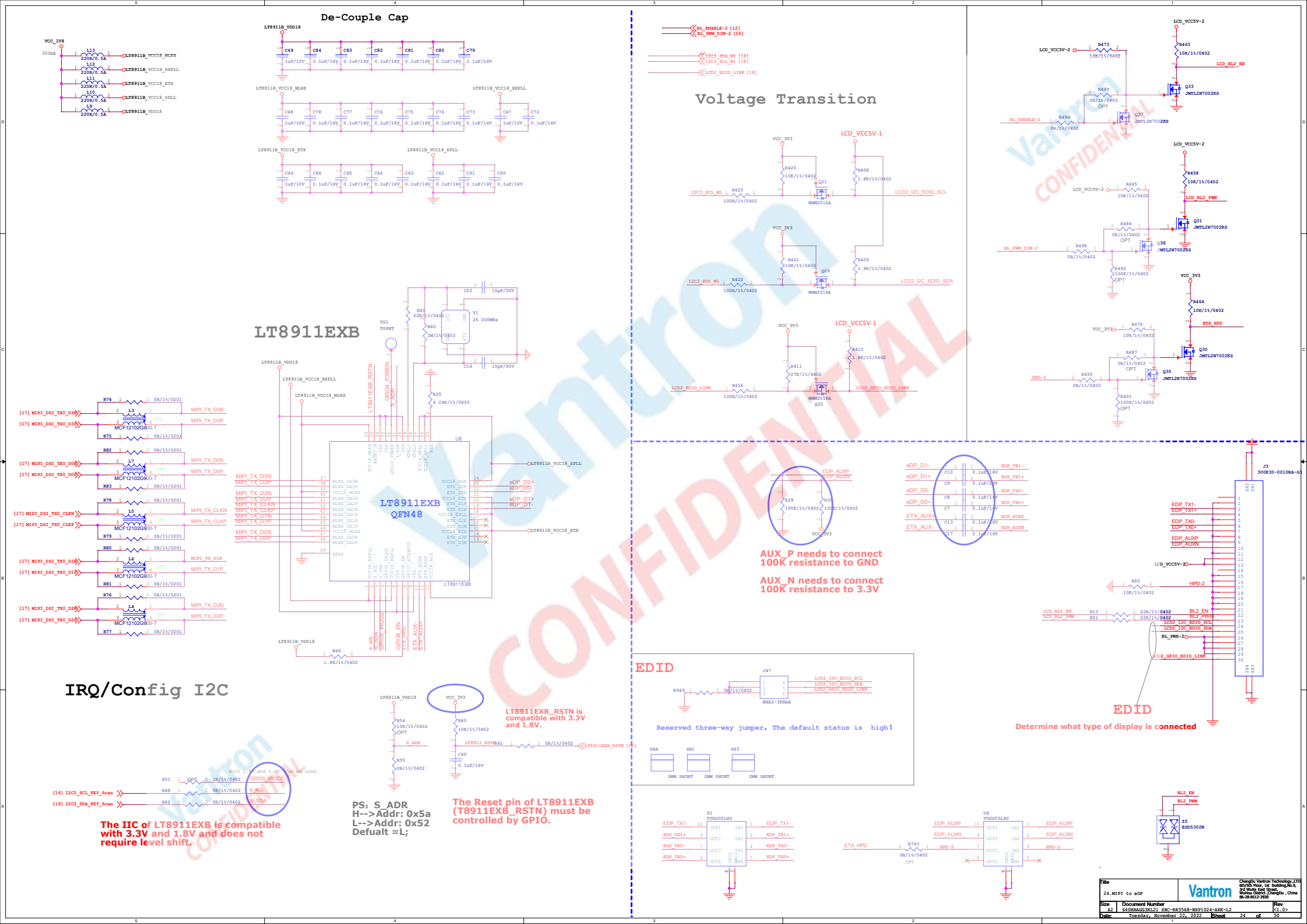
WD_SET [18]
WD_RESET [12]
WD_WDI [18]

WATCHDOG



tWD_extended (ms) = 78.3 × CCWD (nF) + 51 (ms)

Title: 23.Buzzer/WTD	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District, ChengDu , China 86-28-8512-3930
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2	Rev: <1.0>
Date: Tuesday, November 22, 2022	Sheet 23 of 50	


De-Couple Cap
LT8911B_VDD18
C49 C84 C83 C82 C81 C80 C79
1uF/10V 0.1uF/16V
LT8911B_VCC18_MLRX
C48 C78 C77 C76 C75 C74 C73 C47 C72
LT8911B_VCC18_RXPLL
LT8911B_VCC18_ETX
C46 C66 C65 C64 C63 C62 C61 C60
LT8911B_VCC18_SPLL
VCC_1V8
300mA
L13 220R/0.5A LT8911B_VCC18_MLRX
L12 220R/0.5A LT8911B_VCC18_RXPLL
L11 220R/0.5A LT8911B_VCC18_ETX
L10 220R/0.5A LT8911B_VCC18_SPLL
L9 220R/0.5A LT8911B_VDD18
LT8911EXB
LT8911EXB QFN48
TS1 TSPNT
Y1 25.000MHz
C22 15pF/50V
C16 15pF/50V
R47 22R/1%/0402
R40 1M/1%/0402
R25 6.04K/1%/0603
U8
LT8911EXB_RSTN
GPIO4_PSREN
S_ADR
MIPI_TX_D3N
MIPI_TX_D3P
MIPI_TX_D2N
MIPI_TX_D2P
MIPI_TX_CLKN
MIPI_TX_CLKP
MIPI_TX_D1N
MIPI_TX_D1P
MIPI_TX_D0N
MIPI_TX_D0P
eDP_D0+
eDP_D0-
eDP_D1+
eDP_D1-
R46 1.8K/1%/0402
[17] MIPI_DSI_TX0_D3N
[17] MIPI_DSI_TX0_D3P
[17] MIPI_DSI_TX0_D2N
[17] MIPI_DSI_TX0_D2P
[17] MIPI_DSI_TX0_CLKN
[17] MIPI_DSI_TX0_CLKP
[17] MIPI_DSI_TX0_D1N
[17] MIPI_DSI_TX0_D1P
[17] MIPI_DSI_TX0_D0N
[17] MIPI_DSI_TX0_D0P
R74 R82 R78 R80 R76 0R/1%/0201
L3 L7 L5 L6 L4 MCF12102G900-T
R75 R83 R79 R81 R77
IRQ/Config I2C
GPIO5_IRQO2
S_SCL
S_SDA
[16] I2C2_SCL_KEY_Scan
[16] I2C2_SDA_KEY_Scan
R51 OPT
R68 R62 0R/1%/0402
Both 1.8V and 3.3V can be used.
The IIC of LT8911EXB is compatible with 3.3V and 1.8V and does not require level shift.
VCC_3V3
R54 10K/1%/0402 OPT
R65 10K/1%/0402
R55 0R/1%/0402
C40 0.1uF/16V
LT8911_RSTN
R61 0R/1%/0402
LT8911EXB_RSTN [18]
LT8911EXB_RSTN is compatible with 3.3V and 1.8V.
PS: S_ADR
H-->Addr: 0x5a
L-->Addr: 0x52
Defualt =L;
The Reset pin of LT8911EXB (T8911EXB_RSTN) must be controlled by GPIO.
BL_ENABLE-2 [12]
BL_PWM_DIM-2 [16]
I2C3_SDA_M1 [18]
I2C3_SCL_M1 [18]
LCD2_EDID_LINK [18]
Voltage Transition
LCD_VCC5V-1
VCC_3V3
R420 10K/1%/0402
R408 1.8K/1%/0402
Q21
I2C3_SCL_M1
R425 100R/1%/0402
WNM2016A
LCD2_I2C_EDID_SCL
R421 10K/1%/0402
R409 1.8K/1%/0402
Q26
I2C3_SDA_M1
R422 100R/1%/0402
LCD2_I2C_EDID_SDA
R411 27K/1%/0402
R410 1.8K/1%/0402
Q22
LCD2_EDID_LINK
R416 100R/1%/0402
LCD2_GPIO_EDID_LINK
LCD_VCC5V-2
R473 10K/1%/0402
R463 10K/1%/0402
LCD_BL2_EN
Q33 JMTL2N7002KS
R489 0R/1%/0402 OPT
Q37 JMTL2N7002KS
BL_ENABLE-2
R494 0R/1%/0402
R458 10K/1%/0402
LCD_BL2_PWM
R465 10K/1%/0402
Q31 JMTL2N7002KS
R486 0R/1%/0402 OPT
Q36 JMTL2N7002KS
BL_PWM_DIM-2
R496 0R/1%/0402
R492 100K/1%/0402 OPT
R464 10K/1%/0402
ETX_HPD
VCC_3V3
R476 10K/1%/0402
R487 0R/1%/0402 OPT
Q30 JMTL2N7002KS
Q35 JMTL2N7002KS
HPD-2
R495 0R/1%/0402
R491 100K/1%/0402 OPT
EDP_AUXP
EDP_AUXN
R29 100K/1%/0402
R35 100K/1%/0402
VCC_3V3
AUX_P needs to connect 100K resistance to GND
AUX_N needs to connect 100K resistance to 3.3V
eDP_D1-
eDP_D1+
eDP_D0-
eDP_D0+
ETX_AUX+
ETX_AUX-
C10 C9 C8 C7 C13 C17 0.1uF/16V
EDP_TX1-
EDP_TX1+
EDP_TX0-
EDP_TX0+
EDP_AUXP
EDP_AUXN
J3 300E30-0010RA-G3
EDP_TX1-
EDP_TX1+
EDP_TX0-
EDP_TX0+
EDP_AUXP
EDP_AUXN
LCD_VCC5V-2
R60 10K/1%/0402
HPD-2
LCD_BL2_EN
LCD_BL2_PWM
R13 R21 22R/1%/0402
BL2_EN
BL2_PWM
LCD2_I2C_EDID_SCL
LCD2_I2C_EDID_SDA
BL_PWR-2
LCD2_GPIO_EDID_LINK
EDID
J47
R949 0R/1%/0402
LCD2_I2C_EDID_SCL
LCD2_I2C_EDID_SDA
LCD2_GPIO_EDID_LINK
MX2A-3PBAA
Reserved three-way jumper, The default status is high!
SH4 SH1 SH3
2MM SHUNT
EDID
Determine what type of display is connected
U1
TUSD05L4U
EDP_TX1-
EDP_TX1+
EDP_TX0-
EDP_TX0+
U6
TUSD05L4U
EDP_AUXP
EDP_AUXN
ETX_HPD
R743 0R/1%/0402
HPD-2
BL2_EN
BL2_PWM
Z5 ESD5302N
Vantron CONFIDENTIAL
Title
24.MIPI to eDP
Vantron
ChangDu Vantron Technology,LTD
6th/5th Floor, 1st Building,No.9, 3rd Wuliu East Street, Wuhou District ,ChangDu , China 86-28-8512-3930
Size A2
Document Number 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2
Rev <1.0>
Date: Tuesday, November 22, 2022
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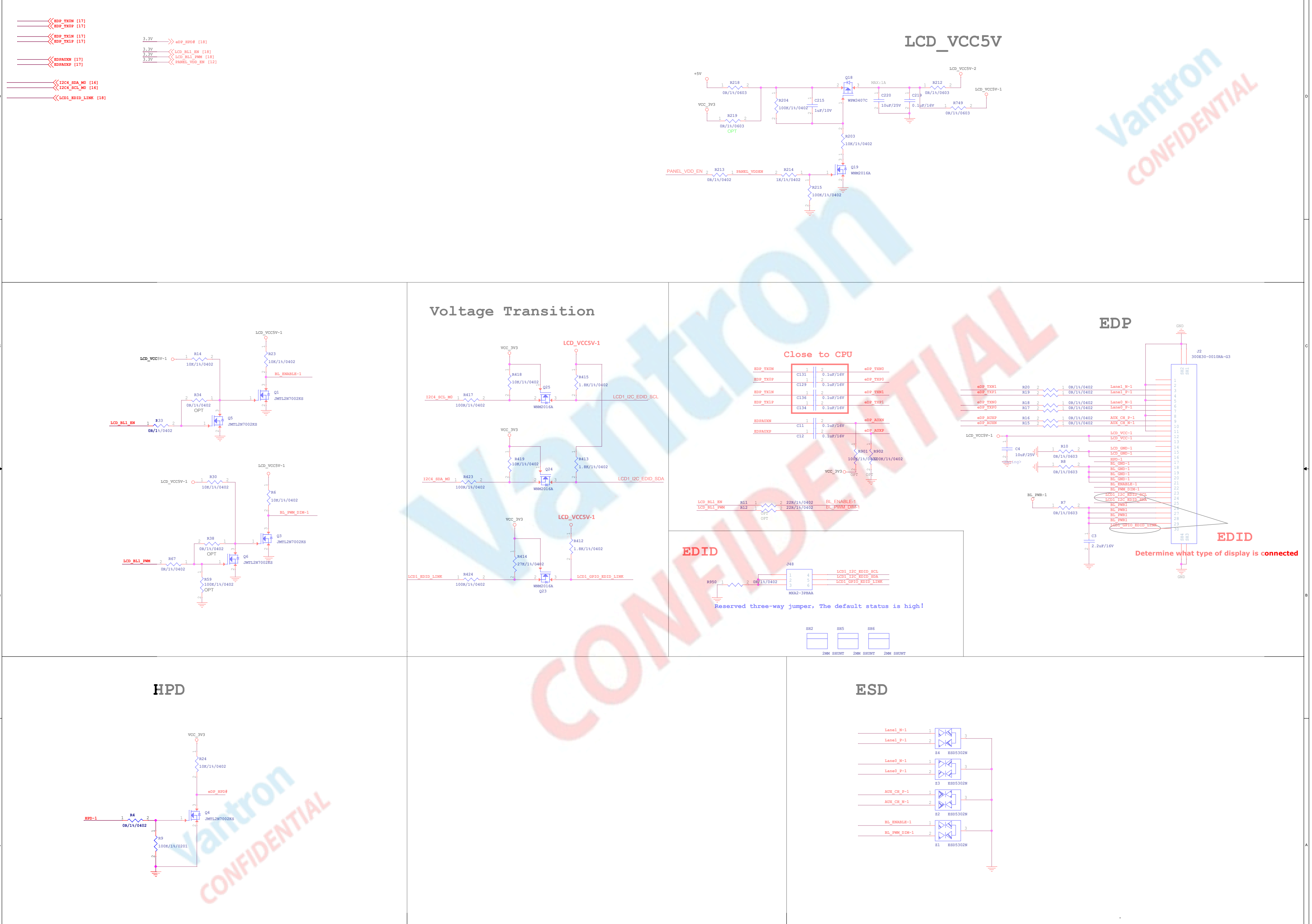
Signal & Power



Title: 25.VO_eDP TX

Vantron

ChengDu Vantron Technology.,LTD

Size: Custom | Document Number: 64088AGG3KL21_SBC-RK3568-NXP1024-ARK-12 | Rev: 1.0

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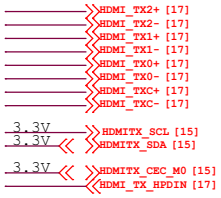
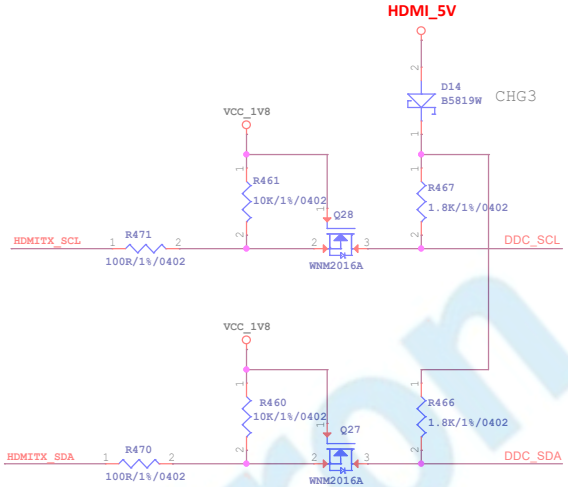
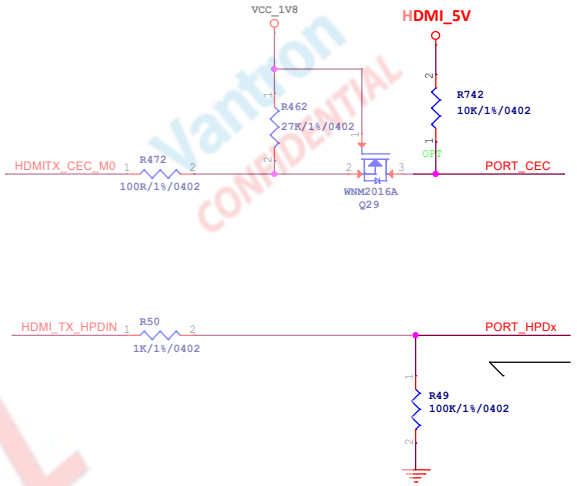
Siganal & Power



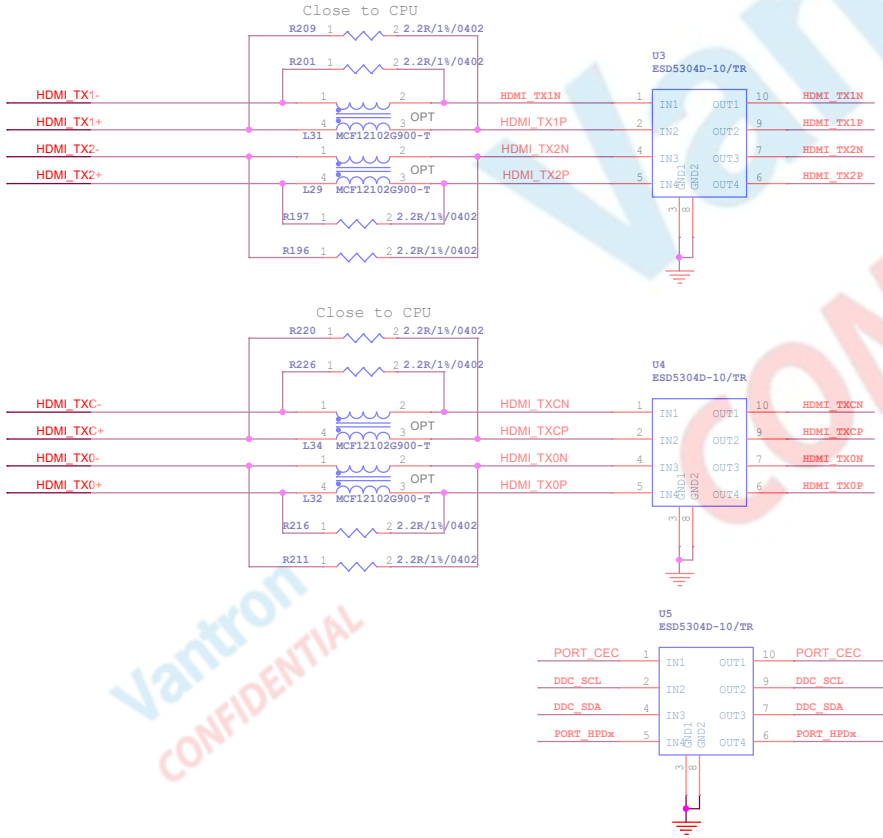
Voltage Transition



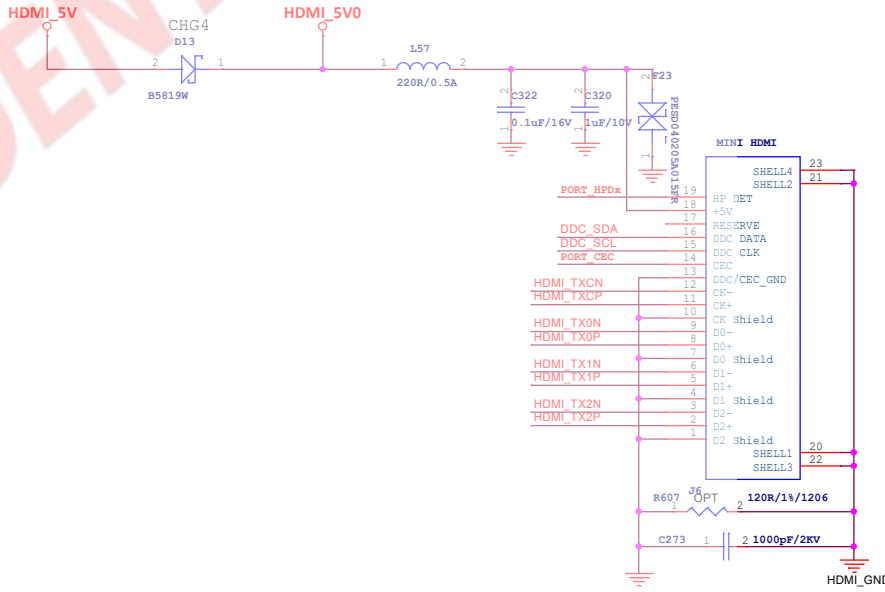
Voltage Transition



ESD & EMI



HDMI



Title	26.VO-HDMI2.0 TX	Vantron
Size	A3	Document Number 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2 Rev 1.0
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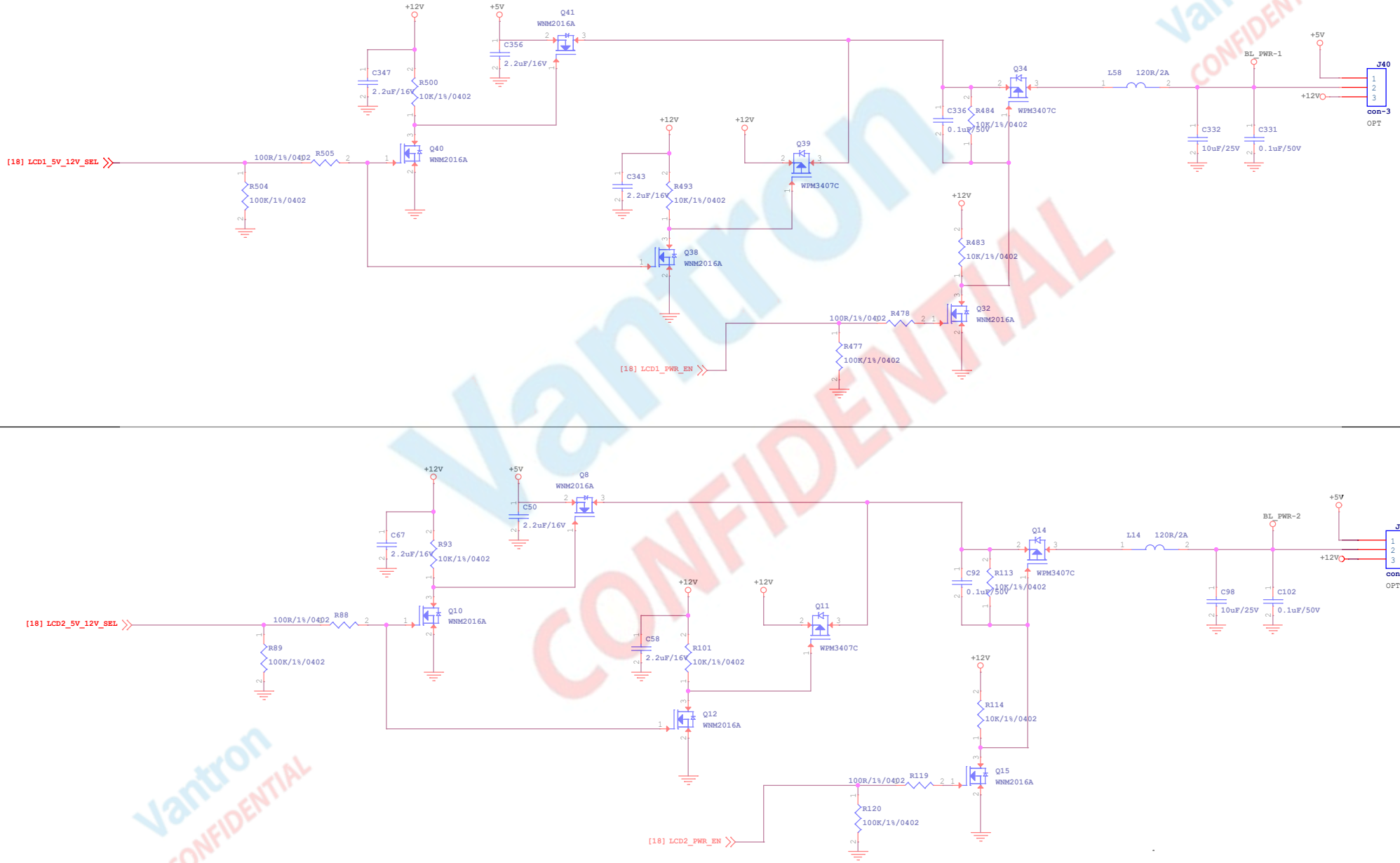
ChengDu Vantron Technology.,LTD
6th/5th Floor, 1st Building,No.9,
3rd Wuke East Street,
Wuhou District, ChengDu , China
86-28-8512-3930



Title: 27.Load Switch		Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District, ChengDu , China 86-28-8512-3930
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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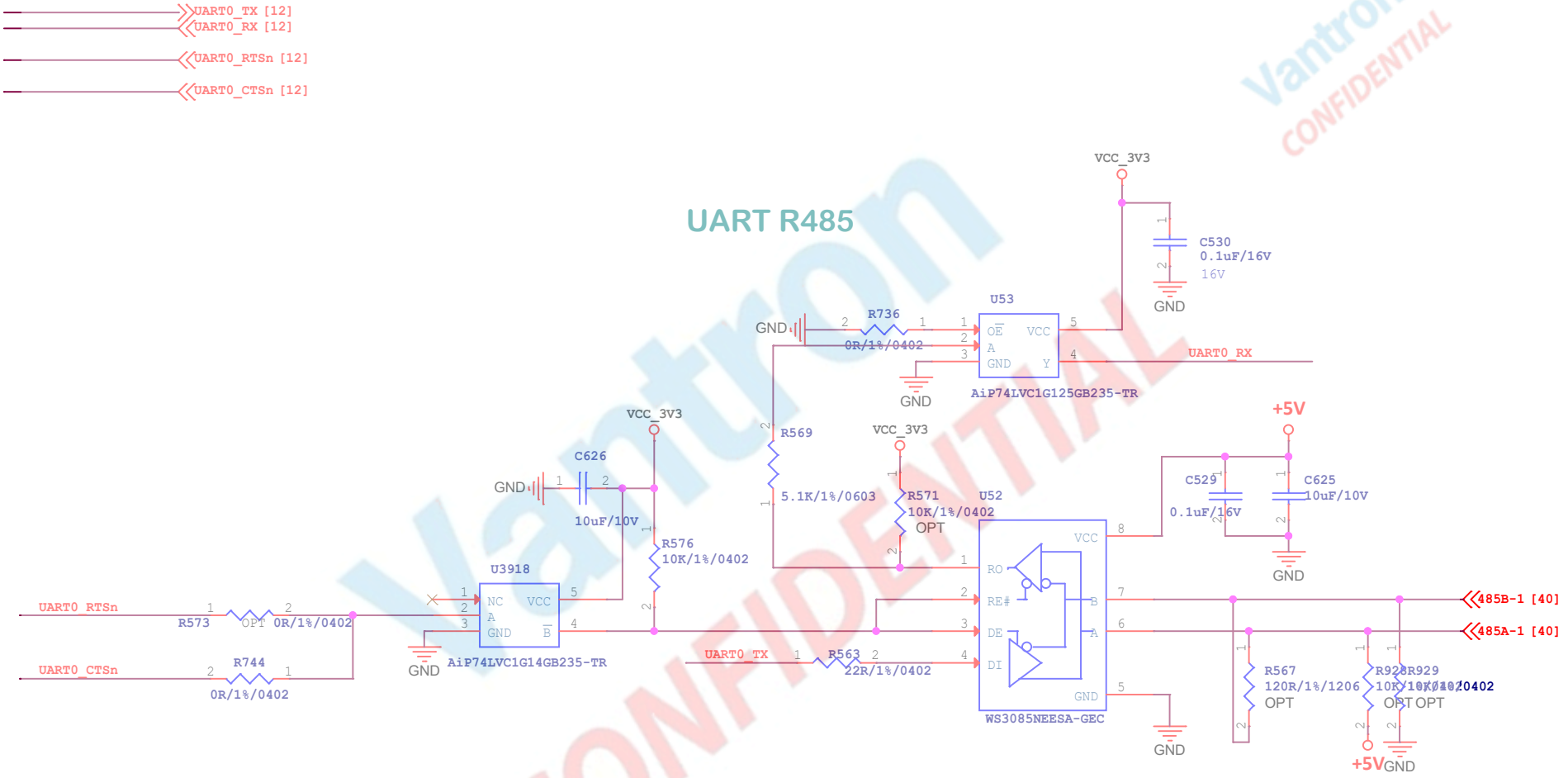

Title	28.RS485	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
Size A4	Document Number 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2	Rev <1.0>
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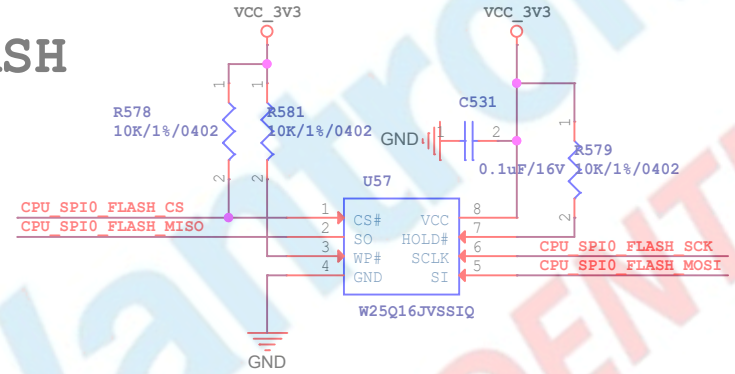
[18] CPU_SPI0_FLASH_CS
[18] CPU_SPI0_FLASH_MISO
[18] CPU_SPI0_FLASH_SCK
[18] CPU_SPI0_FLASH_MOSI

NOR FLASH



Title: 29.SPI_FLASH	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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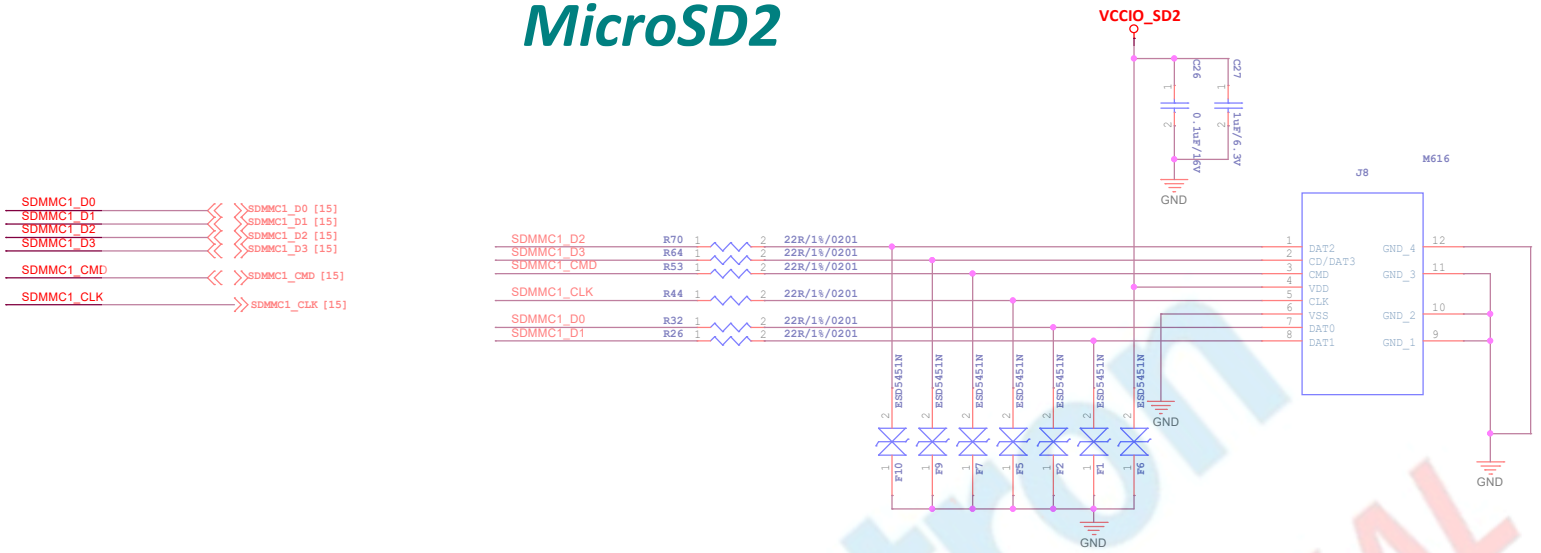
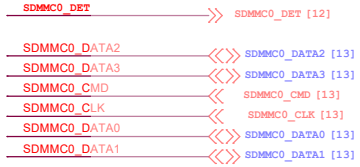
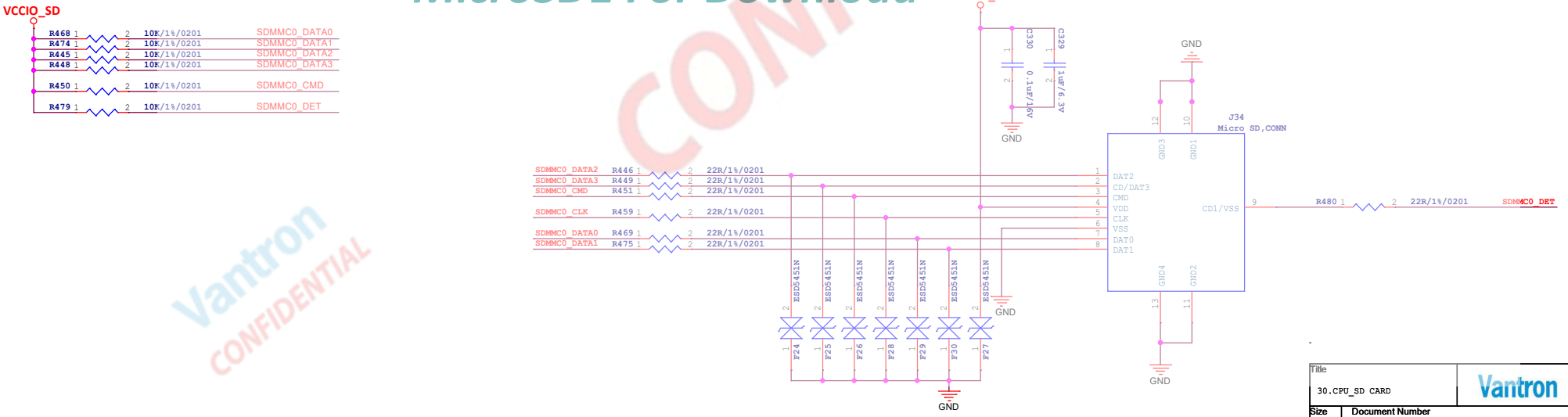
MicroSD2





MicroSD1 For Download



Title: 30.CPU_SD CARD	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District, ChengDu , China 86-28-8512-3930
Size: A3	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2	Rev: <1.0>
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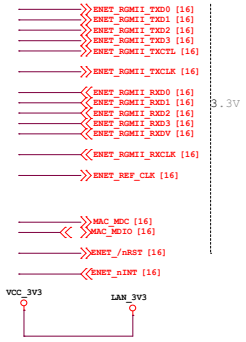
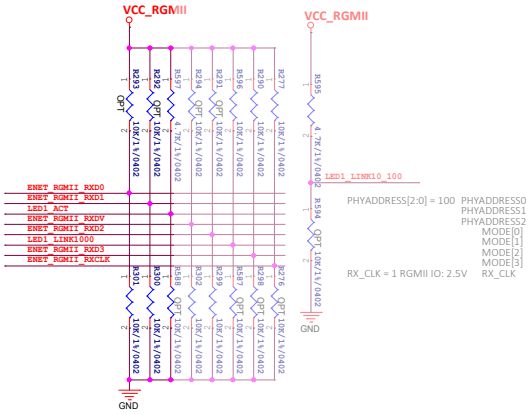
Signal & Power

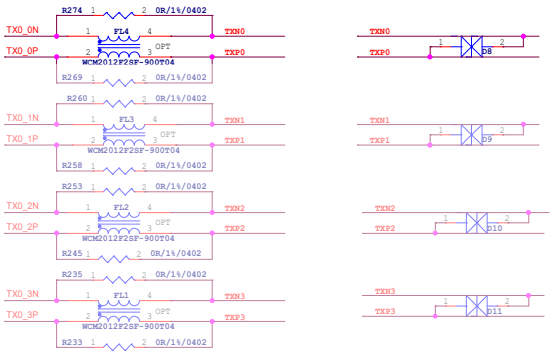




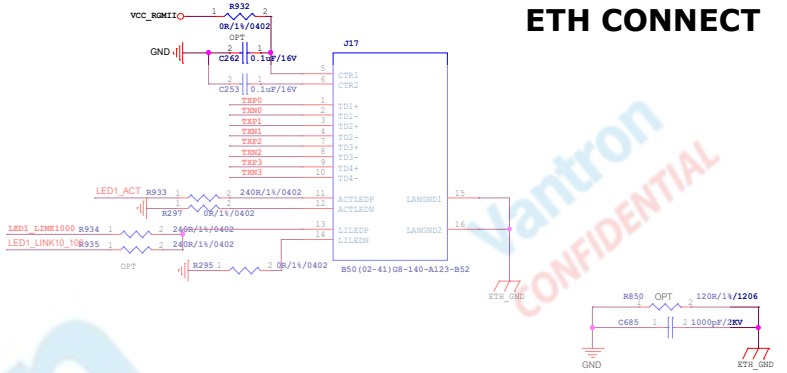
POWER ON STRAPPING

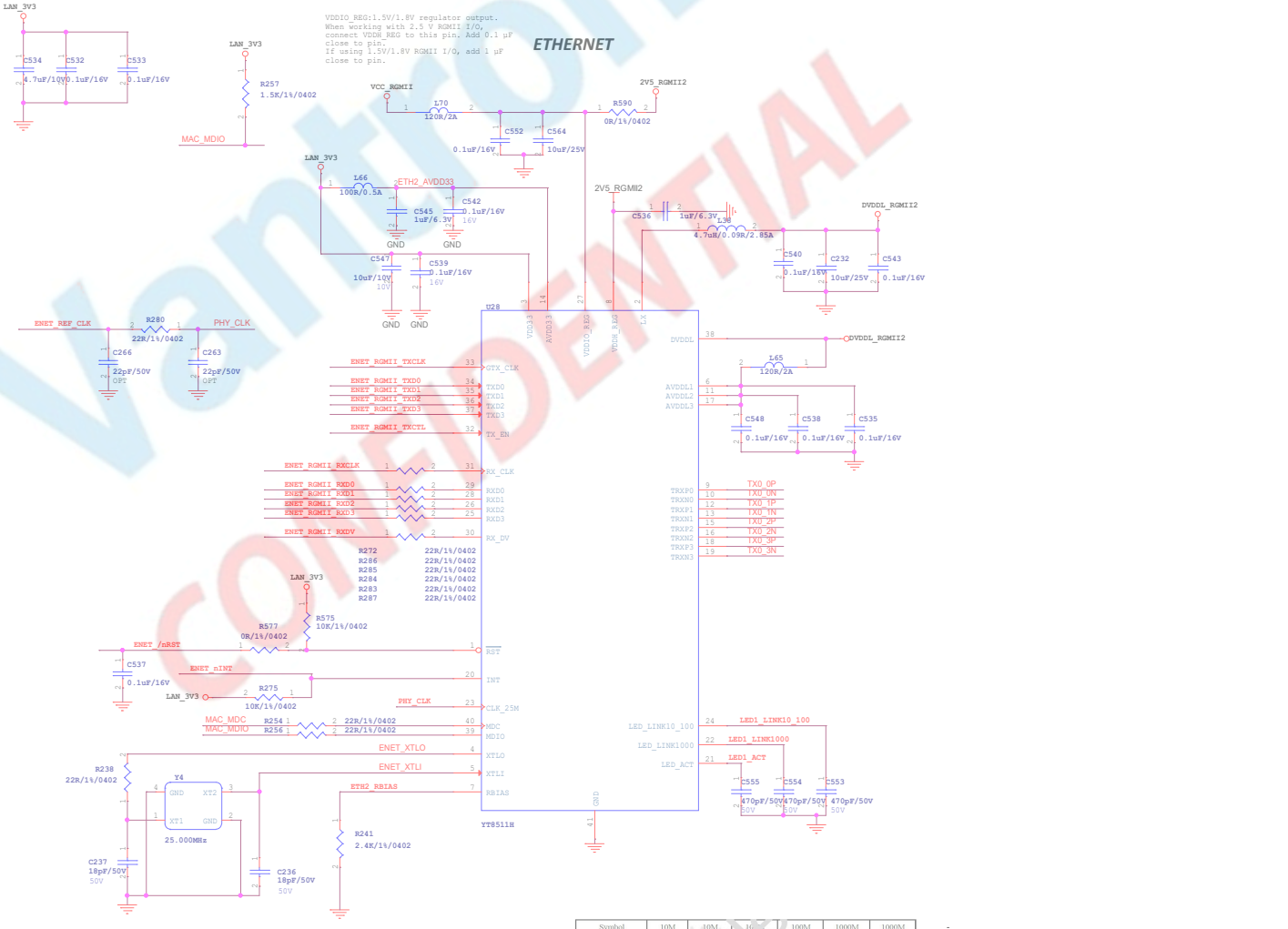
PHY Pin	PHY Core Config	Description	Default
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
LED_ACT	PHYADDRESS2	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	1
RX_DV	RGMII IO power selection	0= RGMII IO 3.3V 1= RGMII IO 2.5V	0
RXD2	PLLON selection	0= PLL off in hibernation when cable unplugged 1= PLL on in hibernation when cable unplugged	0
LED_1000	TEST Mode	0=Test Mode only for internal use 1=Normal Mode, Must external pull up	1
RXD3	Low Power Mode selection	0= Force Low Power mode for shorter cable application 1= Normal cable application	0
LED_10_100	RXC delay enable	0= RXC delay disable 1= RXC delay enable	1
RX_CLK	clk 25m disable	0= clk 25m output enable 1= clk 25m output disable	0

PHY Pin	PHY Core Config	Description	Default
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
LED_ACT	PHYADDRESS2	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	1



ETH CONNECT





Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100	off	off	on	on	off	off
LED_1000	off	off	off	off	on	on
LED_ACT	on	blink	on	blink	on	blink

Title	31.Ethernet-GEPHY_YT8511C	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.5, 3rd Wuke East Street, Wuhou District ,ChengDu , China 86-28-8512-3930
Size	C	Document Number	6408BAGG3RL21 SBC-RK3568-NXP1024-ARK-L2
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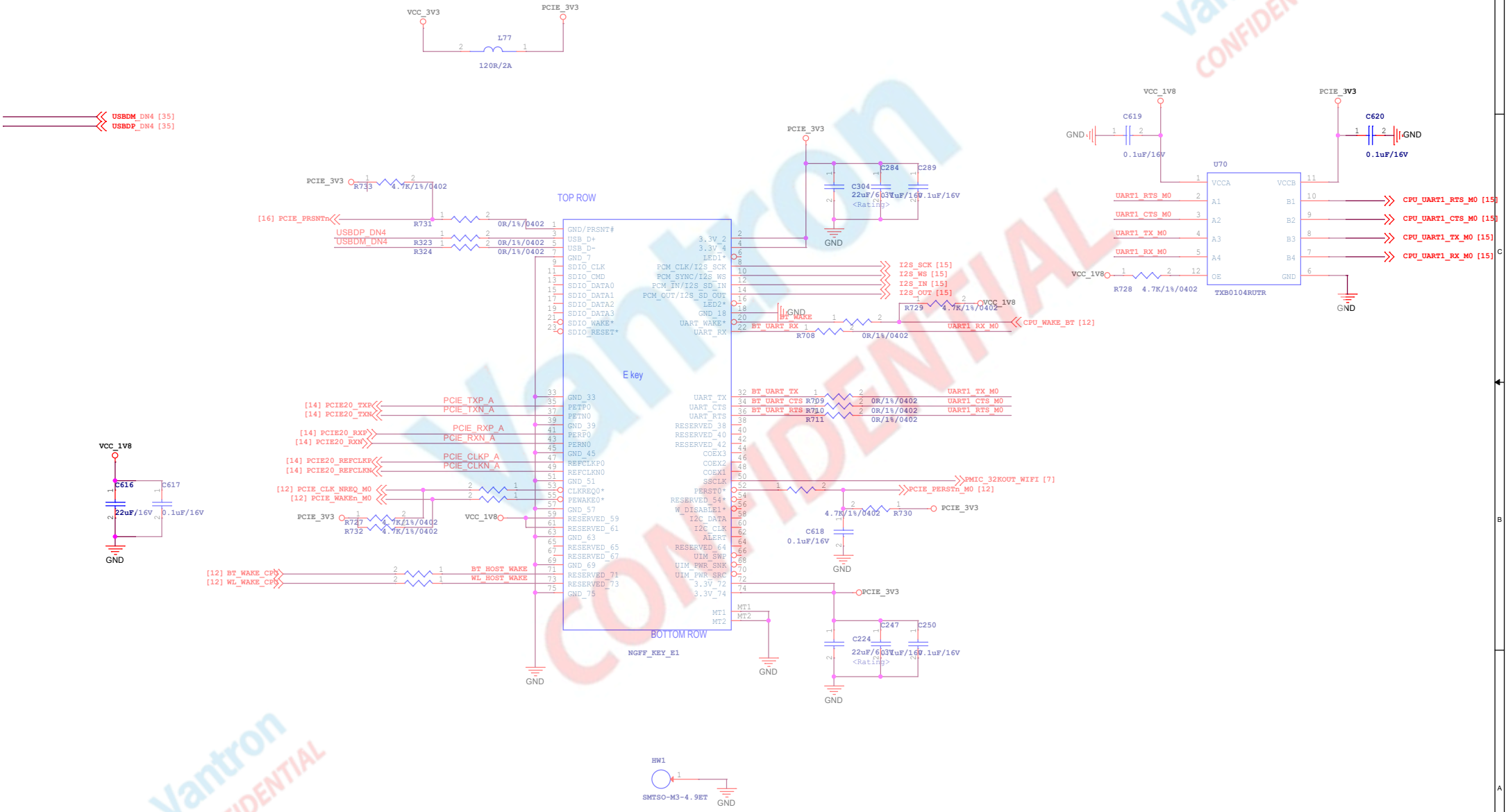
Signal & Power



Title	30.MiniPCIe2.0 Slot	Vantron	ChengDu Vantron Technology,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930
Size	A3	Document Number	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2
Rev	1.0		
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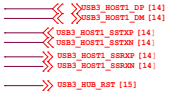
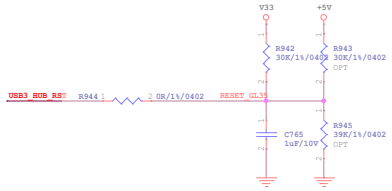
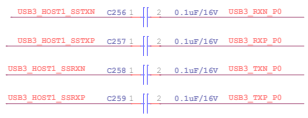
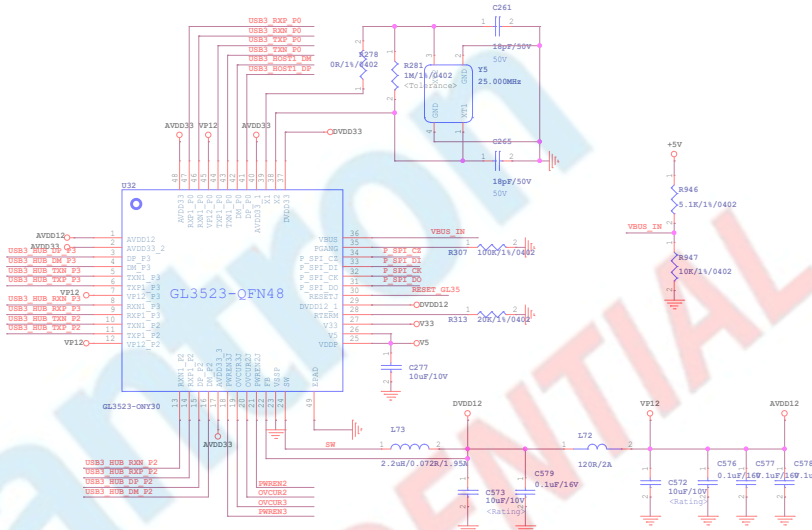
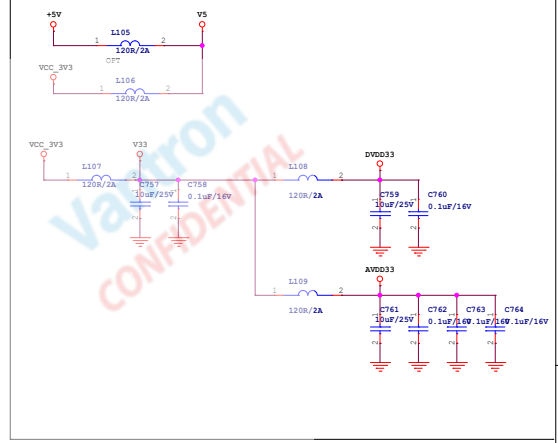
Siganal & Power

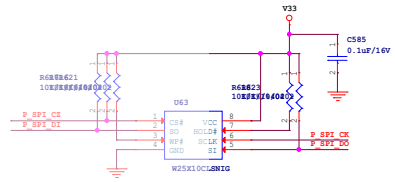


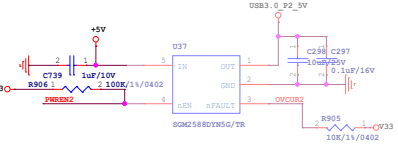


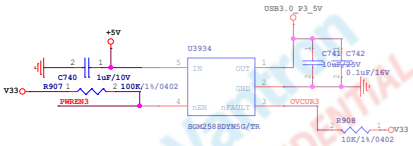


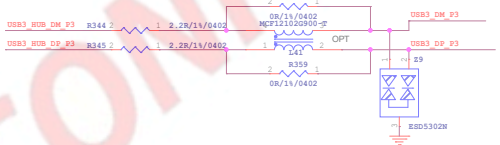


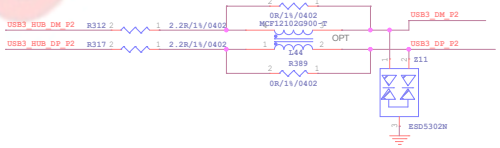


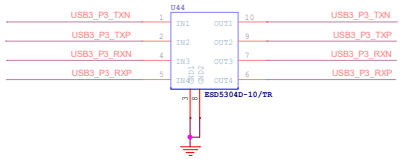


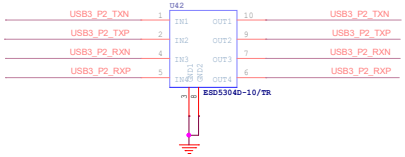




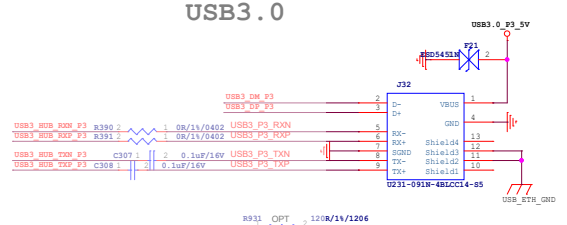


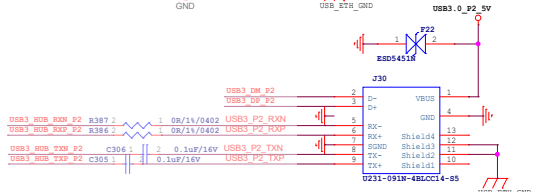






USB3.0





Title: 33.USB3.0	Vantron	ChangDu Vantron Technology,LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuhu East Street, Wuhou District ,ChangDu , China 86-28-8512-3930	
Size: A2	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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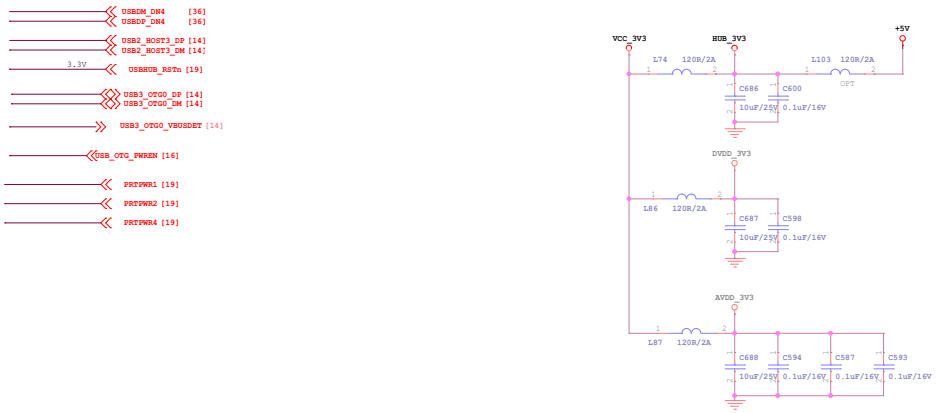
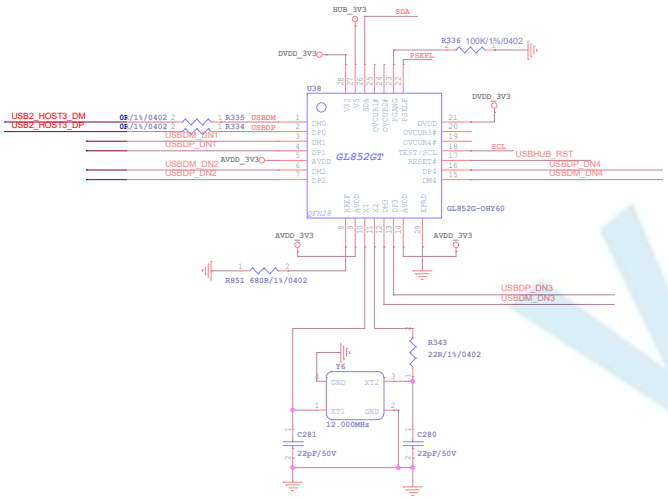
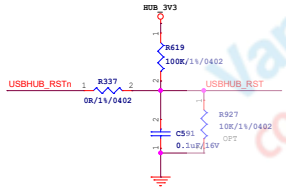
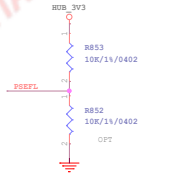


USB HUB CONTROLLER

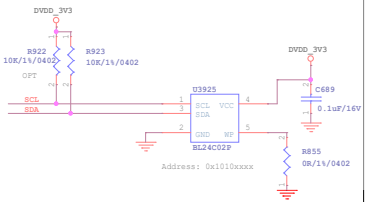
Layout: 90ohm differential pairs

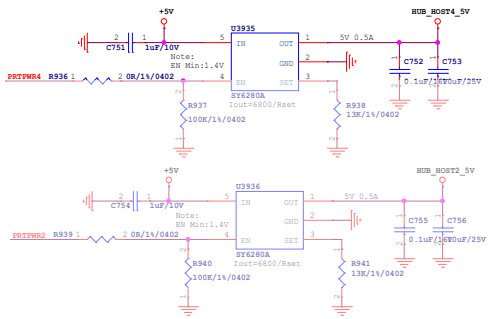


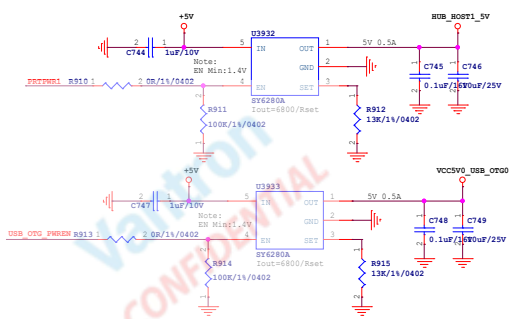




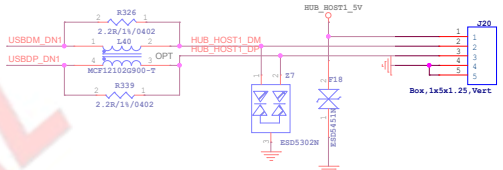
EEPROM



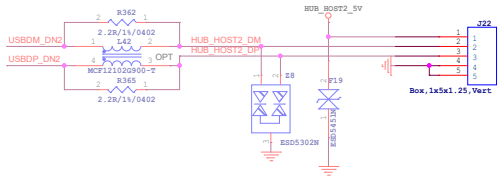




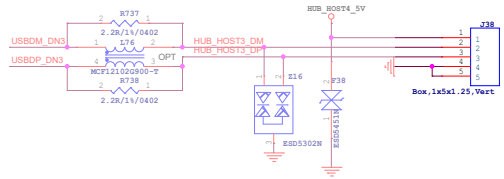
USB2.0



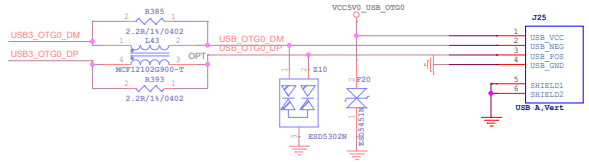
USB2.0

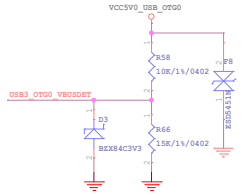


USB2.0



USB2.0 OTG Type-A





Title: 34.USB2.0_USB_HUB_A	Vantron	ChangDu Vantron Technology,LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuhu East Street, Wuhou District,ChangDu ,China 86-28-8512-3930	
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Signal

AM_HPL_OUT [41]
AM_HPR_OUT [41]
SPEAKER_SD_A# [18]
AUDIO_MUTE [18]

AM_HPL_OUT — R195 1K/1%/0402 — C205 100pF/50V — C204 100pF/50V — C160 — 0.1uF/16V — R874 30K/1%/0402 — LINN

AM_HPR_OUT — R148 1K/1%/0402 — C161 — 0.1uF/16V — R875 30K/1%/0402 — RINN

+12V — L98 120R/2A — C720 0.1uF/50V — C721 1000pF/50V — C726 330uF/25V — PVCC — L35 120R/2A — AVCC — C725 10uF/25V — C727 0.1uF/50V

VCC_3V3 — R200 100K/1%/0402 OPT — SPEAKER_SD_A# — R199 0R/1%/0402 — SD — R198 100K/1%/0402

AUDIO_MUTE — R876 0R/1%/0402 OPT — MUTE — R930 100K/1%/0402

PVCCL — R175 100K/1%/0402 — GAIN0 — R176 100K/1%/0402 OPT

PVCCL — R167 100K/1%/0402 — GAIN1 — R168 100K/1%/0402 OPT

AMP 5W

GVDD — C211 10uF/25V

AVCC

PVCC — C728 1000pF/50V

U22 LY8326A

SD — SD, FAULTB

GAIN0, GAIN1 — GAIN0, GAIN1

LINN — C199 0.1uF/16V — R677 30K/1%/0402 — LINP, LINN

RINN — C166 0.1uF/16V — R678 30K/1%/0402 — RINP, RINN

MUTE, MODE — MUTE, MODE, BYPASS

R894 0R/1%/0402 — C188 1uF/16V

GVDD, AVCC, PVCC1, PVCC2

AGND, PAGND1, PAGND2, PAGND3, EPAD

BSTPL, OUTPL, OUTNL, BSTNL, BSTPR, OUTPR, OUTNR, BSTNR, NC

C707 1uF/16V — C708 330pF/50V — R887 10R/1%/0402 OPT — C709 1000pF/50V OPT — L28 120R/2A

L99 120R/2A — C715 1000pF/50V OPT

C713 1uF/16V — C714 330pF/50V — R888 10R/1%/0402 OPT

C716 1uF/16V — C717 330pF/50V — R889 10R/1%/0402 OPT — C718 1000pF/50V OPT — L100 120R/2A

L101 120R/2A — C722 1000pF/50V OPT

C723 1uF/16V — C724 330pF/50V — R890 10R/1%/0402 OPT

BZT24C06 — R202 — R192

SPK_OUTL+A — SPK_OUTL-A — J45 — 53398-0271

SPK

SPK_OUTR+A — SPK_OUTR-A — J13 — 53398-0271

R891 — R892 — BZT24C06

Title	36.AUDIO OUT	
Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuke East Street, Wuhou District, ChengDu , China 86-28-8512-3930	
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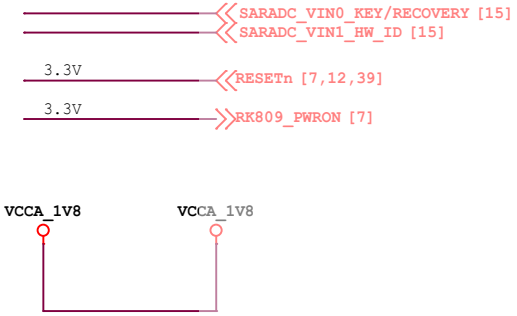
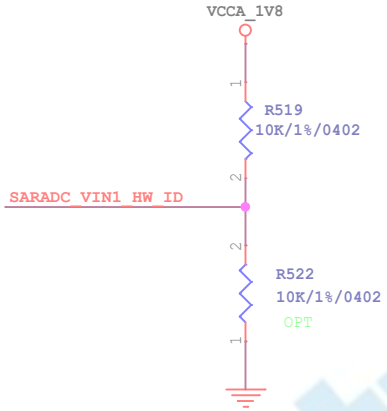
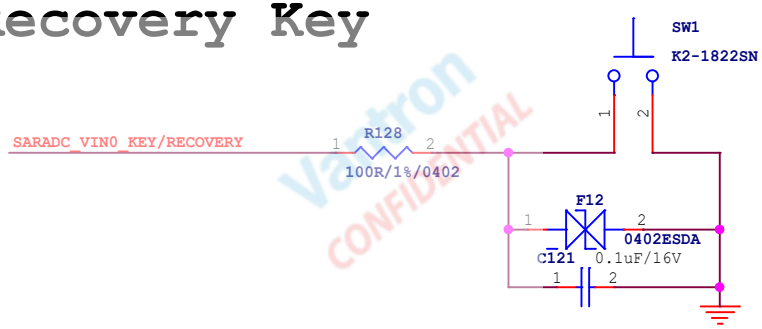
Signal & Power



HW_ID



Recovery Key

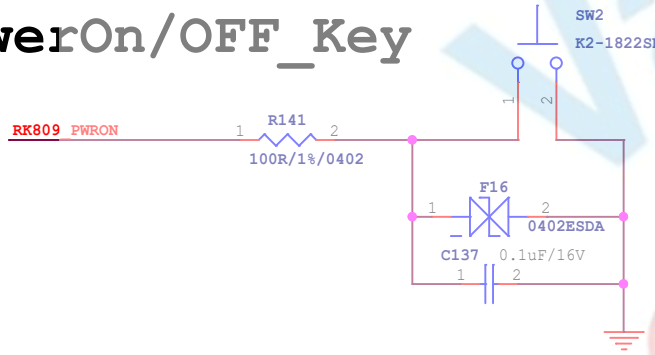


Note:

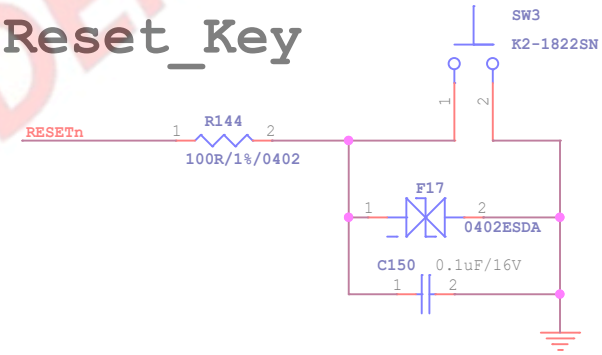
If there is no Key requirement,
It is suggested to reserve a
SW9200 Key to facilitate the
development debug

RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

PowerOn/OFF_Key



Reset_Key



Title: 37.KEY Array/SARADC		ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: 1.0
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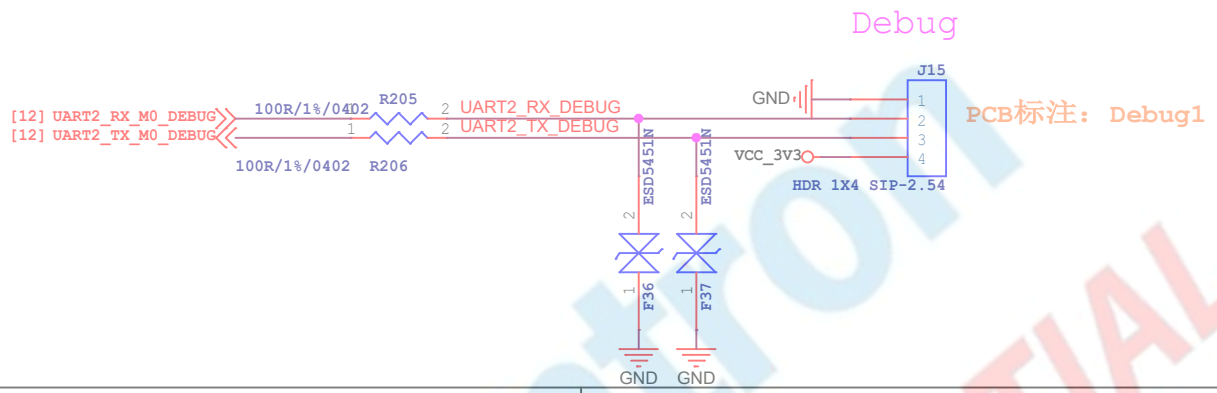
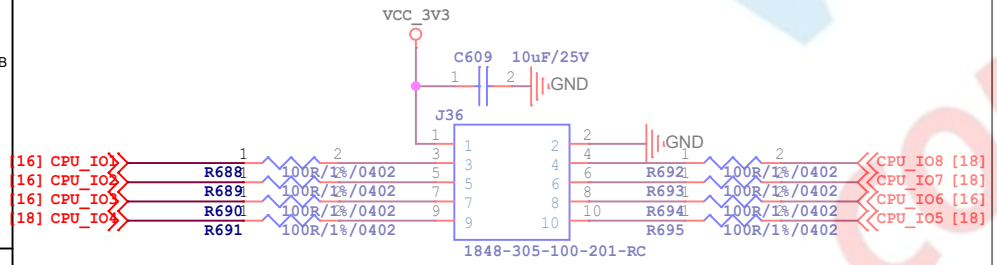
URAT2 Debug



IO expansion



Title: 38.Uart Debug/IO	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: 1.0
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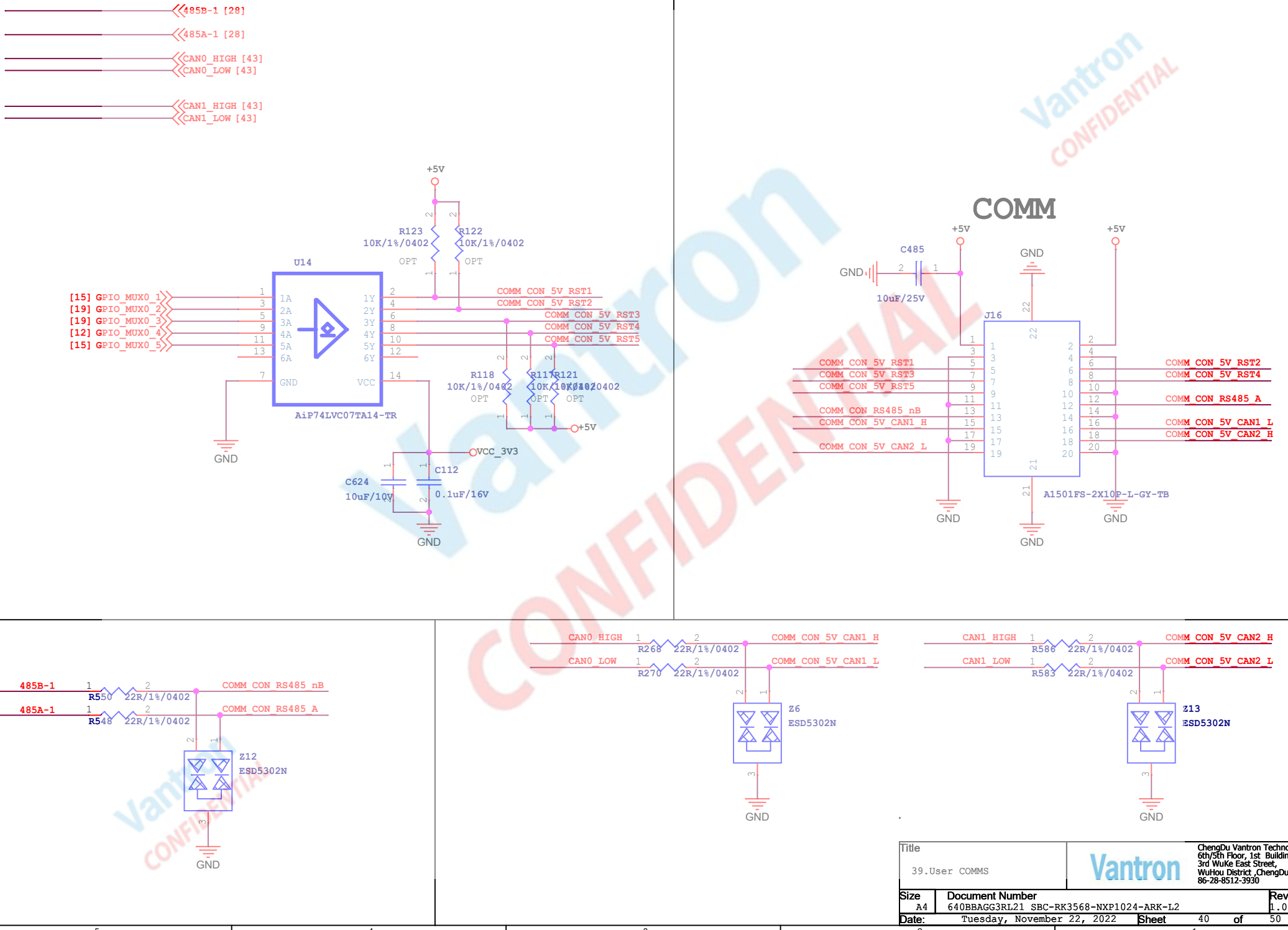

Title	39.User COMMS	Vantron
Size	A4	
Document Number	640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2	Rev 1.0
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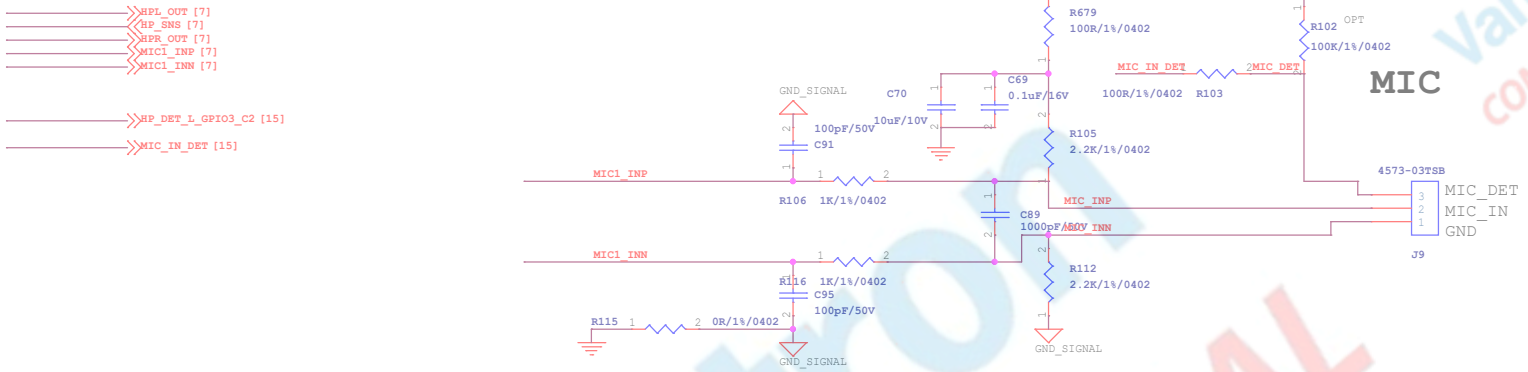
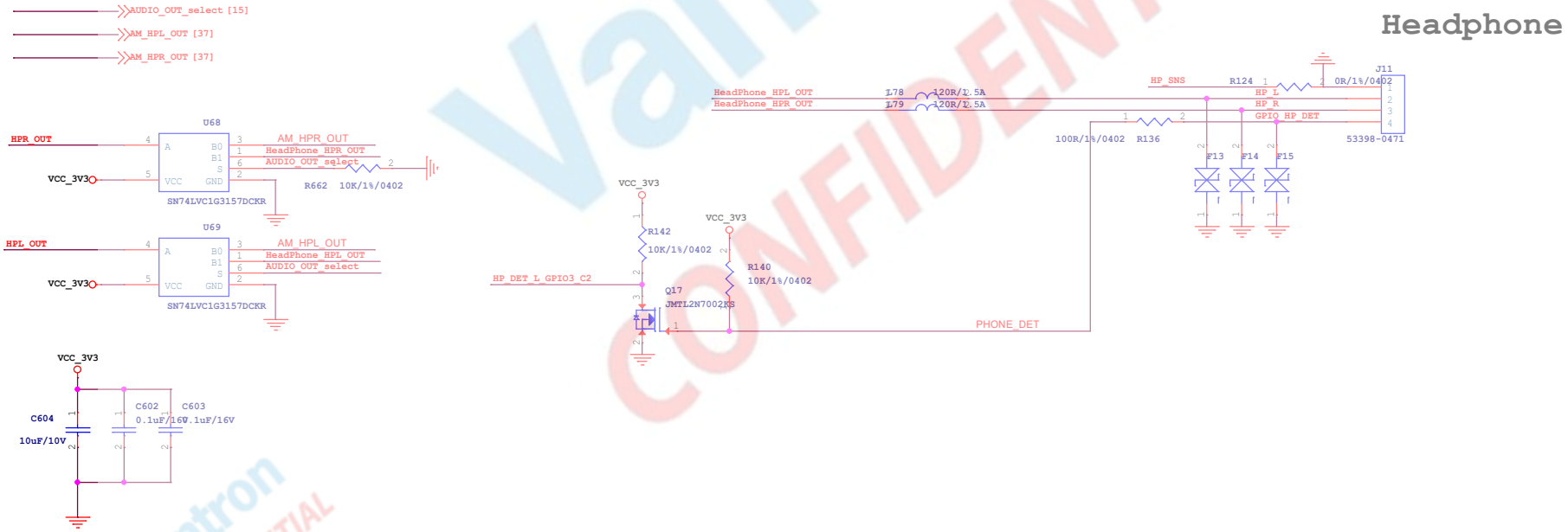
WuHou District ,ChengDu , China
86-28-8512-3930





Title	40.MIC/Headphone	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuke East Street, Wuhou District, ChengDu , China 86-28-8512-3930	
Size	Document Number		Rev
A3	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		1.0
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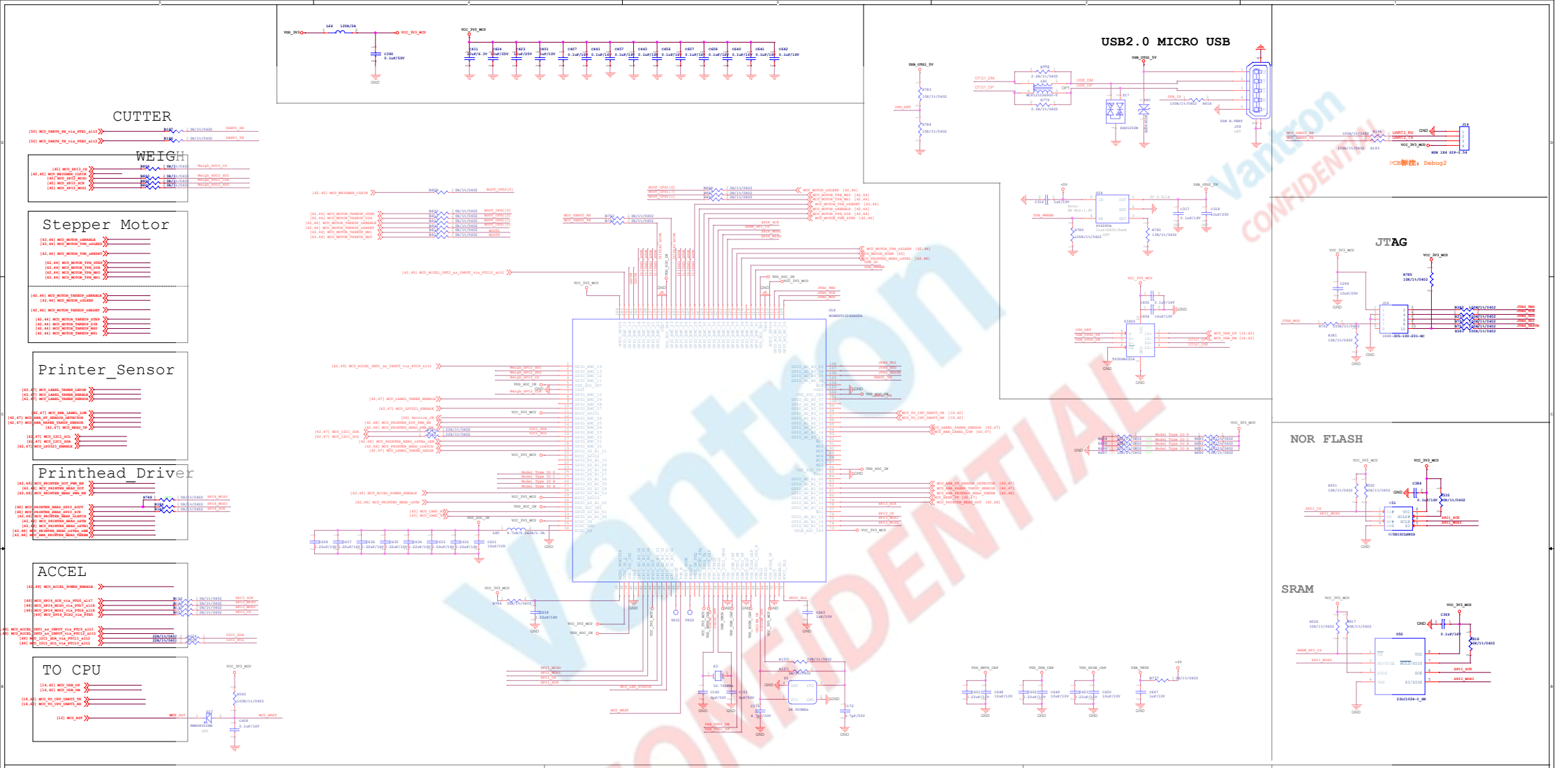
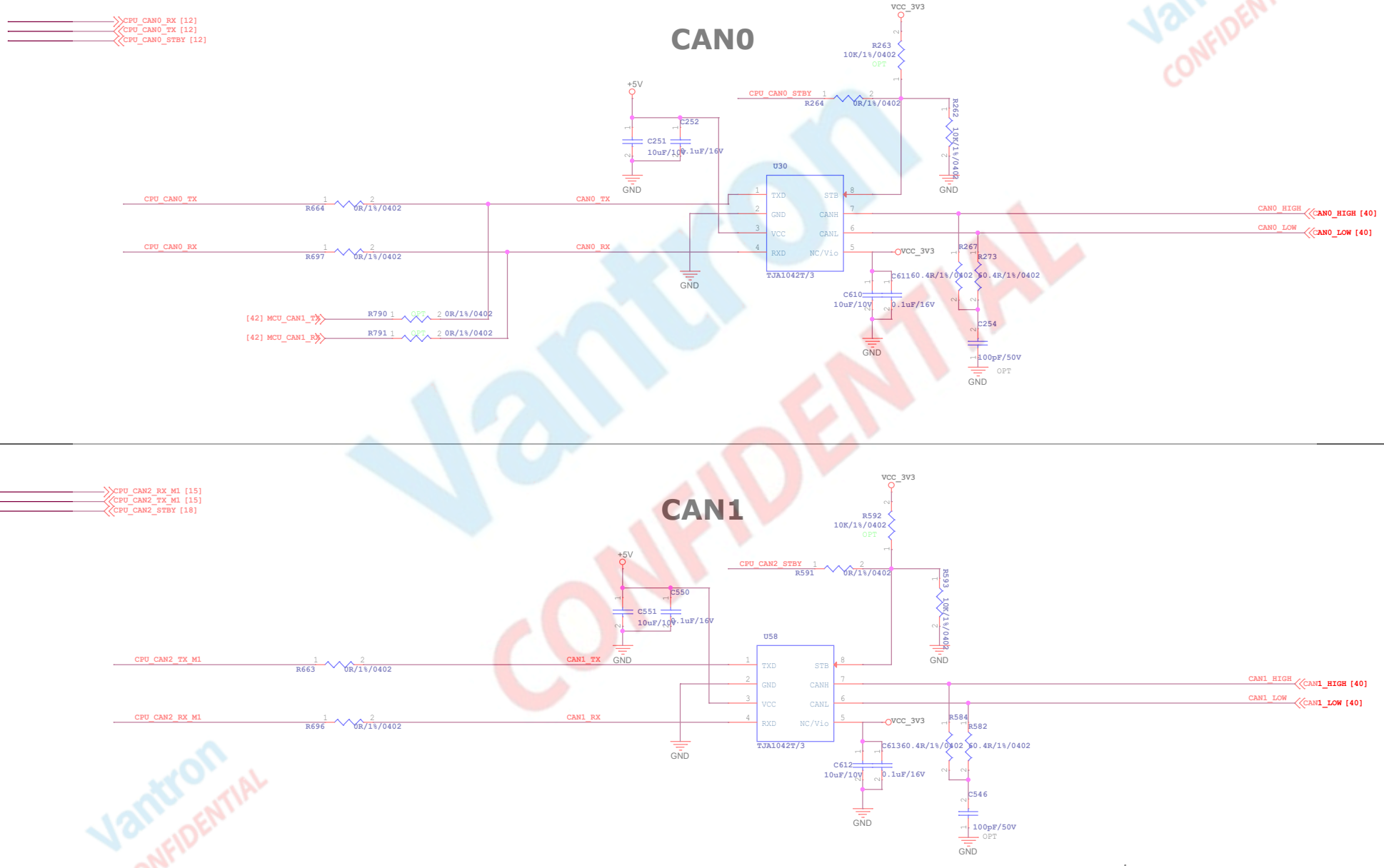


Table 22-1. Boot device select

Boot Device	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]
FlexSPI1 (Serial NOR)	0	0	0	0
SD	0	0	1	x
MMC/eMMC	1	0	x	x
SEMC (NAND)	0	1	x	x
SEMC (NOR)	0	0	0	1

Table 9-2. Boot MODE pin settings

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot
11	Reserved



Title	42.CPU_CAN0/1	
Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District, ChengDu , China 86-28-8512-3930	
Size	Document Number	Rev
A3	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2	<1.0>
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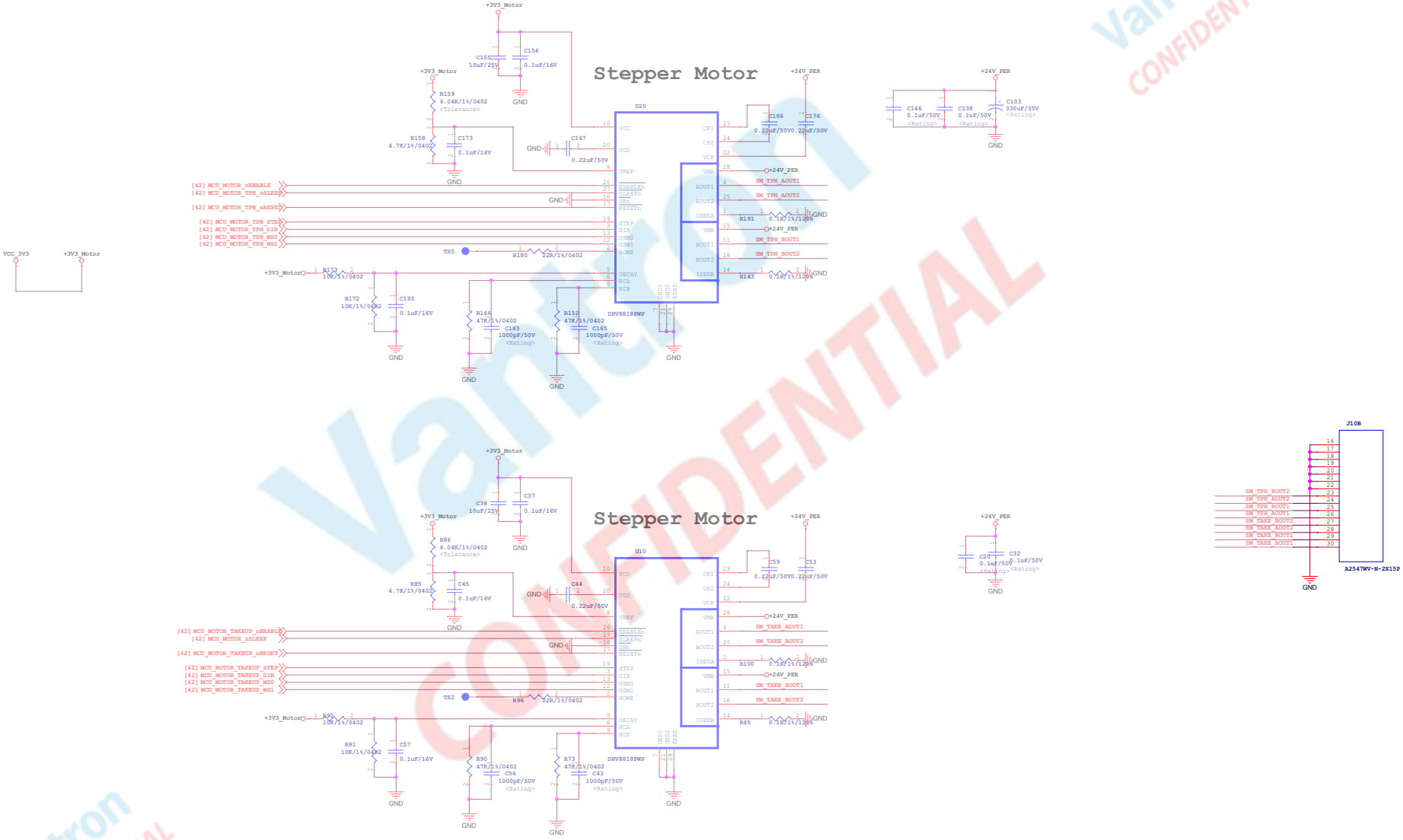

Title	43.MCU_Motor
Vantron	ChengDu Vantron Technology.LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuhu East Street, Wuhou District ,ChengDu , China 86-28-8512-3930
Size	A2
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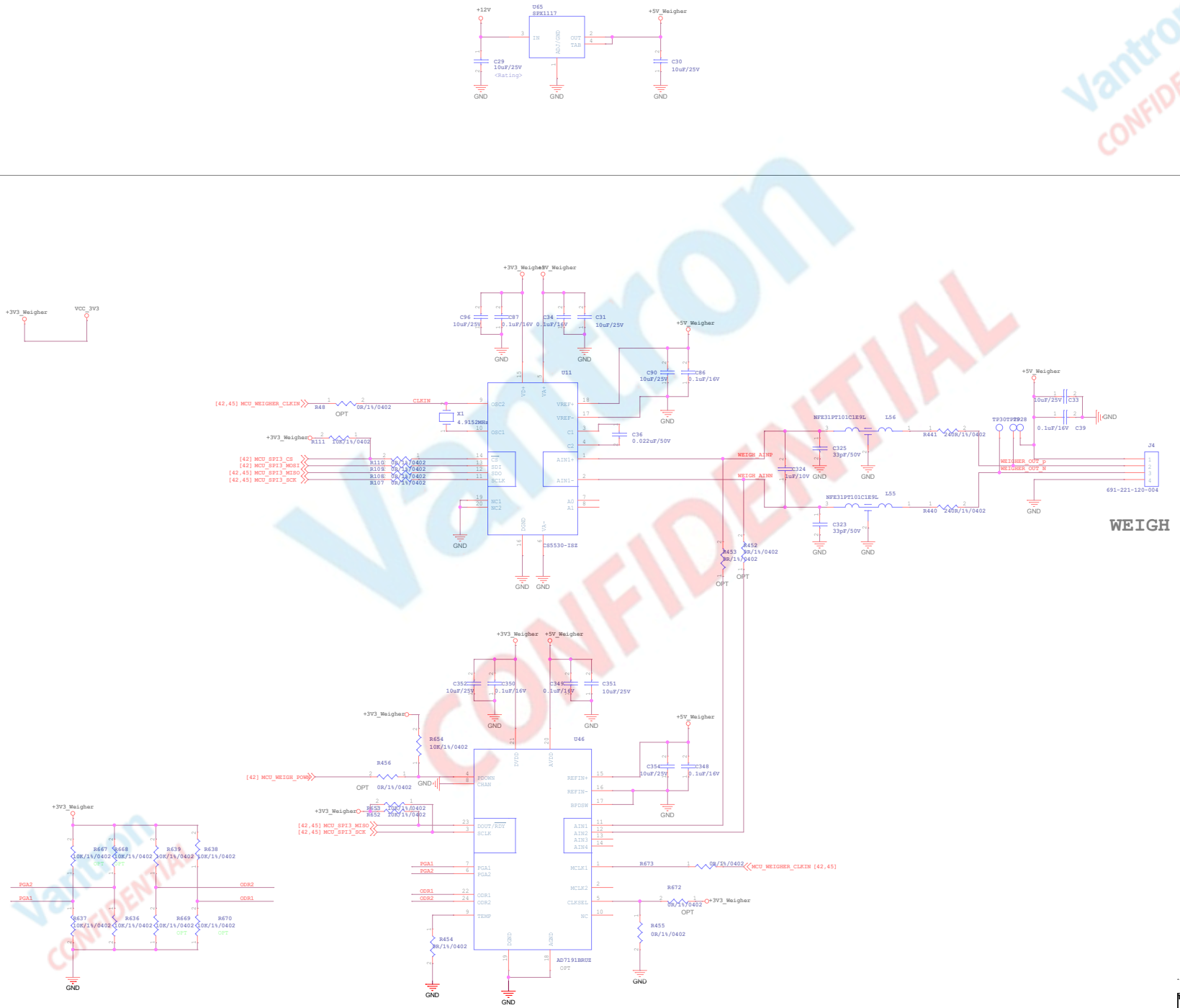

Title: 44.Weigh_ADC	Vantron	ChengDu Vantron Technology.LTD 6th/5th Floor, 1st Building,No.9, 3rd Wuhu East Street, Wuhou District ,ChengDu , China 86-28-8512-3930	
Size: A2	Document Number: 640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2		Rev: 1.0
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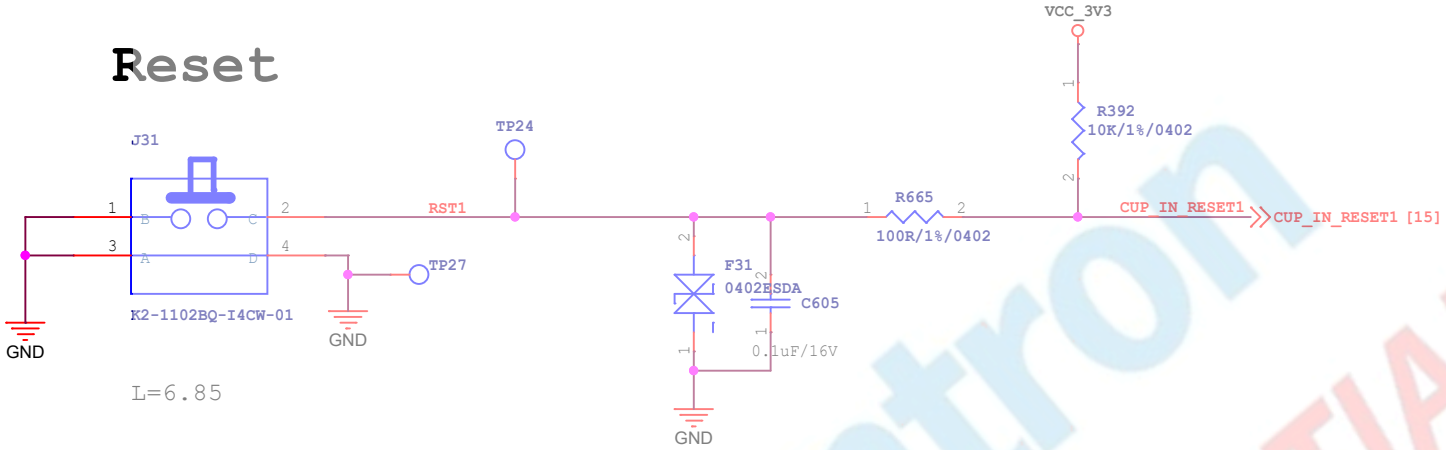

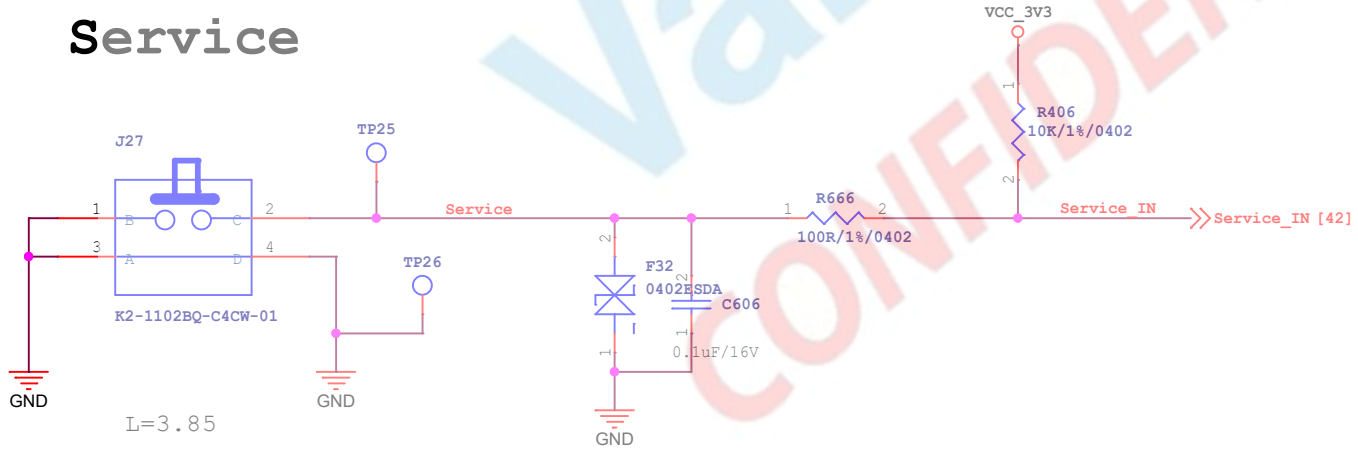

Title: 45.Reset Switch	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: 1.0
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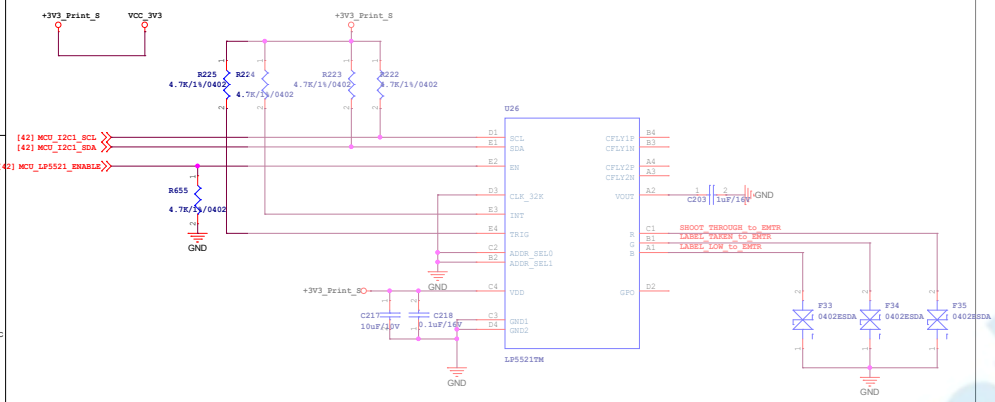
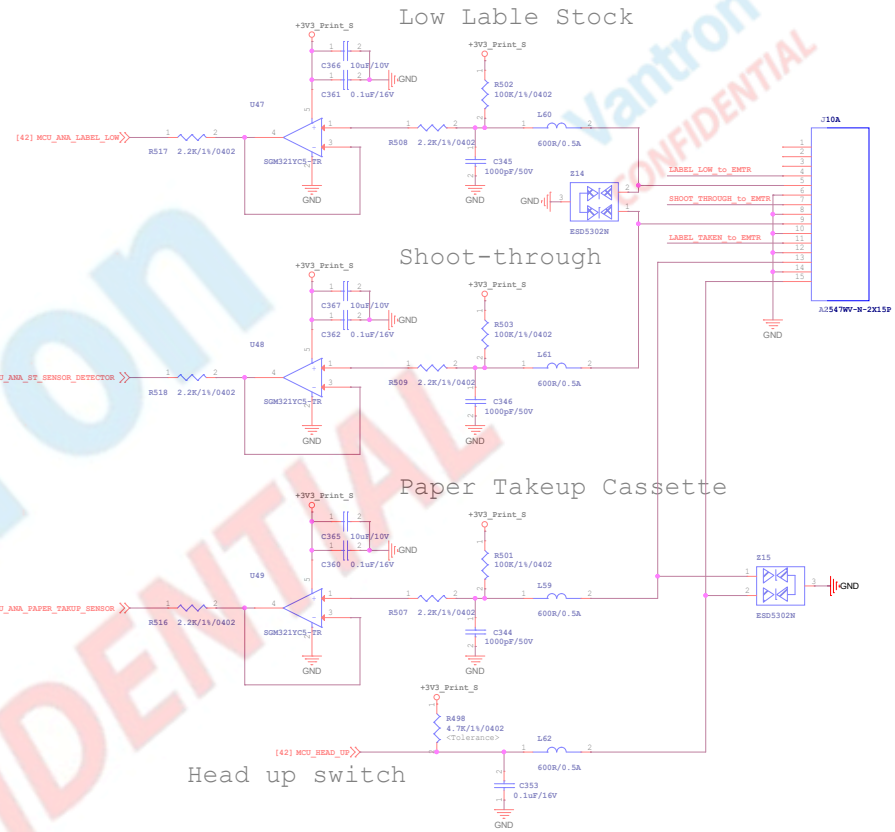
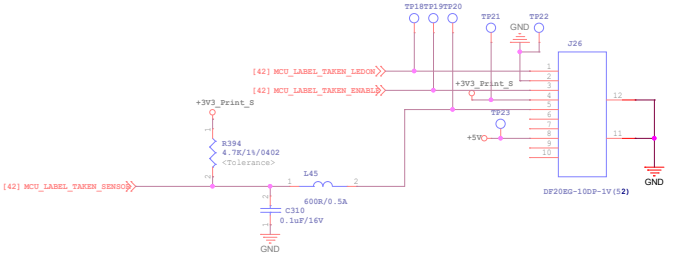


Address: 0X64





Title	46.Printer_Sensor	Vantron
Size	Document Number	Rev
A2	640BBAG03RL21 SBC-RK3568-NXP1024-ARK-L2	1.0
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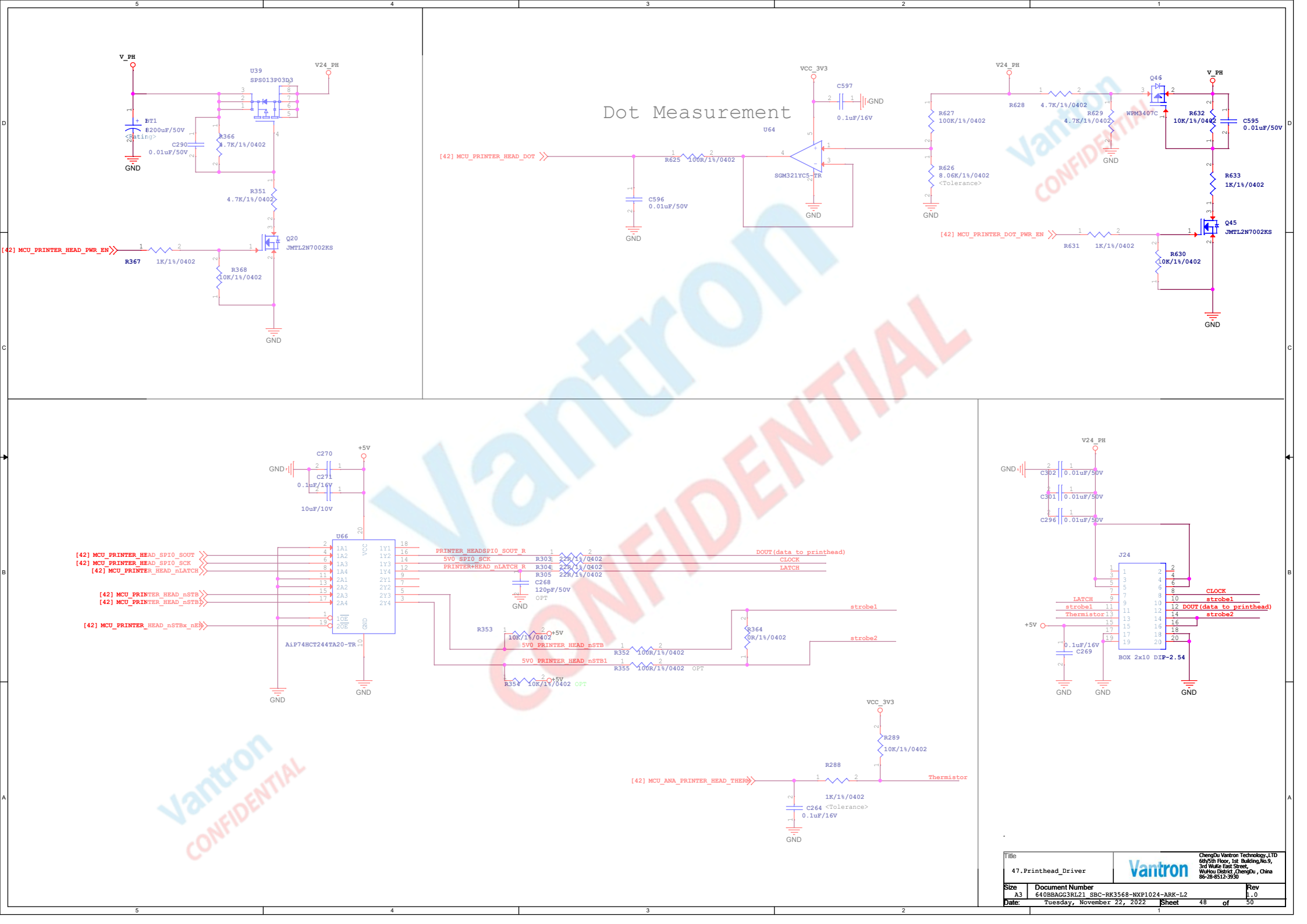
6th/5th Floor, 1st Building,No.9,
3rd Wuhu East Street,
Wuhou District ,ChengDu , China
86-28-8512-3930



Title	47.Printhead_Driver		
Size	A3	Document Number	640BBAGG3RL21_SBC-RK3568-NXP1024-ARK-L2
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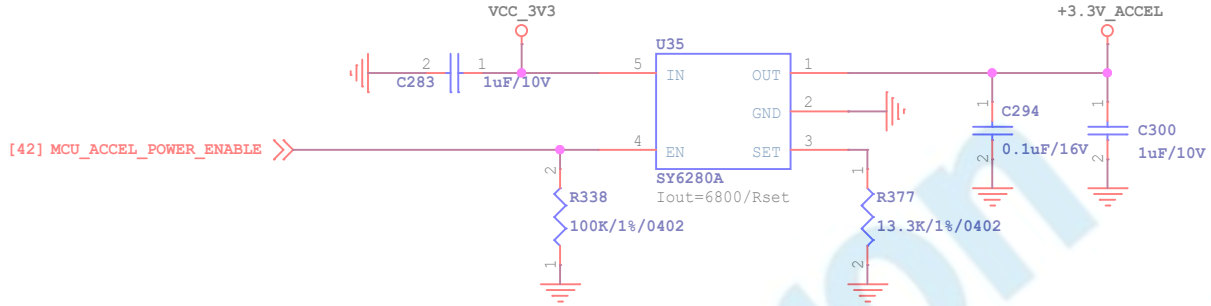
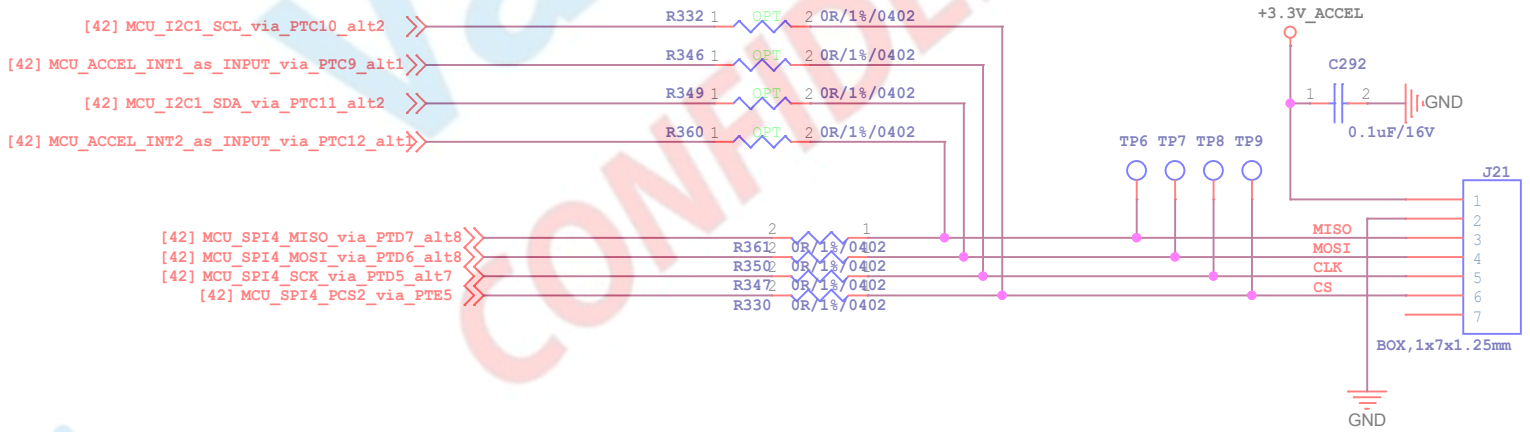
6th/5th Floor, 1st Building,No.9,
3rd Wuke East Street,
Wuhou District, ChengDu , China
86-28-8512-3930



Accelerometer



Title: 48.ACCEL	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: 1.0
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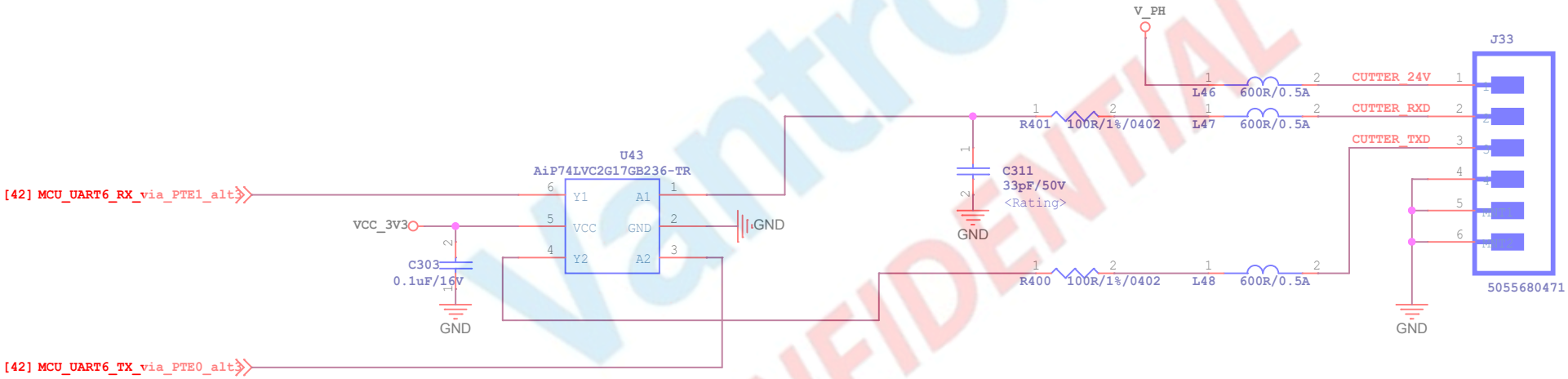
CUTTER



Title: 49.CUTTER	Vantron	ChengDu Vantron Technology.,LTD 6th/5th Floor, 1st Building,No.9, 3rd WuKe East Street, WuHou District ,ChengDu , China 86-28-8512-3930	
Size: A4	Document Number: 640BBAGG3RL21 SBC-RK3568-NXP1024-ARK-L2		Rev: <1.0>
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