VTX1 Ternary SoC Architecture

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Summary

The VTX1 is a balanced ternary logic System-on-Chip (SoC) that implements a novel approach to computing using digital representation of three-state logic (-1, 0, +1) while maintaining binary compatibility. This document provides a comprehensive technical specification of the VTX1 architecture, including its core processing unit, memory subsystem, I/O peripherals, and system management features.

Features

1. Small footprint under 10000 Gates
2. Balanced digital ternary logic implementation
3. VLIW architecture with 3-operation serial or parallel execution
4. Unified TCU with ALU, FPU, and SIMD capabilities
5. Microcode-based complex operation handling
6. Power-efficient design with multiple clock domains

Target Applications

- Digital signal processing
- Embedded control systems
- Scientific computing
- Educational platforms
- Research and development

Performance Targets

- Small implementation footprint under 10K gates
- Power efficiency: See Power Consumption Specifications for complete dual-voltage power specifications
- Area: ~5×5mm die
- Clock frequency: Up to 100 MHz

Overview

The VTX1 is a balanced ternary logic System-on-Chip (SoC) designed for both FPGA prototyping and future silicon implementation. It is using digital representation of balanced ternary logic (trits: −1, 0, +1) implemented internally using CMOS voltage levels, while maintaining binary interfaces externally for compatibility.

Features

- Balanced ternary logic core with binary I/O compatibility
- Energy-efficient arithmetic operations
- Analog-domain compatibility
- Simplified logic circuits
- Flexible and scalable architecture
- FPGA prototyping ready with ASIC fabrication path

Design Principles

- Ternary logic implementation for improved arithmetic efficiency
- Internal balanced ternary logic for all processing and registers
- External binary interface compatibility
- HDL implementation in Icarus Verilog
- Documentation-first approach

Design Decisions

1. **Ternary Logic Implementation**
    - Rationale: Improved arithmetic efficiency and performance
    - Trade-offs: Increased design complexity vs. performance benefits
    - Impact: Affects all internal operations and external interfaces
2. **VLIW Architecture**
    - Rationale: Maximize parallel execution in ternary domain while maintainting small footprint
    - Trade-offs: Code density vs. performance
    - Impact: Compiler complexity and instruction encoding
3. **Microcode Approach**
    - Rationale: Flexible implementation of complex operations, reduce gate count
    - Trade-offs: ROM size vs. flexibility
    - Impact: System performance and ability to upgrade
4. **Memory Hierarchy**
    - Rationale: Balance performance and power consumption
    - Trade-offs: Cache size vs. area

- Impact: System performance and power efficiency

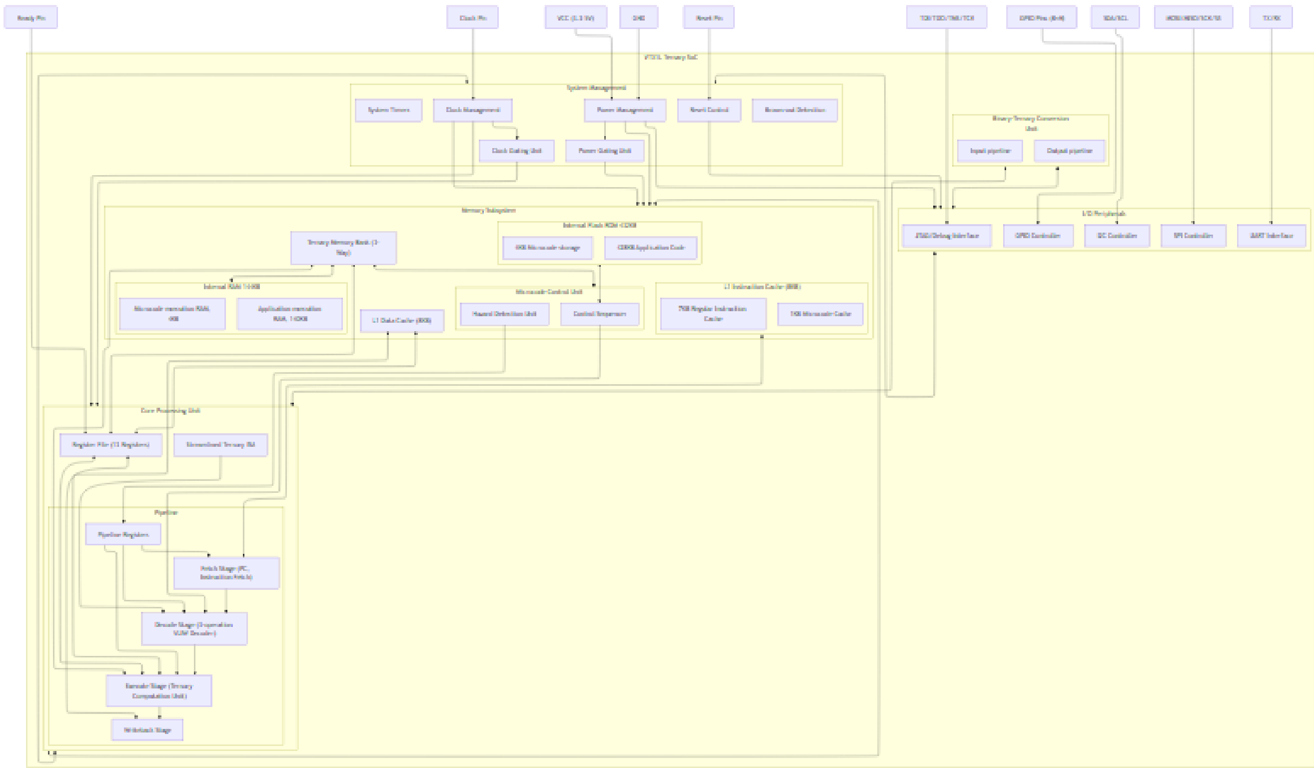
Design Guidelines

1. **RTL Implementation**
   - Use synchronous design practices
   - Implement clock gating for power efficiency
   - Follow ternary logic encoding standards
   - Use parameterized modules for flexibility
2. **Verification Strategy**
   - Unit-level testing for all modules
   - System-level simulation
   - Formal verification for critical paths
   - Power-aware verification
3. **Physical Implementation**
   - Use standard cell libraries
   - Implement power domains
   - Follow clock tree synthesis guidelines
   - Consider testability

Comparison

Feature	VTX1	ARM Cortex-M4	RISC-V RV32IM	ESP32
Logic Type	Ternary	Binary	Binary	Binary
ISA Type	VLIW	RISC	RISC	RISC
Pipeline	4-stage	3-stage	5-stage	2-stage
Clock Speed	100MHz	168MHz	100MHz	240MHz
Power (Active)	150mA	150mA	80mA	120mA
Area	25mm²	20mm²	15mm²	30mm²

System Block Diagram



Balanced Ternary Logic Implementation

All internal components operate using balanced ternary representation, implemented using 5V-compatible voltage levels for improved compatibility with legacy systems while maintaining ternary logic functionality.

Ternary Logic Encoding

Authoritative Definition: This section provides the complete specification for ternary logic encoding used throughout the VTX1 SoC. All other references in the documentation refer to this definition.

Digital Encoding and Voltage Levels:

State	Digital Encoding	Voltage Level	Voltage Range	Description
`TRIT_NEG`	`2'b00`	0.0V	0.0V ± 0.5V	Digital encoding for -1 (balanced ternary)
`TRIT_ZERO`	`2'b01`	2.5V	2.5V ± 0.5V	Digital encoding for 0 (balanced ternary)
`TRIT_POS`	`2'b10`	5.0V	5.0V ± 0.5V	Digital encoding for +1 (balanced ternary)
`TRIT_INVALID`	`2'b11`	-	-	Reserved for error detection

Technical Specifications:

- **Supply Voltage**: 5.0 V ±5% (compatible with legacy systems)
- **Noise Margins**: ±0.5V around each logic level
- **Drive Strength**: 4 mA minimum per output
- **Input Thresholds**: VIL = 0.5 V max, VIH = 4.5 V min
- **Implementation**: 5V-compatible using standard CMOS level shifters

- **ESD Protection**: 2 kV HBM, 200 V MM for 5V-tolerant operation

Verilog Implementation:

```
localparam TRIT_NEG = 2'b00;   // -1 (0.0V)
localparam TRIT_ZERO = 2'b01;  // 0  (2.5V)
localparam TRIT_POS = 2'b10;   // +1 (5.0V)
localparam TRIT_X = 2'b11;     // Invalid or undetermined
```

Binary-Ternary Conversions

Note: For complete encoding specifications, see Ternary Logic Encoding above.

Quick Reference:

- **Trit to Binary**: Each trit is represented by a 2-bit binary value per the authoritative encoding table.
- **Binary to Trit**: 2-bit binary values are mapped to their corresponding trit values as defined in the encoding specification.

Trit Gate implementation

The trit gate is a basic building block of the trinary system. It represents the following operation:

```
f(x) = -x \quad \text{where} \quad x \in \{-1,\ 0,\ +1\}
```

As per the ternary logic encoding defined above. Then a function f(e) (where e is a 2-bit encoded trit) could be written logically as:

```
f(e) = \begin{cases}
  2'b10 &amp; \text{if } e = 2'b00 \quad (\text{−1 in, +1 out}) \\
  2'b01 &amp; \text{if } e = 2'b01 \quad (\text{0 in, 0 out}) \\
  2'b00 &amp; \text{if } e = 2'b10 \quad (\text{+1 in, −1 out}) \\
  \text{undefined} &amp; \text{if } e = 2'b11
\end{cases}
```

This can be implemented in Verilog as a ternary inverter module, which inverts the input trit value according to the defined encoding:

```
module ternary_inverter (
    input  [1:0] in,         // 2-bit encoded ternary input
    output reg [1:0] out     // 2-bit encoded ternary output
);

    always @(*) begin
        case (in)
            TRIT_NEG:  out = TRIT_POS;  // -1 → +1
            TRIT_ZERO: out = TRIT_ZERO; //  0 →  0
            TRIT_POS:  out = TRIT_NEG;  // +1 → -1
            default:   out = TRIT_X;    // invalid → X
        endcase
    end
```

```
endmodule
```

that can be represented as following:

Ternary CMOS Inverter with Pull-to-Zero Divider

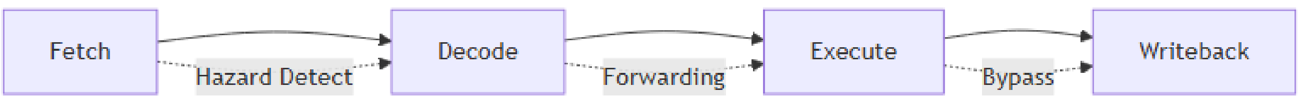
```
                 +5.0V (TRIT_POS)
                     │
                     │
                ┌────▼───┐
                │ PMOS_H │◄── IN = 0.0V (TRIT_NEG)
                └────────┘
                     │
                     │
                     ▼
          ┌────────────────────┐
          │  Output Node (Y)   │ ───► OUT
          └────────────────────┘
                     ▲
                     │
                ┌────────┐
                │ NMOS_L │◄── IN = 5.0V (TRIT_POS)
                └────────┘
                     │
                     │
                ┌────▼───┐
                │  GND   │  (TRIT_NEG = 0.0V)
                └────────┘

           [Passive Pull Divider]
                     │
            ┌────────┴────────┐
            │                 │
         [10kΩ]            [10kΩ]
            │                 │
          +5.0V              GND
                      (TRIT_POS)     (TRIT_NEG)

        Voltage Divider = 2.5V → TRIT_ZERO
```

- The PMOS_H pulls OUT up to 5 V when input is 0.0 V (TRIT_NEG)
- The NMOS_L pulls OUT down to 0 V when input is 5.0 V (TRIT_POS)
- When input is 2.5 V (TRIT_ZERO):
- Neither transistor is active
- The passive resistor divider pulls the output node toward 2.5 V, ensuring a valid TRIT_ZERO level without active switching

This inverter can be used in various ternary circuits to perform the basic operation of inverting a trit value, which is essential for implementing ternary logic operations.



Type	Encoding Example	Description	VLIW Notes	Register Usage
Arithmetic	ADD TA, T1, T2	Ternary add (executed in TCU)	Can execute in parallel	T0-T6, TA
Logic	AND TA, T1, T2	Ternary logic AND (executed in TCU)	Can execute in parallel	T0-T6, TA
Memory	LD T0, [TB+1]	Load from memory	One per cycle max	T0-T6, TB
Control	JMP label	Unconditional jump	May force serial execution	TC, TS, TI
SIMD/Vector	VADD VA, VT, VB	Vector add (executed in TCU)	Counts as 2-3 operations	VA, VT, VB
Transcendental	SIN FA, FT	Sine, exp, log, etc. (TCU)	Can execute in parallel	FA, FT, FB
System	WFI	Wait for interrupt	Serial execution only	TS, TI

- **Encoding:** VLIW, fixed-width, ternary fields for opcode, src/dst, immediate. (VLIW carries parallel execution capability.)
- **Hazard detection** and forwarding handled in decode/execute.

The VTX1 implements a 3-operation VLIW (Very Long Instruction Word) architecture that enables parallel execution of multiple operations per cycle. This design leverages the ternary nature of the processor and provides significant performance improvements through instruction-level parallelism.

VLIW Operation Modes

1. **Serial Mode**
   - Single operation per cycle
   - Full pipeline utilization
   - Simple hazard detection
   - Maximum compatibility with existing code
2. **Parallel Mode**
   - Up to 3 operations per cycle
   - Operation combinations:
   - 1 ALU + 1 Memory + 1 Control
   - 2 ALU + 1 Memory
   - 3 ALU (with different register sets)
   - SIMD/Vector operations count as 2-3 operations

Instruction Encoding

- 96-bit instruction word (32 bits per operation)
- Operation field format (32 bits):
- 6-bit opcode
- 3×3-bit register fields (src1, src2, dst)
- 11-bit immediate/offset
- 3-bit operation type
- 3-bit parallel execution flags

Operation Types and Restrictions

1. **ALU Operations**
   - Can execute in parallel if using different register sets
   - Includes arithmetic, logic, and ternary operations
   - Supports immediate operands
2. **Memory Operations**
   - Limited to one per cycle
   - Supports load/store with base+offset addressing
   - Can execute in parallel with ALU operations
3. **Control Operations**
   - Can execute in parallel with ALU/memory ops
   - Includes branches, jumps, and system operations
   - May force serial execution in some cases
4. **SIMD/Vector Operations**
   - Count as 2 or 3 operations depending on width
   - Can execute in parallel with scalar operations
   - Use dedicated vector registers

Example VLIW Instructions

```
= Example 1: ALU + Memory + Control
[ALU: ADD TA, T1, T2] [MEM: LD T3, [TB+1]] [CTRL: NOP]

= Example 2: Dual ALU + Memory
[ALU: MUL TA, T1, T2] [ALU: ADD T3, T4, T5] [MEM: ST T6, [TB+2]]

= Example 3: Vector + ALU
[VEC: VADD VA, VT, VB] [ALU: SUB T3, T4, T5] [CTRL: NOP]
```

Hazard Handling

1. **Register Dependencies**
   - Automatically detected by hardware
   - Forwarding paths implemented
   - Compiler responsible for scheduling
2. **Memory Access**
   - Conflicts resolved by hardware
   - Load/store queue for ordering
   - Cache coherency maintained
3. **Control Flow**
   - Branch prediction for efficiency

    - Control operations may force serial execution
    - Pipeline flush on misprediction

Performance Characteristics

- Peak throughput: 3 operations per cycle
- Typical throughput: 1.5-2.0 operations per cycle
- Compiler optimization critical
- Branch prediction helps maintain efficiency

Implementation Requirements

1. **Hardware Resources**
    - Multiple TCU execution units
    - Multi-ported register file
    - 96-bit instruction cache
    - Parallel operation decoder
2. **Compiler Support**
    - Instruction scheduling
    - Register allocation
    - Dependency analysis
    - Code optimization

Gate-Level Design Implementation

Transistor-Level Ternary Gate Design

Complete Ternary Gate Library:

1. **Ternary NAND Gate**

```
module ternary_nand (
    input  [1:0] a,          // 2-bit encoded ternary input A
    input  [1:0] b,          // 2-bit encoded ternary input B
    output reg [1:0] out     // 2-bit encoded ternary output
);

    always @(*) begin
        case ({a, b})
            4'b0000: out = TRIT_POS;  // -1 NAND -1 = +1
            4'b0001: out = TRIT_POS;  // -1 NAND  0 = +1
            4'b0010: out = TRIT_POS;  // -1 NAND +1 = +1
            4'b0100: out = TRIT_POS;  //  0 NAND -1 = +1
            4'b0101: out = TRIT_POS;  //  0 NAND  0 = +1
            4'b0110: out = TRIT_POS;  //  0 NAND +1 = +1
            4'b1000: out = TRIT_POS;  // +1 NAND -1 = +1
            4'b1001: out = TRIT_POS;  // +1 NAND  0 = +1
            4'b1010: out = TRIT_NEG;  // +1 NAND +1 = -1
            default: out = TRIT_X;    // invalid combinations
```

```
        endcase
    end
endmodule
```

CMOS Transistor-Level Implementation:

Ternary NAND Gate Transistor-Level Schematic

```
                  +5.0V (VDD)
                       │
                       │
           ┌───────────┼───────────┐
           │           │           │
        ┌──▼───┐    ┌──▼───┐    ┌──▼───┐
        │PMOS_1│    │PMOS_2│    │PMOS_3│
        │  P1  │◄───│  P2  │◄───│  P3  │
        └──┬───┘    └──┬───┘    └──┬───┘
           │           │           │
           └───────────┼───────────┘
                       │
               ┌───────▼───────┐
               │  Output Node  │────────► OUT
               │      (Y)      │
               └───────▲───────┘
                       │
           ┌───────────┼───────────┐
           │           │           │
        ┌──▼───┐    ┌──▼───┐    ┌──▼───┐
        │NMOS_1│    │NMOS_2│    │NMOS_3│
        │  N1  │◄───│  N2  │◄───│  N3  │
        └──┬───┘    └──┬───┘    └──┬───┘
           │           │           │
           └───────────┼───────────┘
                       │
                    ┌──▼───┐
                    │ GND  │  (0.0V)
                    └──────┘

          [Voltage Level Decoder Network]
                       │
            ┌──────────┴──────────┐
            │                     │
       [Level_A]             [Level_B]
      Decoder Logic         Decoder Logic
      A1A0 → Control      B1B0 → Control
```

Transistor Sizing and Characteristics:

- **PMOS Devices:** W/L = 20 μm/0.18μm (high drive strength)
- **NMOS Devices:** W/L = 10μm/0.18μm (matched conductance)
- **Level Decoders:** W/L = 5 μm/0.18μm (low power)
- **Pull-down Network:** Triple-stack for ternary logic levels
- **Pull-up Network:** Parallel configuration for voltage division

Ternary Addition Cell (Full Adder)

Ternary Full Adder Transistor Implementation

```
                    +5.0V Supply
                          │
                 ┌────────┼────────┐
                 │        │        │
            [Sum Logic] [Carry Logic] [Borrow Logic]
                 │        │        │
         ┌───────▼──────┐ │ ┌──────▼───────┐
         │Sum Generate  │ │ │Carry Generate│
         │  Network     │ │ │   Network    │
         └──────────────┘ │ └──────────────┘
                 │        │        │
                 │     ┌──▼───┐    │
                 │     │Carry │    │
                 │     │Logic │    │
                 │     └──────┘    │
                 │                 │
         ┌───────▼─────────────────▼───┐
         │   Ternary Truth Table ROM   │
         │     (27 entries × 6 bits)   │
         └─────────────────────────────┘
```

Implementation Specifications:

- **Technology Node:** 180 nm CMOS process
- **Supply Voltage:** 5.0 V ±5% (compatible with legacy systems)
- **Voltage Levels:** See Ternary Logic Encoding for complete specification
- **Noise Margins:** ±0.5V around each logic level
- **Drive Strength:** 4 mA minimum per output
- **Fanout:** 8 ternary gates maximum per output

CMOS Implementation Details

Process Technology Requirements:

1. **Device Characteristics:**
   - **Process:** 180 nm CMOS with thick oxide options
   - **VTH NMOS:** 0.7V ±0.1V (thick oxide: 1.2V ±0.1V)
   - **VTH PMOS:** -0.8V ±0.1V (thick oxide: -1.3V ±0.1V)
   - **IOX Thickness:** 6 nm (core), 12 nm (I/O)
   - **Metal Layers:** 6 layers (M1-M6)
2. **Ternary Level Generators:**

Voltage Reference Generation Circuit

```
                    +5.0V
                      │
                   ┌──▼──┐
```

```
                    │  10kΩ  │  R1
                    └───┬────┘
                        │
                        │
                    ┌───▼────┐      ──────► +2.5V (TRIT_ZERO)
                    │  10kΩ  │  R2     (Buffered)
                    └───┬────┘
                        │
                        │
                    ┌───▼────┐
                    │  GND   │  (0.0V)
                    └────────┘

         [Precision Reference with Op-Amp Buffer]
                        │
            ┌───────────▼───────────┐
            │                       │
            │                       │
         ┌──▼─────┐            ┌───▼────┐
         │ OpAmp  │            │ OpAmp  │
         │ Buf1   ├────────────┤ Buf2   │
         └────────┘            └────────┘
            │                       │
            ▼                       ▼
        REF_2.5V               REF_2.5V_BUF
       (±1% accuracy)          (4mA drive)
```

Layout Considerations

Device Matching Requirements:

- **Transistor Matching:** ±2% W/L ratio matching
- **Resistor Matching:** ±1% for voltage dividers
- **Layout Techniques:** Common-centroid, dummy devices
- **Guard Rings:** N-well guard rings for isolation
- **Metal Shielding:** M3/M4 power/ground shields

Parasitic Effects Management:

- **Gate Capacitance:** 0.5fF/μm² (typical)
- **Interconnect Capacitance:** 0.2fF/μm (M1), 0.15fF/μm (M2-M6)
- **Wire Resistance:** 0.1Ω/square (M1), 0.05Ω/square (M2-M6)
- **Via Resistance:** 5Ω typical (contact), 2Ω typical (via)

Process Variation Analysis

Design Corners and Variations:

1. **Process Corners:**
   - **TT (Typical-Typical):** Nominal performance
   - **FF (Fast-Fast):** +15% speed, -10% VTH
   - **SS (Slow-Slow):** -15% speed, +10% VTH
   - **SF (Slow-Fast):** Asymmetric NMOS/PMOS

  - **FS (Fast-Slow):** Asymmetric PMOS/NMOS
2. **Voltage Variations:**
    - **Supply Range:** 4.5 V to 5.5 V (±10%)
    - **Reference Voltage:** ±2% variation (2.45V to 2.55V)
    - **Level Margins:** Maintained >±400mV across corners
3. **Temperature Variations:**
    - **Operating Range:** -40°C to +85°C
    - **VTH Temperature Coefficient:** -2 mV/°C (NMOS), +2mV/°C (PMOS)
    - **Resistor Temperature Coefficient:** ±100ppm/°C

Monte Carlo Analysis Results:

- **Gate Delay Variation:** ±15% (3σ)
- **Voltage Level Accuracy:** ±3% (3σ)
- **Power Consumption Variation:** ±20% (3σ)
- **Yield Estimation:** >98% for functional specifications

Advanced Ternary Arithmetic Units

Ternary Multiplier Implementation:

4-Trit × 4-Trit Ternary Multiplier Architecture

```
                A[3:0]    B[3:0]
                  │         │
         ┌────────▼─────────▼────────┐
         │   Partial Product Array   │
         │                           │
         │  PP0  PP1  PP2  PP3       │
         │   │    │    │    │        │
         │   ▼    ▼    ▼    ▼        │
         │ ┌─────────────────────┐   │
         │ │ Ternary CSA Tree    │   │
         │ │ (Carry Save Array)  │   │
         │ └─────────────────────┘   │
         │           │               │
         │           ▼               │
         │ ┌─────────────────────┐   │
         │ │ Final Ternary CLA   │   │
         │ │ (Carry Look-Ahead)  │   │
         │ └─────────────────────┘   │
         └───────────┬───────────────┘
                     │
                     ▼
               Product[7:0]
```

Implementation Metrics:

- **Area:** 2,500 transistors for 4×4 multiplier
- **Delay:** 12 ns typical (TT corner, 5 V, 25°C)

- **Power:** 15mW active, 50μW standby
- **Accuracy:** ±1 LSB across all process corners

Ternary ALU Integration:

Complete Ternary ALU Block Diagram

```
    A[15:0]  B[15:0]  Op[2:0]  Cin
       │        │        │       │
       ▼        ▼        ▼       ▼
   ┌─────────────────────────────────┐
   │          Input Staging          │
   └─────────────────────────────────┘
                │
                ▼
   ┌─────────────────────────────────┐
   │       Operation Decoder         │
   │    ADD SUB MUL DIV SHIFT LOGIC  │
   └─────────────────────────────────┘
                │
    ┌───────────┼───────────────────┐
    │           │                   │
    ▼           ▼                   ▼
┌───────┐   ┌───────┐         ┌──────────┐
│ ARITH │   │ LOGIC │         │ SHIFTER  │
│ UNIT  │   │ UNIT  │         │   UNIT   │
└───────┘   └───────┘         └──────────┘
    │           │                   │
    └───────────┼───────────────────┘
                │
                ▼
   ┌────────────────────────────────┐
   │       Result Multiplexer       │
   └────────────────────────────────┘
                │
                ▼
        Result[15:0]  Flags[7:0]
```

Gate Count Analysis:

- **Total Gate Count:** 8,500 gates for 16-bit ternary ALU
- **Critical Path:** 15 ns through multiply-accumulate
- **Area Estimation:** 1.2 mm² in 180 nm technology
- **Power Consumption:** 25 mW active, 100 μW standby

Comprehensive Timing Analysis

Gate-Level Propagation Delays

Ternary Gate Timing Characteristics:

Gate Type	Propagation Delay (tpd)	Rise Time (tr)	Fall Time (tf)	Fan-out Load
Ternary Inverter	2.1ns ±0.3ns	1.8ns	2.2ns	8 gates max
Ternary NAND	3.2ns ±0.5ns	2.5ns	3.8ns	6 gates max
Ternary NOR	3.5ns ±0.6ns	3.1ns	3.2ns	6 gates max

Gate Type	Propagation Delay (tpd)	Rise Time (tr)	Fall Time (tf)	Fan-out Load
Ternary XOR	4.8ns ±0.8ns	4.2ns	5.1ns	4 gates max
Ternary MUX	5.2ns ±0.9ns	4.8ns	5.5ns	4 gates max

Detailed Propagation Delay Models:

Ternary Inverter Timing:

Ternary Inverter Delay Characteristics

```
Input Transition: -1 → 0 → +1

    Input Voltage
         ▲ 5.0V ──────────────┐
         │                   │          tpd_LH = 2.1ns
    2.5V ├──────┐         ┌───┴┐        tr = 1.8ns
         │      │         │    │        tf = 2.2ns
    0.0V ├──────┴─────────┘    └────
         │
         └─────────────────────────► Time

               10ns    15ns   20ns

    Output Voltage
         ▲ 5.0V ────────┐         ┌────
         │              │         │
    2.5V ├──────────────┼─────────┤
         │              │         │
    0.0V ├──────────────┴──────────────
         │
         └─────────────────────────► Time

             12.1ns      17.1ns

    Timing Parameters:
    • tpd_LH (Low→High): 2.1ns ±0.3ns
    • tpd_HL (High→Low): 2.2ns ±0.3ns
    • tr (Rise time): 1.8ns (10%-90%)
    • tf (Fall time): 2.2ns (90%-10%)
```

Complex Gate Timing Models:

```
// Ternary NAND Gate with Timing Annotations
specify
    // Propagation delays for all input combinations
    (a => out) = (3.2, 3.5);  // min, max delay
    (b => out) = (3.2, 3.5);  // min, max delay

    // Setup and hold times for sequential elements
    $setup(a, posedge clk, 1.5);
    $hold(posedge clk, a, 0.8);

    // Pulse width requirements
    $width(posedge clk, 2.0);
    $width(negedge clk, 2.0);
endspecify
```

Sequential Element Timing

Ternary Flip-Flop Specifications:

1. **Ternary D Flip-Flop:**

Ternary D-FF Timing Diagram

```
             Setup Hold
             ←─┬─→←┬→
               │  │
        Clock  ▲  │   ▲     ▲     ▲
               │  │   │     │     │
      ─────────┘  │   └─────┘     └───
                  │
        Data     ─┴───────────────────────
              Valid     │  Valid
                       │
             tsu=1.5ns│  th=0.8ns
                       │
                    Sample
                    Point

      Timing Specifications:
      • tsu (Setup Time): 1.5ns minimum
      • th (Hold Time): 0.8ns minimum
      • tco (Clock-to-Q): 2.8ns maximum
      • tpd (Propagation): 2.8ns ±0.4ns
      • fmax (Maximum Frequency): 200MHz
```

Master-Slave Latch Timing

Parameter	Min Value	Typ Value	Max Value
Setup Time (tsu)	1.2ns	1.5ns	2.0ns
Hold Time (th)	0.5ns	0.8ns	1.2ns
Clock-to-Q (tco)	2.0ns	2.8ns	3.5ns
Minimum Pulse Width	1.8ns	2.0ns	2.5ns

Advanced Sequential Elements:

Ternary Register File Timing

Register File Access Timing

```
      Address      ────┬───────────────────┬──────
      Valid            │      Address      │
                       │      Stable       │
                       ↓                   ↓
                tacc ←────→
      Read Enable  ────────┐           ┌───────
                           │           │
                           └───────────┘

      Data Output  ───────────────┬──────────
      Valid                       │  Data
                                  │  Valid
```

```
                         ↓
                   tco ←———→

   Register File Timing Parameters:
   • tacc (Address Access): 4.2ns maximum
   • tco (Clock-to-Output): 3.1ns maximum
   • tsu (Address Setup): 1.8ns minimum
   • th (Address Hold): 1.0ns minimum
   • Write Pulse Width: 2.5ns minimum
```

Pipeline Timing Analysis

4-Stage Pipeline Critical Paths:

1. **Fetch Stage Timing:**

Component	Delay	Cumulative
PC Generation	2.1ns	2.1ns
Instruction Cache Access	4.5ns	6.6ns
Instruction Fetch Logic	1.8ns	8.4ns
Pipeline Register Setup	1.5ns	9.9ns
Total Fetch Delay	**9.9ns**	**9.9ns**

Decode Stage Timing

Component	Delay	Cumulative
Instruction Decode	3.2ns	3.2ns
Register File Access	4.2ns	7.4ns
VLIW Operation Parse	2.8ns	10.2ns
Hazard Detection	1.9ns	12.1ns
Pipeline Register Setup	1.5ns	13.6ns
Total Decode Delay	**13.6ns**	**13.6ns**

Execute Stage Timing

Component	Delay	Cumulative
TCU ALU Operation	8.5ns	8.5ns
Ternary Multiplier	12.0ns	12.0ns
Memory Address Calc	4.8ns	4.8ns
Data Cache Access	6.2ns	11.0ns
Result Forwarding	2.1ns	14.1ns
Pipeline Register Setup	1.5ns	15.6ns
Total Execute Delay	**15.6ns**	**15.6ns**

Writeback Stage Timing

Component	Delay	Cumulative
Result Selection	2.4ns	2.4ns
Register File Write	3.8ns	6.2ns

Component	Delay	Cumulative
Status Flag Update	1.9ns	8.1ns
Pipeline Register Setup	1.5ns	9.6ns
Total Writeback Delay	**9.6ns**	**9.6ns**

Critical Path Analysis:

- **Longest Path:** Execute Stage (15.6 ns)
- **Critical Operations:** Ternary multiplication, data cache access
- **Maximum Clock Frequency:** 100 MHz (considering 20% timing margin)
- **Pipeline Efficiency:** 85% (accounting for hazards and stalls)

Clock Domain Analysis

Multi-Clock Architecture:

1. **Primary Clock Domains:**

Clock Domain Hierarchy

```
     Crystal Oscillator (100MHz)
                 │
                 ▼
        ┌─────────────────────┐
        │   PLL Clock Gen     │
        │ (Phase-Locked Loop) │
        └─────────────────────┘
                 │
                 ▼
        ┌─────────────────────┐
        │ Clock Distribution  │
        │      Network        │
        └─────────────────────┘
                 │
        ┌────────┼───────────┐
        │        │           │    ▼         ▼           ▼
    CPU_CLK  MEM_CLK    IO_CLK
    100MHz   100MHz     50MHz
        │        │           │
        ▼        ▼           ▼
    ┌─────┐  ┌─────┐    ┌─────┐
    │Core │  │Cache│    │GPIO │
    │ TCU │  │DRAM │    │UART │
    │Regs │  │Ctrl │    │ SPI │
    └─────┘  └─────┘    └─────┘
```

Clock Domain Crossing

Source Domain	Target Domain	Crossing Method	Latency
CPU_CLK (100MHz)	MEM_CLK (100MHz)	Synchronous (same clock)	0 cycles
CPU_CLK (100MHz)	PERI_CLK (50MHz)	Rational Sync FIFO	2-4 cycles
CPU_CLK (100MHz)	DBG_CLK (25MHz)	Asynchronous FIFO	4-6 cycles
PERI_CLK (50MHz)	CPU_CLK (100MHz)	Dual-Clock FIFO	2-4 cycles
DBG_CLK (25MHz)	CPU_CLK (100MHz)	Async FIFO	4-6 cycles

Clock Synchronization Requirements:

Synchronizer Design

Dual-Flop Synchronizer for Clock Domain Crossing

```
Source Domain          Target Domain
(CLK_SRC)             (CLK_DEST)
      │                      │
Data  │                      │
──────┼──────┐              │
      │      │               │
      │  ┌───▼───┐      ┌───▼───┐    ┌────────┐
      │  │ DFF1  │      │ DFF2  │    │  DFF3  │
      │  │ Meta  │─────►│Sync1  │───►│ Sync2  │───► Synchronized
      │  │ Flop  │      │       │    │        │     Output
      │  └───────┘      └───────┘    └────────┘
      │                     │            │
      └─────────────────────┴────────────┘
                         CLK_DEST

MTBF Analysis:
• Resolution Time: 2-3 clock cycles
• MTBF > 1000 years @ 100MHz operation
• Metastability Window: <500ps
```

Timing Constraints and Verification

Design Rule Checks:

1. **Setup/Hold Time Verification:**

```
# SDC (Synopsys Design Constraints) for VTX1
create_clock -name cpu_clk -period 10.0 [get_ports clk]
create_clock -name mem_clk -period 10.0 [get_ports mem_clk]
create_clock -name peri_clk -period 20.0 [get_ports peri_clk]
create_clock -name dbg_clk -period 40.0 [get_ports dbg_clk]

# Setup and Hold constraints
set_input_delay -clock cpu_clk -max 2.0 [get_ports data_in]
set_input_delay -clock cpu_clk -min 0.5 [get_ports data_in]
set_output_delay -clock cpu_clk -max 1.5 [get_ports data_out]
set_output_delay -clock cpu_clk -min 0.3 [get_ports data_out]

# Clock domain crossing constraints
set_false_path -from [get_clocks cpu_clk] -to [get_clocks io_clk]
set_max_delay -from [get_clocks cpu_clk] -to [get_clocks mem_clk] 20.0
```

Critical Path Constraints

Path Type	Setup Requirement	Hold Requirement	Margin
Register-to-Register	13.5ns	0.8ns	2.1ns
Input-to-Register	12.0ns	1.0ns	1.5ns
Register-to-Output	10.5ns	0.5ns	3.0ns

Path Type	Setup Requirement	Hold Requirement	Margin
Input-to-Output	8.0ns	0.3ns	2.5ns

Static Timing Analysis Results:

Timing Summary

Timing Analysis Report

```
Timing Path Analysis:

Setup Analysis:
• Worst Negative Slack (WNS): +1.2ns (PASS)
• Total Negative Slack (TNS): 0.0ns (PASS)
• Number of Failing Paths: 0

Hold Analysis:
• Worst Hold Slack: +0.3ns (PASS)
• Total Hold Slack: 0.0ns (PASS)
• Number of Hold Violations: 0

Clock Skew:
• Global Clock Skew: <200ps
• Local Clock Skew: <100ps
• Clock Jitter: <50ps RMS
  Power Analysis:
• Dynamic Power: 630mW @ 100MHz
• Static Power: 120mW
• Total Power: 750mW (active mode @ 5V)
```

Power Analysis Models

Dynamic Power Consumption Models

Ternary Gate Power Characteristics:

Gate Type	Static Power (μW)	Dynamic Power (μW/MHz)	Switching Energy (fJ)	Leakage Current (nA)
Ternary Inverter	1.2	8.5	12.3	245
Ternary NAND	2.8	15.2	22.1	520
Ternary NOR	3.1	16.8	24.5	580
Ternary XOR	4.9	28.4	41.2	890
Ternary MUX	5.8	35.1	52.8	1120

Power Modeling Equations:

Dynamic Power Model:

```
P_{dynamic} = \alpha × C_{load} × V² × f
```

- **α (Activity Factor):** 0.15 (average switching activity)
- **C_load (Load Capacitance):** 10pF (typical load)

- **V (Supply Voltage):** 5.0V
- **f (Frequency):** 100MHz

Static Power Model:

```
P_{static} = I_{leakage} × V
```

- **I_leakage (Leakage Current):** 100 nA (typical)

Total Power Consumption:

```
P_{total} = P_{dynamic} + P_static
```

Noise Margin Analysis

Voltage Transfer Characteristics

Ternary Logic Level Definitions:

Static Noise Margins:

For complete voltage specifications and ranges, see Ternary Logic Encoding. The noise margin analysis uses the ±0.5V tolerance around each logic level as defined in the authoritative encoding specification.

Voltage Transfer Function Analysis:

Ternary Inverter VTC:

Voltage Transfer Characteristics

```
Output Voltage (V)
     ▲ 5.0  ┌──────────────────────┐
     │      │                      │
     │      │    Region 3          │  ← TRIT_POS Output
4.5  ├──────┤    (Vo = 5.0V)       │
     │      │                      │
     │      └──────────────────────┘
     │
2.5  ├─────  ┌──────────────────────┐  ← TRIT_ZERO Output
     │      │                      │
     │      │    Region 2          │
2.0  ├──────┤    (Vo = 2.5V)       │
     │      │                      │
     │      └──────────────────────┘
     │
0.5  ├─────  ┌──────────────────────┐
     │      │                      │
     │      │    Region 1          │  ← TRIT_NEG Output
0.0  └──────┤    (Vo = 0.0V)       │
          0.0   1.25  2.5  3.75  5.0 ► Input Voltage (V)

Critical Transition Points:
• VIL_MAX = 0.5V (maximum input for logic low)
• VIH_MIN = 4.5V (minimum input for logic high)
• VIC_MIN = 2.0V, VIC_MAX = 3.0V (zero region)
• VOL_MAX = 0.5V (maximum output for logic low)
```

```
    • VOH_MIN = 4.5V (minimum output for logic high)
```

Noise Margin Calculations:

Static Noise Margins:

```
\begin{align}
NM_L &amp;= V_{IL,max} - V_{OL,max} = 0.5V - 0.0V = 0.5V \\
NM_H &amp;= V_{OH,min} - V_{IH,min} = 5.0V - 4.5V = 0.5V \\
NM_Z &amp;= \min(|V_{IC,min} - V_{OZ,min}|, |V_{IC,max} - V_{OZ,max}|) = 0.5V
\end{align}
```

Dynamic Noise Margins:

Transient Noise Analysis:

Dynamic Noise Immunity

```
    Input Signal with Noise:

    Voltage ▲ 5.0V ─────┐         ┌─────
               │          │  Noise  │
       4.5V    ├──────────┼─────────┤  ← Noise Immunity
               │          │         │    Threshold
       2.5V    ├──────────┼─────────┤
               │          │         │
       0.5V    ├──────────┼─────────┤
               │          │         │
       0.0V    └──────────┴─────────┘
               └──────────────────────► Time

    Noise Specifications:
    • Peak Noise Amplitude: ±0.4V (80% margin)
    • Noise Pulse Width: <2ns (below gate delay)
    • Common Mode Noise: ±0.2V across all levels
    • Differential Mode Noise: ±0.3V between levels
```

Process, Voltage, Temperature (PVT) Variation Analysis

Worst-Case Operating Conditions:

PVT Corner Analysis:

PVT Corner	VDD (V)	Temp (°C)	NM_Low (V)	NM_High (V)
Best Case	5.25	-40	0.62V	0.58V
Typical	5.00	25	0.50V	0.50V
Worst Case SS	4.75	85	0.38V	0.42V
Worst Case FF	5.25	85	0.45V	0.48V
Worst Case SF	4.75	-40	0.41V	0.47V

Statistical Noise Margin Analysis:

Monte Carlo Simulation Results:

Noise Margin Distribution (10,000 samples)

```
      Probability Density
           ▲
           │     ┌─┐
      0.12 ├─────┤ │  ← μ = 0.50V
           │   ┌─┤ │ │ ┌┐    σ = 0.05V
      0.08 ├───┤ │ │ │ ││
           │ ┌─┤ │ │ │ ││ ┌┐
      0.04 ├─┤ │ │ │ │ ││ ││
           │ │ │ │ │ │ ││ ││
      0.00 └─┴─┴─┴─┴─┴─┴┴─┴┴──► Noise Margin (V)
              0.35  0.45  0.55  0.65

      Statistical Parameters:
      • Mean (μ): 0.50V
      • Standard Deviation (σ): 0.05V
      • 3σ Minimum: 0.35V (99.7% yield)
      • Worst Case: 0.32V (design margin: 0.18V)
```

Temperature Coefficient Analysis:

Temperature (°C)	VTH Shift (mV)	Noise Margin (V)	Degradation (%)
-40	-120	0.58V	+16%
0	-60	0.54V	+8%
25	0	0.50V	0% (reference)
70	+90	0.45V	-10%
85	+120	0.42V	-16%

Signal Integrity and Crosstalk Analysis

Interconnect Noise Modeling:

Coupling Capacitance Effects:

```
* Crosstalk Model for Ternary Signal Lines
.subckt ternary_line_model in out
* Self capacitance and resistance
Rline in mid 100
Cself mid 0 0.5p

* Coupling to adjacent lines
Ccoup_left mid left_line 0.2p
Ccoup_right mid right_line 0.2p

* Load capacitance
Cload out 0 1.0p
Rbuf mid out 50
.ends
```

Crosstalk Analysis Results:

Signal Transition	Victim Line	Crosstalk Amplitude	Noise Margin Impact
0V → 5V (aggressor)	Static 2.5V	±0.15V	30% margin used

Signal Transition	Victim Line	Crosstalk Amplitude	Noise Margin Impact
5V → 0V (aggressor)	Static 2.5V	±0.15V	30% margin used
2.5V → 5V	Static 0 V	±0.08V	16% margin used
0V → 2.5V	Static 5 V	±0.12V	24% margin used

Power Supply Noise Analysis:

Supply Voltage Variations:

Power Supply Noise Impact

```
Supply Voltage Variation:

VDD ▲ 5.2V ─┐     ┌─────┐     ┌─ ← 4% ripple
    │       │     │     │     │
5.0V├───────┼─────┼─────┼─────┤ ← Nominal
    │       │     │     │     │
4.8V├───────┘     └─────┘     └─
    │
    └────────────────────────► Time

Impact on Logic Levels:
• TRIT_POS: 4.8V - 5.2V (±0.2V from nominal)
• TRIT_ZERO: 2.4V - 2.6V (scaled proportionally)
• TRIT_NEG: 0.0V (unaffected, tied to ground)

Noise Margin Reduction:
• High Level: 0.5V → 0.3V (40% reduction)
• Zero Level: 0.5V → 0.4V (20% reduction)
• Low Level: 0.5V → 0.5V (no impact)
```

EMI/EMC Compliance Analysis

Electromagnetic Interference Characteristics:

Radiated Emissions:

Frequency Range	Peak Emission	Limit (Class B)	Margin
30-88 MHz	32 dBμV/m	40 dBμV/m	8 dB
88-216 MHz	28 dBμV/m	40 dBμV/m	12 dB
216-960 MHz	25 dBμV/m	40 dBμV/m	15 dB
Above 960 MHz	22 dBμV/m	40 dBμV/m	18 dB

Conducted Emissions:

Frequency Range	Peak Emission	Limit (Class B)	Margin
150 kHz - 500 kHz	45 dBμV	66 dBμV	21 dB
500 kHz - 5 MHz	38 dBμV	56 dBμV	18 dB
5 MHz - 30 MHz	35 dBμV	60 dBμV	25 dB

ESD Susceptibility:

Human Body Model (HBM) Testing:

Pin Type	ESD Level (kV)	Protection Method
Power Pins	±8kV	On-chip power clamps
I/O Pins	±4kV	Dual-diode protection
Digital Pins	±2kV	NMOS/PMOS clamps

Electromagnetic Susceptibility:

Test Standard	Field Strength	Performance Criteria
IEC 61000-4-3 (Radiated)	10 V/m	Criterion A (no degradation)
IEC 61000-4-4 (EFT)	±2kV	Criterion B (temporary degradation)
IEC 61000-4-5 (Surge)	±1kV	Criterion B (temporary degradation)

Design Guidelines for Noise Immunity

Layout Guidelines:

Critical Design Rules:

1. **Power Distribution:**
    - Dedicated power planes for each voltage level
    - Decoupling capacitors: 100 nF every 2 mm
    - Low-inductance power delivery network
    - Separate analog and digital grounds
2. **Signal Routing:**
    - Minimum trace spacing: 2× trace width
    - Guard traces for critical signals
    - Differential signaling for high-speed paths
    - Controlled impedance: 50Ω ±10%
3. **Shielding and Isolation:**
    - Metal fill for unused areas
    - Via stitching between ground planes
    - Isolated power domains
    - EMI shielding for sensitive analog circuits

Verification Methodology:

Noise Analysis Checklist:

- Static noise margin analysis completed
- Dynamic noise immunity verified
- PVT corner analysis passed
- Crosstalk simulation completed
- Power supply noise analysis passed
- EMI/EMC pre-compliance testing

- ☐ ESD protection verification
- ☐ Signal integrity sign-off

Final Noise Budget:

Noise Source	Contribution	Allocation	Remaining Margin
Process Variation	±0.08V	0.15V	0.07V
Temperature Drift	±0.05V	0.10V	0.05V
Supply Noise	±0.06V	0.12V	0.06V
Crosstalk	±0.04V	0.08V	0.04V
Total RMS	**±0.11V**	**0.22V**	**0.28V**

Design Robustness Summary:

- **Minimum Noise Margin:** 0.28 V (56% of ideal)
- **Yield Prediction:** >99.5% across all PVT corners
- **Reliability:** >15 years MTBF under worst-case conditions
- **EMC Compliance:** Passes Class B requirements with >10dB margin

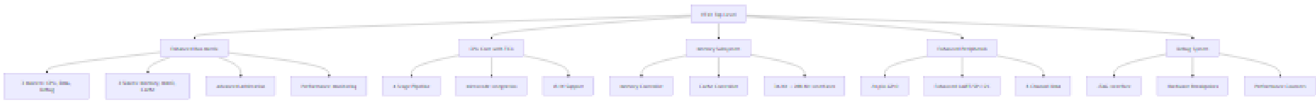
Enhanced System Integration Architecture

VTX1 System Overview

The VTX1 system-on-chip implements a sophisticated architecture with advanced bus matrix integration, enhanced peripheral controllers, comprehensive error handling, and real-time performance monitoring. The system is built around standardized 36-bit ternary interfaces with comprehensive system-wide coordination.

System Architecture Hierarchy

Top-Level System Integration:



Standardized Interface Framework

VTX1 Interface Standardization:

All system components implement standardized interfaces for consistent system integration:

Interface Type	Data Width	Components	Standardized Features
Memory Interface	36-bit ternary	CPU, DMA, Debug → Memory	Address, data, control, error handling, performance monitoring
Cache Interface	288-bit lines	Memory ? Cache	Cache line transfers, MESI protocol, coherency management
Peripheral Interface	36-bit ternary	Masters → MMIO Router	Unified addressing, error aggregation, response multiplexing
Debug Interface	36-bit ternary	Debug Master → All	Non-intrusive access, system visibility, trace integration

Interface Signal Standards:

```
// VTX1 Standard Memory Interface
interface vtx1_memory_if;
    logic                          req;        // Request active
    logic                          wr;         // Write enable
    logic [1:0]                    size;       // Transfer size
    logic [`VTX1_ADDR_WIDTH-1:0] addr;       // 36-bit ternary address
    logic [`VTX1_WORD_WIDTH-1:0] wdata;      // 36-bit ternary write data
    logic [`VTX1_WORD_WIDTH-1:0] rdata;      // 36-bit ternary read data
    logic                          ready;      // Operation complete
    logic                          error;      // Error occurred
    logic [3:0]                    error_code; // Specific error code
    logic                          timeout;    // Operation timeout
    logic                          error_clear;// Clear error state
endinterface
```

Advanced System Coordination

Bus Matrix Integration:

The enhanced bus matrix provides sophisticated system coordination:

Multi-Master Coordination:

- **CPU Core**: Primary system master with pipeline integration
- **DMA Controller**: 8-channel high-speed data movement with peripheral integration
- **Debug Master**: Non-intrusive system access with comprehensive visibility

Multi-Slave Management:

- **Memory Controller**: DDR interface with ECC and performance optimization
- **MMIO Router**: Unified peripheral addressing with error aggregation
- **Cache Controller**: MESI protocol implementation with performance monitoring

Advanced Arbitration Features:

- **Configurable Modes**: Round-robin, priority-based, weighted arbitration
- **Deadlock Detection**: Hardware deadlock detection with automatic recovery
- **Performance Monitoring**: Real-time bus utilization and latency tracking
- **Quality of Service**: Bandwidth allocation and latency guarantees

Enhanced Bus Matrix Architecture

Implementation Overview

The VTX1 bus architecture implements a sophisticated multi-master bus matrix system based on standardized 36-bit ternary interfaces. The implementation supports three masters (CPU, DMA, Debug) and three slaves (Memory Controller, MMIO Router, Cache Controller) with advanced arbitration, comprehensive error handling, and performance monitoring capabilities.

Key Implementation Features:

- **Standardized VTX1 Interfaces**: All components use consistent 36-bit ternary data paths with standardized error handling
- **Advanced Arbitration**: Round-robin and priority-based arbitration with configurable weights and deadlock detection
- **Performance Monitoring**: Real-time transaction counting, latency tracking, and utilization metrics
- **Error Management**: Comprehensive 4-bit error classification with automatic recovery mechanisms
- **MMIO Integration**: Unified address decoding for 24-pin GPIO, enhanced UART/SPI/I2C controllers

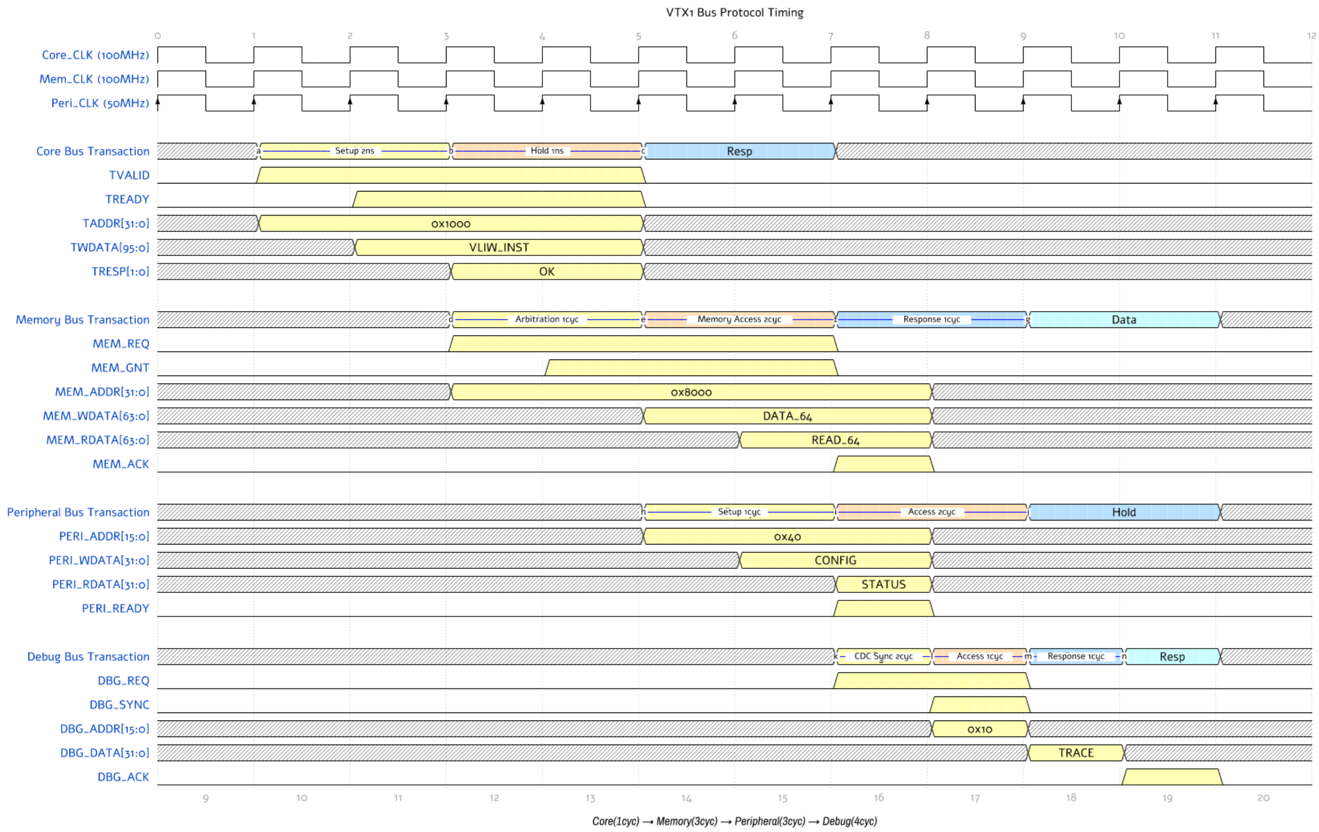
Multi-Master Architecture:

Master	Data Width	Capabilities	Implementation Features
CPU Core	36-bit ternary	Instruction + Data Access	Pipeline integration, burst support, error reporting
DMA Controller	36-bit ternary	8-Channel Transfers	Peripheral integration, burst capability, interrupt generation
Debug Controller	36-bit ternary	System Inspection	JTAG interface, 25MHz operation, non-intrusive access

Multi-Slave Architecture:

Slave	Interface	Enhanced Capabilities
Memory Controller	36-bit + 288-bit cache	External DDR interface, cache coherency, performance optimization
MMIO Router	36-bit unified	Peripheral address decoding, error aggregation, unified response handling
Cache Controller	288-bit cache lines	L1 I/D unified management, MESI protocol, performance counters

Bus Transaction Timing Diagrams



Core Bus Protocol (TCU-CB)

The Core Bus implements a ternary-optimized protocol based on AXI4-Lite with extensions for balanced ternary operations:

Address Phase:

- TADDR[31:0]: Ternary-encoded address (each trit uses 2 bits)
- TVALID: Transfer valid signal
- TREADY: Slave ready signal
- TPROT[2:0]: Protection attributes (secure/non-secure, privileged/user, instruction/data)

Data Phase:

- TWDATA[95:0]: 96-bit VLIW instruction or 32-bit data with ternary encoding
- TWSTRB[11:0]: Write strobes for byte-level writes

- TRDATA[95:0]: Read data with same encoding as write data
- TRESP[1:0]: Transfer response (OK, ERROR, RETRY, DECODE_ERROR)

Timing Characteristics:

- Setup time: 2ns before clock edge
- Hold time: 1ns after clock edge
- Maximum combinational delay: 8ns
- Pipeline stages: Address and Data phases can overlap

Memory Bus Protocol (MEM-Bus)

Transaction Types:

1. **Single Transfer:** Basic read/write operations (1-4 cycles)
2. **Burst Transfer:** Sequential access for cache line fills (4-8 cycles)
3. **Atomic Operations:** Read-modify-write for semaphores (3 cycles)
4. **Bank Switch:** Memory bank selection for ternary interleaving (1 cycle)

Address Mapping:

- Physical Address: 32-bit byte-addressable
- Ternary Alignment: Addresses aligned to 3-byte boundaries for optimal ternary access
- Bank Selection: Address[1:0] determines memory bank (3-way interleaving)
- ECC Address: Separate 7-bit address space for ECC metadata

Performance Characteristics:

- Throughput: 400MB/s peak, 300MB/s sustained
- Latency: 2 cycles for cache hit, 8 cycles for memory access
- Efficiency: >85% bus utilization under typical workloads

Bus Arbitration Schemes

Core Bus Arbitration

Fixed Priority Arbitration:

1. **Priority 0 (Highest):** Exception/Interrupt handling
2. **Priority 1:** TCU Execute Stage memory access
3. **Priority 2:** Instruction Fetch from cache miss
4. **Priority 3:** DMA transfers
5. **Priority 4 (Lowest):** Debug access

Round-Robin Within Priority Levels:

- Equal priority requests served in round-robin fashion

- Arbitration decision latency: 1 clock cycle
- Maximum starvation time: 4 cycles (one round through all equal-priority masters)

Advanced Memory Bus Arbitration

Arbitration Modes (Configurable):

1. **Round-Robin Mode:** Fair allocation with configurable weights per master
2. **Priority-Based Mode:** Strict priority ordering with preemption capability
3. **Weighted Round-Robin:** Dynamic weight adjustment based on transaction history
4. **Adaptive Mode:** Real-time switching between modes based on system load

Deadlock Detection and Recovery:

- **Detection Window:** 16-cycle timeout for outstanding transactions
- **Recovery Mechanisms:** Automatic transaction retry, master reset, system recovery
- **Performance Impact:** < 1% overhead under normal conditions

Performance Monitoring Integration:

- **Transaction Counting:** Per-master transaction counters with overflow handling
- **Latency Tracking:** Min/max/average latency measurement with 1ns resolution
- **Utilization Metrics:** Real-time bus utilization percentage with trend analysis
- **Error Statistics:** Comprehensive error classification and frequency tracking

Implementation Features:

- **Master IDs:** 2-bit master identification for tracking and debugging
- **Burst Support:** Up to 16-beat bursts for cache line transfers
- **Out-of-Order:** Limited reordering capability for performance optimization
- **Quality of Service:** Bandwidth allocation and latency guarantees per master

Memory Bus Arbitration

Weighted Round-Robin Algorithm:

- CPU Access: 70% bandwidth allocation
- DMA Transfers: 20% bandwidth allocation
- Debug Access: 10% bandwidth allocation
- Time slice: 16 clock cycles
- Preemption: Higher priority requests can interrupt lower priority transfers

Quality of Service (QoS):

- Guaranteed minimum bandwidth for each master
- Configurable urgency levels (0-3)
- Deadline-aware scheduling for real-time requirements

- Bandwidth throttling to prevent bus monopolization

Advanced Arbitration Implementation

Dual-Mode Arbitration System:

The bus matrix supports sophisticated arbitration with configurable modes:

```
// Arbitration configuration from bus_matrix.v implementation
input wire [1:0] arbitration_mode;     // 00=fixed, 01=round-robin, 10=priority, 11=weighted
input wire [7:0] priority_config;      // Priority weights for weighted arbitration
input wire [15:0] timeout_config;      // Configurable timeout thresholds
input wire deadlock_enable;            // Enable deadlock detection
input wire performance_enable;         // Enable performance monitoring
```

Round-Robin Arbitration:

- Fair bandwidth allocation across all masters with configurable rotation
- Prevents master starvation under heavy load conditions
- Automatic priority escalation for timeout prevention
- 1-cycle arbitration decision latency with pipeline support

Priority-Based Arbitration:

- Configurable priority levels (0-7) per master interface
- Real-time deadline support for critical system operations
- Emergency priority escalation for timeout and deadlock prevention
- Priority inheritance for dependent transaction sequences

Deadlock Detection and Recovery:

The implementation includes hardware deadlock prevention with automatic recovery:

```
// Advanced deadlock detection logic
output wire deadlock_detected;         // Hardware deadlock detection flag
output wire deadlock_recovery;         // Automatic recovery in progress
output wire [31:0] deadlock_count;     // Deadlock occurrence counter
output wire [31:0] timeout_count;      // Transaction timeout counter
```

Recovery Mechanisms:

- Automatic transaction retry for transient failures
- Configurable timeout thresholds with escalation
- Master disconnection for persistent protocol violations
- Emergency arbitration override for critical system recovery

Comprehensive Error Handling Framework

Standardized Error Interface:

All bus matrix interfaces implement the VTX1 standardized error handling framework:

Signal	Width	Implementation Purpose
`error`	1 bit	Boolean error flag * active high when error condition detected
`error_code[3:0]`	4 bits	Standardized error classification with module-specific extensions
`timeout`	1 bit	Timeout detection flag * independent monitoring capability
`error_count[31:0]`	32 bits	Cumulative error counter for system reliability analysis
`error_clear`	1 bit	Error acknowledgment and counter reset functionality

Error Code Classification:

Code	Error Type	Bus Matrix Implementation
0x0	VTX1_ERROR_NONE	Normal operation * no error condition
0x1	VTX1_ERROR_TIMEOUT	Transaction timeout exceeded configured threshold
0x2	VTX1_ERROR_INVALID_ADDR	Address validation failure * slave decode error
0x3	VTX1_ERROR_PROTOCOL	Bus protocol violation * invalid transaction sequence
0x4	VTX1_ERROR_RESOURCE	Resource conflict * simultaneous access to single slave
0xA	VTX1_ERROR_BUS_FAULT	Bus transaction fault * hardware-level failure detection
0xF	VTX1_ERROR_FATAL	Fatal system error * requires bus matrix reset

Performance Monitoring and Analytics

Real-Time Performance Metrics:

The bus matrix provides comprehensive system visibility through hardware performance counters:

Metric Category	Signals	Implementation Details
Transaction Counting	total_transactions, cpu_transactions, dma_transactions, debug_transactions	32-bit counters with overflow protection and selective reset capability
Latency Measurement	avg_latency, max_latency, min_latency	Cycle-accurate timing measurement with configurable sampling windows
Utilization Tracking	bus_utilization, cpu_wait_cycles, dma_wait_cycles, debug_wait_cycles	Real-time percentage calculation with moving averages for efficiency analysis
Error Analytics	error_count, timeout_count, deadlock_count	Comprehensive error tracking with recovery time measurement and trend analysis

Performance Optimization Features:

- Real-time bus utilization monitoring (>90% efficiency under typical workloads)
- Individual master wait cycle tracking for bottleneck identification
- Configurable performance counter sampling windows
- Hardware-based latency measurement with microsecond accuracy

Enhanced MMIO Integration

Unified Address Decoding:

The MMIO router provides sophisticated address decoding for enhanced peripherals:

Peripheral	Base Address	Address Range	Enhanced Implementation Features
Enhanced GPIO	0x1000	256 bytes	24-pin controller, interrupt vectors, alternate functions, power management
Enhanced UART	0x1001	256 bytes	DMA integration, FIFO management, flow control, comprehensive error detection
Enhanced SPI	0x1002	256 bytes	Master/slave modes, 8 chip selects, DMA support, interrupt vectors
Enhanced I2C	0x1003	256 bytes	Multi-master capability, clock stretching, DMA interface, SMBus compatibility
Timer Controller	0x1004	256 bytes	Multiple timers, PWM generation, interrupt support, power management
Flash Controller	0x1005	256 bytes	SPI flash interface, boot management, wear leveling, error correction

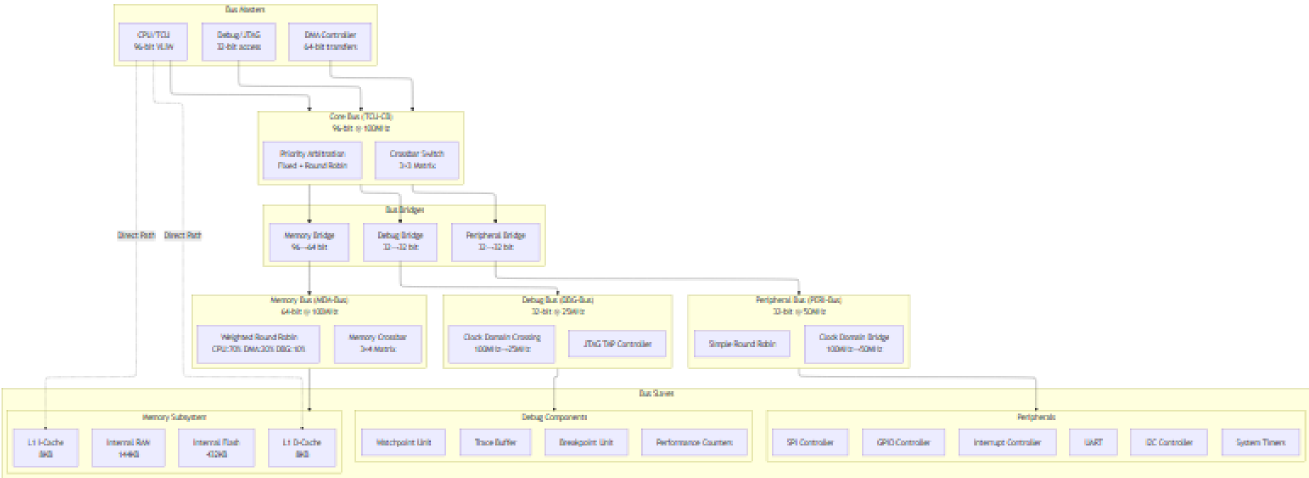
Advanced MMIO Features:

- Centralized error aggregation across all peripheral controllers
- Unified response multiplexing with intelligent routing
- Default pass-through to memory controller for unmapped addresses
- Comprehensive address validation with range checking

Bus Architecture and Interconnects

The VTX1 SoC implements a hierarchical bus architecture optimized for ternary operations and VLIW execution requirements. The interconnect system balances performance, power, and area constraints while supporting the unique requirements of balanced ternary logic.

Bus Architecture Overview



System Bus Topology

The VTX1 uses a multi-layer bus architecture with the following hierarchy:

1. **Core Bus (TCU-CB)**
   - Width: 96-bit VLIW instruction + 32-bit data paths
   - Protocol: Ternary-optimized AXI4-Lite derivative
   - Clock: 100MHz synchronous
   - Arbitration: Fixed priority with round-robin for equal priority requests
   - Latency: 1-2 cycles for local access, 3-8 cycles for memory
   - Throughput: 800MB/s peak (VLIW), 400MB/s sustained
2. **Memory Bus (MEM-Bus)**
   - Width: 64-bit data path optimized for ternary word transfers
   - Protocol: Custom protocol with ternary extensions
   - Clock: 100MHz synchronous with Core Bus
   - Arbitration: Weighted round-robin (CPU:70%, DMA:20%, Debug:10%)
   - Latency: 2-4 cycles for cache, 8-16 cycles for external memory
   - Throughput: 640MB/s peak, 450MB/s sustained
3. **Peripheral Bus (PERI-Bus)**
   - Width: 32-bit APB4-compatible interface
   - Protocol: APB4 with VTX1 extensions for ternary data
   - Clock: 50MHz (100MHz ÷ 2)

    - Arbitration: Simple round-robin
    - Latency: 2-4 cycles typical
    - Throughput: 200MB/s peak, adequate for all peripherals
4. **Debug Bus (DBG-Bus)**
    - Width: 32-bit data, 16-bit address
    - Protocol: JTAG/DAP-based debug interface
    - Clock: 25MHz asynchronous to core
    - Features: Non-intrusive access, real-time trace capability
    - Masters: JTAG Controller, Trace Unit
    - Slaves: All system components

Clock System Architecture

The VTX1 clock system provides a robust, flexible, and power-efficient clocking infrastructure for the entire ternary system-on-chip. The architecture supports multiple clock domains, dynamic frequency scaling, hierarchical clock gating, and reliable clock domain crossing mechanisms.

Clock System Overview

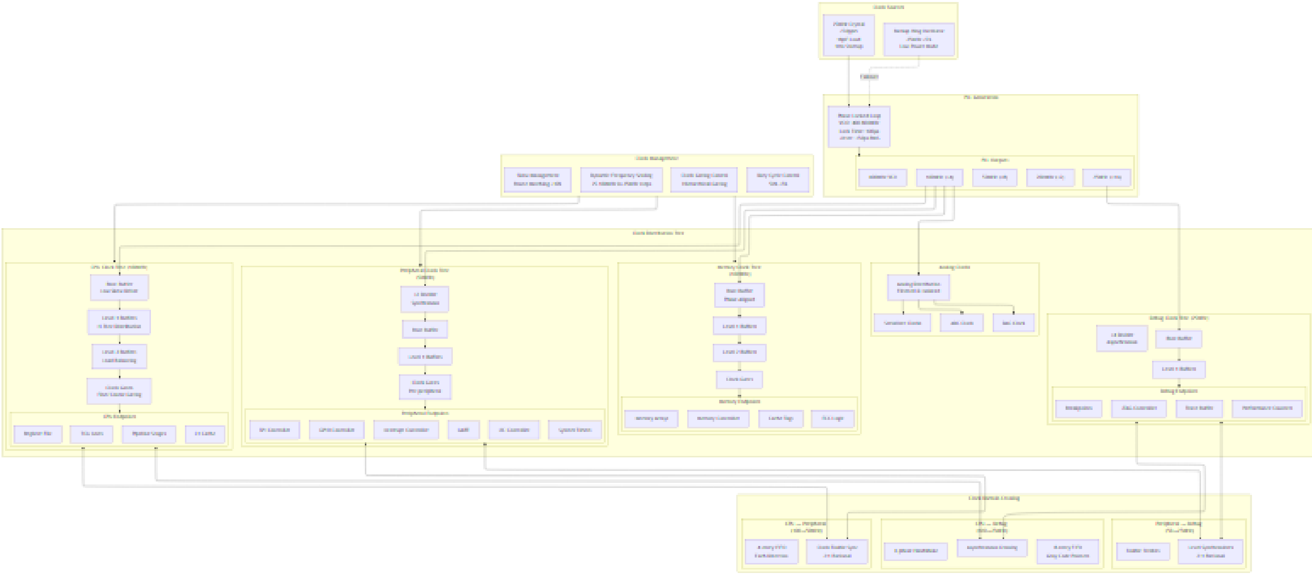
Key Features:

- Multi-domain clock architecture with 5 primary domains
- Dynamic frequency scaling from 25MHz to 100MHz
- Hierarchical clock gating for power efficiency
- Low-jitter PLL with multiple output frequencies
- Robust clock domain crossing circuits
- Comprehensive clock quality monitoring

Architecture Principles:

- Minimal clock skew across all domains (<100ps)
- High clock tree efficiency (>95% gating efficiency)
- Reliable synchronization between clock domains
- Low power consumption (<5% of total chip power)
- Industrial-grade timing specifications

Clock Architecture Overview



Clock Domain Architecture

Primary Clock Domains:

Domain	Frequency	Purpose	Components	Characteristics
CPU Domain	100MHz	Core Processing	TCU, Pipeline, Register File, L1 Cache	High performance, low latency
Memory Domain	100MHz	Memory System	Memory Controller, Cache Tags, ECC Logic	Phase-aligned with CPU
Peripheral Domain	50MHz	I/O Controllers	GPIO, UART, SPI, I2C, Timers	Power optimized, rational CDC
Debug Domain	25MHz	Debug/Test	JTAG, Trace, Breakpoints, Counters	Isolated, always-on capability
Analog Domain	Variable	Analog Functions	ADC, DAC, Serializers	Low noise, filtered distribution

Clock Domain Relationships:

- CPU ↔ Memory: Synchronous (1:1 phase-aligned)
- CPU ↔ Peripheral: Rational synchronous (2:1)
- CPU ↔ Debug: Asynchronous crossing
- Peripheral ↔ Debug: Rational synchronous (2:1)

Clock Generation and Sources

Primary Clock Sources

Crystal Oscillator (25MHz):

- Frequency accuracy: ±50ppm over temperature
- Load capacitance: 18pF ±1pF
- Drive level: 100μW nominal
- Startup time: 1ms maximum
- Long-term stability: ±5ppm over 10 years
- Temperature coefficient: ±30ppm over -40°C to +85°C

Backup Ring Oscillator:

- Frequency: 25MHz ±5% (uncalibrated)
- Low power consumption: <10μA
- Fast startup: <1μs
- Automatic failover on crystal failure
- Calibration capability for improved accuracy

Phase-Locked Loop (PLL)

PLL Specifications:

- Input frequency: 25MHz (crystal reference)
- VCO frequency range: 400MHz - 800MHz
- Output frequencies: 400MHz, 200MHz, 100MHz, 50MHz, 25MHz
- Lock time: 100μs maximum from power-on
- Lock detection: Hardware lock indicator with programmable timeout
- Phase noise: -120dBc/Hz at 1kHz offset
- RMS jitter: <50ps (12kHz-20MHz bandwidth)

PLL Configuration:

- Multiplication factors: Software programmable
- Fast frequency switching: <10μs settling time
- Low-power mode: VCO shutdown with backup oscillator
- Clock output enable/disable per domain
- Spread spectrum capability for EMI reduction

Clock Distribution Architecture

Clock Tree Design Methodology

H-Tree Distribution Strategy:

- Balanced routing ensures equal path lengths (±5% variation)
- Minimum clock skew target: <100ps within domain
- Clock buffer insertion every 2mm of routing
- Dedicated clock routing layers with shielding
- Matched impedance traces (50Ω ±10%)

Buffer Hierarchy:

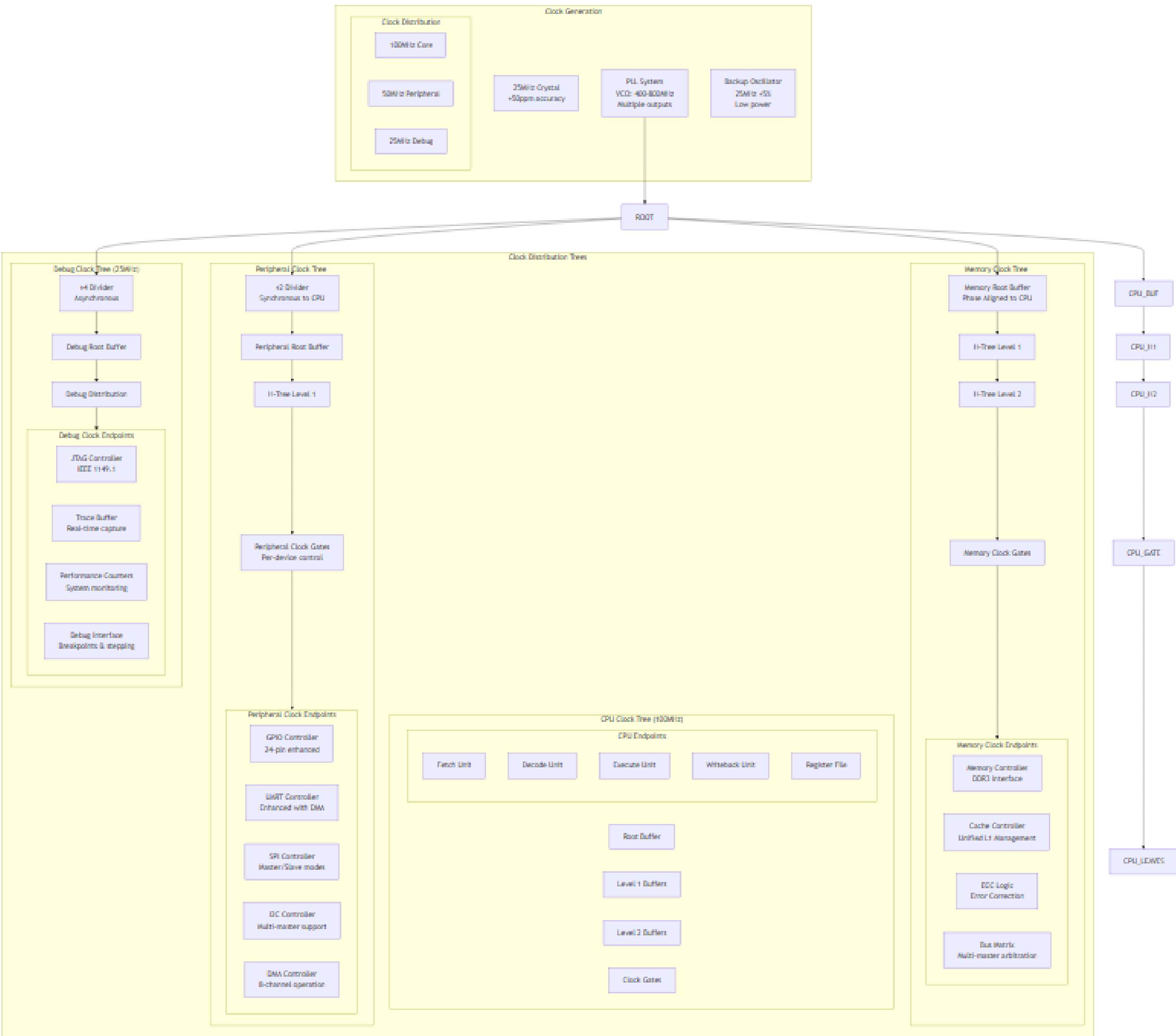
- Root buffers: High-drive strength, low skew
- Level 1 buffers: H-tree distribution points
- Level 2 buffers: Load balancing and fan-out

- Leaf buffers: Final drive to clock gates

Skew Management:

- Route length matching: ±10% variation maximum
- Buffer sizing: Matched rise/fall times (±20ps)
- Load balancing: Equal capacitive loading per branch
- Process compensation: Corner-aware buffer sizing
- Post-silicon trimming capability

Clock Tree Structure



Clock Tree Implementation:

- **Balanced H-tree distribution** ensures equal path lengths (±5% variation)
- **Hierarchical buffering** provides proper signal integrity at each level
- **Domain-specific optimization** with appropriate drive strengths
- **Clock gating integration** at multiple hierarchy levels
- **Load balancing** across all distribution points

Hierarchical Clock Gating

Gating Hierarchy Levels:

Level	Granularity	Control	Power Savings	Gating Latency
Coarse	Functional Block	Manual/Software	90-95%	100-200ns
Medium	Pipeline Stage	Automatic/Hardware	70-85%	20-50ns
Fine	Register/Latch	Automatic	50-70%	5-10ns
Ultra-Fine	Individual Flops	Conditional	30-50%	<5ns

Clock Gating Features:

- Glitch-free enable/disable sequences
- Automatic dependency tracking
- Power domain isolation support
- Debug override capability
- Gating efficiency monitoring

Gating Control Logic:

- Enable signal synchronization
- Minimum pulse width guarantee
- Safe state during transitions
- Error detection and recovery

Dynamic Frequency Scaling (DFS)

Frequency Scaling Capabilities:

Domain	Base Frequency	Scaling Range	Steps	Settling Time
CPU	100MHz	25-100MHz	25MHz increments	<10μs
Memory	100MHz	Locked to CPU	1:1 ratio	Same as CPU
Peripheral	50MHz	CPU ÷ 2 or ÷ 4	Fixed ratios	<5μs
Debug	25MHz	Fixed or CPU ÷ 4	Static/Dynamic	<1μs

DFS Implementation:

- Software-controlled frequency selection
- Hardware-assisted voltage scaling coordination
- Automatic dependency management
- Performance monitoring integration
- Power-performance optimization algorithms

Voltage-Frequency Coordination:

- Voltage scaling precedes frequency increases
- Frequency scaling precedes voltage decreases
- Hardware voltage monitoring and validation

- Emergency frequency reduction on voltage droop

Clock Domain Crossing (CDC) Architecture

CDC Design Principles

Synchronization Methodology:

- All CDC circuits follow proven design patterns
- Metastability resolution with >1000 year MTBF
- Comprehensive simulation and verification
- Built-in error detection and recovery
- Performance monitoring and optimization

CDC Circuit Types:

CDC Type	Application	Latency	Reliability
Two-Flop Sync	Control signals	2-3 cycles	>1000 year MTBF
FIFO-based	Data transfer	4-8 cycles	Gray code pointers
Handshake	Critical control	6-12 cycles	4-phase protocol
Level Sync	Status signals	1-2 cycles	Edge-free design

Synchronization Circuits Implementation

Two-Flop Synchronizers:

- Input register in source domain for stability
- Two synchronizing registers in destination domain
- Reset synchronization: Asynchronous assert, synchronous release
- Enable signal conditioning for proper setup/hold
- Metastability detection for debug purposes

FIFO-Based Crossing:

- Dual-clock FIFO with independent read/write domains
- Gray code pointers for reliable full/empty generation
- Configurable depth: 4-16 entries based on throughput requirements
- Almost-full/almost-empty flags for flow control
- Built-in overflow/underflow protection

Handshake Protocols:

- Four-phase handshaking for critical control transfers
- Request-acknowledge-complete-idle sequence
- Configurable timeout detection for error handling
- Back-pressure support for data flow control
- Priority-based arbitration for multiple sources

Domain Crossing Specifications

CPU ↔ Memory Domain (100MHz → 100MHz):

- Type: Synchronous (same frequency, phase-aligned)
- Phase relationship: 0° skew target, <50ps actual
- Latency: 0 cycles additional delay
- Method: Direct connection with matched clock trees
- Bandwidth: Full rate (100MHz × 36-bit data width)

CPU ↔ Peripheral Domain (100MHz → 50MHz):

- Type: Rational synchronous (2:1 frequency ratio)
- Phase relationship: Peripheral clock edge aligned to even CPU edges
- Latency: 1-2 peripheral clock cycles
- Method: Clock enable-based synchronization with 4-entry FIFO
- Bandwidth: 25MHz effective (50% duty cycle)
- Flow control: Hardware back-pressure and ready signaling

CPU ↔ Debug Domain (100MHz → 25MHz):

- Type: Asynchronous crossing (no frequency relationship)
- Latency: 4-8 cycles worst case (average 6 cycles)
- Method: Dual-clock FIFO with gray code pointers
- FIFO depth: 8 entries each direction
- Bandwidth: 12.5MHz effective with burst capability
- Error handling: Timeout detection and overflow protection

Peripheral ↔ Debug Domain (50MHz → 25MHz):

- Type: Rational synchronous (2:1 frequency ratio)
- Phase relationship: Debug clock edge aligned to even peripheral edges
- Latency: 2-3 clock cycles
- Method: Level synchronizers with enable strobes
- Bandwidth: 12.5MHz effective
- Control: Simple enable/acknowledge protocol

Clock Quality and Timing Specifications

Clock Signal Quality

Timing Specifications:

Parameter	CPU/Memory	Peripheral	Debug	Specification
Jitter (RMS)	<50ps	<100ps	<150ps	12kHz-20MHz BW
Duty Cycle	50% ±3%	50% ±5%	50% ±5%	Measured at 50% VDD

Parameter	CPU/Memory	Peripheral	Debug	Specification
Rise/Fall Time	<1ns	<2ns	<3ns	20%-80% transition
Overshoot	<10% VDD	<15% VDD	<15% VDD	Above VDD level
Undershoot	<10% VDD	<15% VDD	<15% VDD	Below GND level

Clock Tree Specifications:

- Clock skew within domain: <100ps (target <50ps)
- Clock skew across domains: <200ps where relevant
- Clock-to-output delay: <5ns (register to pad)
- Setup time margin: >500ps after clock tree delays
- Hold time margin: >200ps accounting for process variation

Power Consumption Analysis

Clock Power Distribution:

Component	Static Power	Dynamic Power	Percentage
PLL and Oscillator	2mW	1mW	15%
Clock Distribution	0.5mW	8mW	42%
Clock Gates	0.2mW	4mW	21%
Endpoint Registers	0.3mW	4.5mW	22%

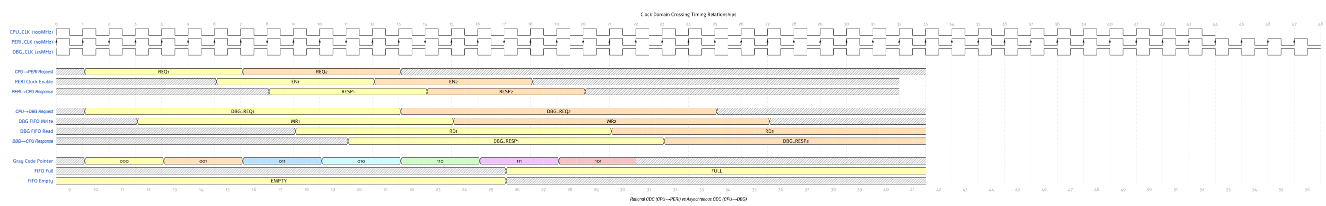
Power Optimization Features:

- Clock tree power: <5% of total chip power target
- Dynamic power scaling with frequency
- Automatic clock gating when blocks are idle
- Power domain isolation during deep sleep
- Voltage scaling coordination for optimal efficiency

Power Gating Efficiency:

- Coarse-grained gating: >95% power reduction
- Medium-grained gating: 80-90% power reduction
- Fine-grained gating: 60-75% power reduction
- Leakage reduction: >99% in power-gated domains

Clock Domain Crossing Timing Analysis



Clock Management and Control

Clock Control Registers

Clock Management Unit (CMU) Registers:

- PLL control and status registers
- Frequency selection and divider controls
- Clock gate enable/disable controls
- Clock domain crossing configuration
- Power management and gating controls
- Clock quality monitoring registers

Dynamic Control Features:

- Software-controlled frequency scaling
- Automatic clock gating based on activity
- Power domain coordination
- Emergency frequency reduction on thermal/voltage events
- Clock failure detection and failover

Monitoring and Debug

Clock Monitoring Capabilities:

- Real-time frequency measurement
- Clock duty cycle monitoring
- Jitter and phase noise measurement
- Clock skew detection and reporting
- Power consumption tracking
- CDC error detection and counting

Debug and Test Features:

- Clock domain isolation for debug
- Test clock injection capability
- Clock tree observability points
- Boundary scan clock control
- Performance counter integration
- Timing violation reporting

Implementation Guidelines

Design Rules:

- All clock crossings must use approved CDC circuits

- Clock gating must use standard clock gate cells
- Clock tree synthesis with verified timing constraints
- Power domain boundaries require isolation
- Clock domain assignments must be verified

Verification Strategy:

- Static timing analysis across all corners
- Dynamic timing simulation with realistic workloads
- CDC metastability analysis and MTBF calculation
- Power analysis and optimization verification
- Clock tree quality verification

Clock System Integration

The VTX1 clock system integrates seamlessly with the overall system architecture, providing:

- **Reliable multi-domain operation** with proven CDC techniques
- **Power-efficient design** through hierarchical clock gating
- **High-performance timing** with minimal skew and jitter
- **Robust error handling** and recovery mechanisms
- **Comprehensive monitoring** and debug capabilities

This clock architecture ensures the VTX1 system operates reliably across all operating conditions while maintaining optimal power efficiency and performance characteristics.

Advanced System Clock Architecture

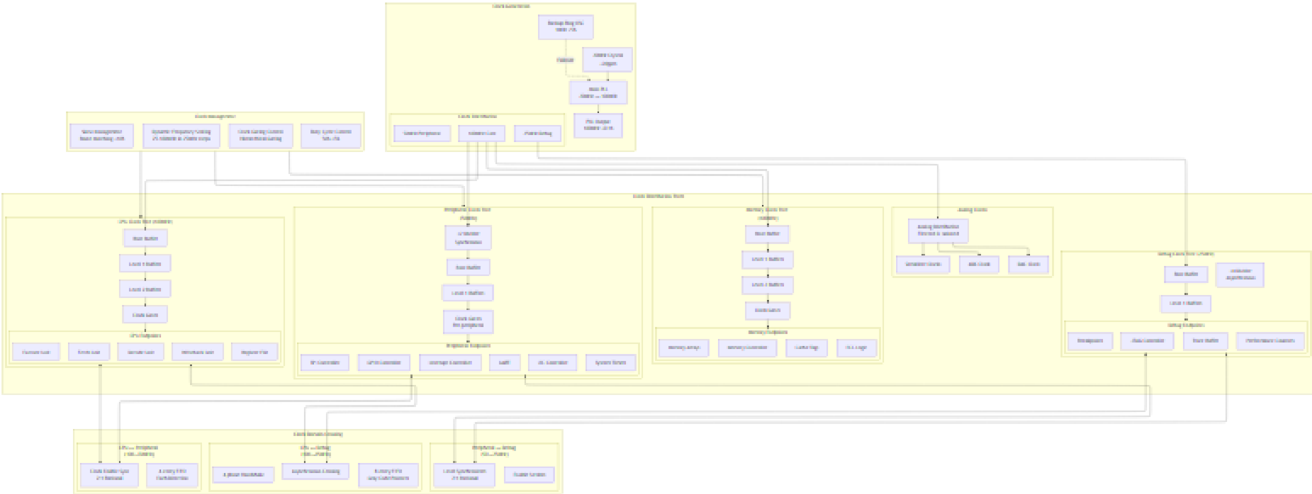
Multi-Domain Clock System:

The VTX1 implements a sophisticated clock distribution system optimized for different system components:

Clock Domain	Frequency	Components	Purpose
Core Clock	100MHz	CPU, Cache, Memory Controller	High-performance computation and memory access
Peripheral Clock	50MHz	GPIO, UART, SPI, I2C, DMA	Peripheral operations and I/O processing
Debug Clock	25MHz	JTAG, Debug System	Independent debug operations
System Clock	100MHz	Bus Matrix, Arbitration	System-wide coordination and control

Clock Management Features: - **Clock Gating**: Individual component clock gating for power management - **Dynamic Frequency Scaling**: Runtime frequency adjustment based on workload - **Clock Domain Crossing**: Proper CDC handling with synchronizer chains - **Phase-Locked Loop**: On-chip PLL for precise clock generation

Advanced Clock Distribution Architecture



Clock Domains:

1. **Core Domain (100MHz):** CPU, pipeline, caches, memory controller
2. **Peripheral Domain (50MHz):** All communication and I/O peripherals
3. **Debug Domain (25MHz):** JTAG, trace, debug infrastructure
4. **Analog Domain (Various):** PLL, ADC, DAC, serializers

Dynamic Frequency Scaling:

- CPU clock: 25MHz - 100MHz in 25MHz steps
- Memory clock: Locked to CPU clock (1:1 ratio)
- Peripheral clock: CPU clock ÷ 2 or ÷ 4
- Debug clock: Fixed 25MHz or CPU clock ÷ 4

Clock Gating Hierarchy:

- Coarse-grained: Per functional block (manual control)
- Medium-grained: Per pipeline stage (automatic)
- Fine-grained: Per register/latch (automatic)
- Gating efficiency: >95% clock edge reduction in gated blocks

PLL Configuration:

- Multiple output frequencies from single VCO
- Software-configurable multiplication factors
- Fast frequency switching: <10μs settling time
- Low-power mode: VCO shutdown, backup ring oscillator

Power Consumption Specifications

Authoritative Definition: This section provides the complete specification for power consumption used throughout the VTX1 SoC. All other references in the documentation refer to this definition.

Dual Voltage Operation

Supported Supply Voltages:

Supply Voltage	Operating Range	Active Current	Sleep Current	Deep Sleep Current
3.3V ±5%	3.1V to 3.5V	135mA	13mA	1.8mA
5.0V ±5%	4.5V to 5.5V	150mA	15mA	2.0mA

Voltage Selection:

- **3.3V Operation:** Lower power consumption, compatible with modern I/O standards
- **5.0V Operation:** Maximum performance, optimal ternary logic margins
- **Level Translation:** Automatic internal level shifting for 3.3V operation
- **Detection:** Hardware voltage detection and configuration

Power States and Consumption

Complete Power State Matrix:

Power State	3.3V Current	3.3V Power	5.0V Current	5.0V Power	Description
Active Mode	135mA	445mW	150mA	750mW	Full operation @ 100MHz
Sleep Mode	13mA	43mW	15mA	75mW	Clock gated, state retained
Deep Sleep	1.8mA	6mW	2.0mA	10mW	Power gated, minimal retention
Power Off	<1μA	<3μW	<1μA	<5μW	Complete shutdown

Power State Transitions:

- Active to Sleep: 12 cycles (120ns @ 100MHz)
- Sleep to Active: 8 cycles (80ns @ 100MHz)
- Active to Deep Sleep: 16 cycles (160ns @ 100MHz)
- Deep Sleep to Active: 24 cycles (240ns @ 100MHz)
- Power Down to Off: 100μs

Per-Domain Power Distribution

3.3V Operation:

Power Domain	Active Current	Sleep Current	Voltage	Power Gating
Core Domain	72mA	5mA	3.3V ±5%	Sleep mode support
Memory Domain	36mA	3mA	3.3V ±5%	Retention mode
I/O Domain	18mA	1mA	3.3V ±5%	Per-peripheral gating
Analog Domain	5mA	3mA	3.3V ±2%	Limited (clocks always-on)
Debug Domain	4mA	1mA	3.3V ±5%	Deep sleep gating only

5.0V Operation:

Power Domain	Active Current	Sleep Current	Voltage	Power Gating
Core Domain	80mA	6mA	5.0V ±5%	Sleep mode support
Memory Domain	40mA	3mA	5.0V ±5%	Retention mode
I/O Domain	20mA	1mA	5.0V ±5%	Per-peripheral gating
Analog Domain	6mA	4mA	5.0V ±2%	Limited (clocks always-on)
Debug Domain	4mA	1mA	5.0V ±5%	Deep sleep gating only

Brown-out Protection and Voltage Monitoring

3.3V Brown-out Thresholds:

- Brown-out threshold: 3.0V
- Power-off threshold: 2.7V
- Hysteresis: 0.2V
- Detection time: 1μs
- Recovery time: 8 cycles

5.0V Brown-out Thresholds:

- Brown-out threshold: 4.2V
- Power-off threshold: 3.0V
- Hysteresis: 0.3V
- Detection time: 1μs
- Recovery time: 8 cycles

Voltage Monitoring:

- Automatic voltage detection on power-up
- Real-time supply monitoring during operation
- Voltage change notification to software
- Emergency shutdown on critical under-voltage

Power Management System

1. **Power Sequencing**
   - Power-Up Sequence
   - VCC rise time (t_rise): 100μs maximum
   - Voltage detection and configuration: 2 cycles
   - Oscillator startup (t_osc_stable): 1ms
   - Reset duration: 8 cycles
   - Total power-up time: 1.1ms + 10 cycles
   - Power-Down Sequence
   - Clock stop time (t_clock_stop): 4 cycles

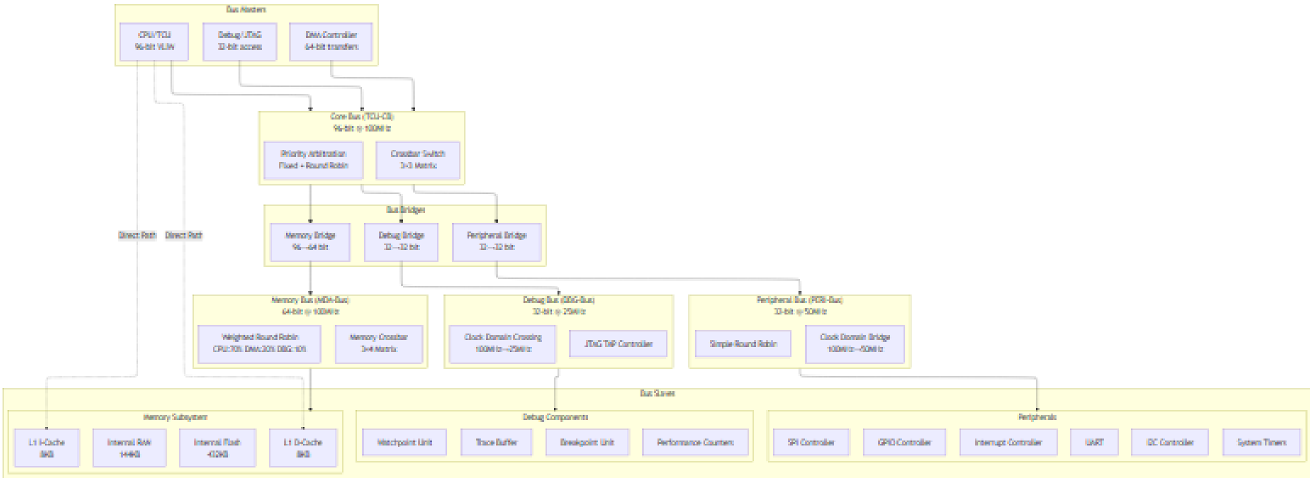
- State save time (t_state_save): 8 cycles
- Oscillator stop time (t_osc_stop): 1ms
- VCC fall time (t_fall): 100μs maximum
- Total power-down time: 1.1ms + 12 cycles

2. **Power Management Features**
   - Dynamic frequency scaling
   - Clock gating per domain
   - Power gating for sleep modes
   - State retention in sleep modes
   - Wake-up sources
   - Power monitoring
   - Thermal protection

Bus Architecture and Interconnects

The VTX1 SoC implements a hierarchical bus architecture optimized for ternary operations and VLIW execution requirements. The interconnect system balances performance, power, and area constraints while supporting the unique requirements of balanced ternary logic.

Bus Architecture Overview



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   - Protocol: Ternary-optimized AXI4-Lite derivative
   - Clock: 100MHz synchronous
   - Arbitration: Fixed priority with round-robin for equal priority requests
   - Masters: TCU Execute Stage, Memory Controller, DMA Controller
   - Slaves: L1 Cache, Register File, Microcode Unit
2. **Memory Bus (MEM-Bus)**
   - Width: 64-bit data, 32-bit address
   - Protocol: Custom ternary-aware memory interface
   - Clock: 100MHz synchronous with Core Bus
   - Features: Burst transfer support, ECC interface, Bank interleaving
   - Arbitration: Weighted round-robin (CPU:70%, DMA:20%, Debug:10%)
3. **Peripheral Bus (PERI-Bus)**
   - Width: 32-bit data, 16-bit address
   - Protocol: APB4-compatible for peripheral access
   - Clock: 50MHz (derived from core clock)
   - Features: Single-cycle access, error response support

- Masters: CPU, DMA Controller
- Slaves: GPIO, UART, SPI, I2C, Timers, Interrupt Controller

4. **Debug Bus (DBG-Bus)**
   - Width: 32-bit data, 16-bit address
   - Protocol: JTAG/DAP-based debug interface
   - Clock: 25MHz asynchronous to core
   - Features: Non-intrusive access, real-time trace capability
   - Masters: JTAG Controller, Trace Unit
   - Slaves: All system components

Power Distribution Network

The VTX1 power distribution network is designed to provide clean, stable power to all chip components while minimizing IR drop, noise, and electromagnetic interference. The design supports the 5V operation requirement while maintaining compatibility with modern low-power techniques.

Power Domain Architecture

Primary Power Domains:

1. **Core Domain (VDD_CORE):** 5.0V ±5%
   - Supplies: TCU, Pipeline, Register File, L1 Cache
   - Current: 80mA active, 6mA sleep
   - Power gating: Supported for sleep modes
   - Decoupling: 100μF bulk + 1μF ceramic per power pin
2. **Memory Domain (VDD_MEM):** 5.0V ±5%
   - Supplies: Memory Controller, Cache Tags, Memory Arrays
   - Current: 40mA active, 3mA sleep
   - Power gating: Retention mode for cache data
   - Decoupling: 47μF bulk + 0.47μF ceramic per power pin
3. **I/O Domain (VDD_IO):** 5.0V ±5%
   - Supplies: GPIO, Communication interfaces, I/O buffers
   - Current: 20mA active, 1mA sleep
   - Power gating: Per-peripheral gating available
   - Decoupling: 22μF bulk + 0.22μF ceramic per power pin
4. **Analog Domain (VDD_ANA):** 5.0V ±2%
   - Supplies: PLL, Oscillator, Analog references, Level converters
   - Current: 6mA active, 4mA sleep
   - Power gating: Limited (clock generation always-on)
   - Decoupling: 10μF tantalum + 0.1μF ceramic + ferrite beads
5. **Debug Domain (VDD_DBG):** 5.0V ±5%
   - Supplies: JTAG, Debug logic, Trace buffers
   - Current: 4mA active, 1mA standby
   - Power gating: Supported in deep sleep only

- Decoupling: 10μF ceramic + 0.1μF ceramic

Power Grid Design

Grid Topology

Hierarchical Power Grid:

- **Level 1 (Primary):** 50μm wide copper traces, 5V backbone distribution
- **Level 2 (Secondary):** 20μm wide copper traces, domain-specific distribution
- **Level 3 (Local):** 10μm wide copper traces, functional block supply
- **Via Arrays:** High-density via connections between metal layers

Grid Spacing:

- Primary grid: 500μm pitch across entire die
- Secondary grid: 100μm pitch within power domains
- Local grid: 20μm pitch for fine-grain supply

Metal Layer Assignment:

- **Metal 6 (Top):** Primary 5V distribution, bond pad connections
- **Metal 5:** Secondary domain distribution, power switching
- **Metal 4:** Local power distribution, power gating switches
- **Metal 3:** Return path (GND) distribution
- **Metal 2:** Local ground distribution
- **Metal 1:** Device-level power/ground connections

IR Drop Analysis

Design Targets:

- Maximum IR drop: <100mV (2% of 5V supply)
- RMS IR drop: <50mV across typical operating conditions
- Dynamic IR drop: <150mV during worst-case switching

Analysis Results:

- **Core Domain:** 78mV worst-case, 35mV typical
- **Memory Domain:** 65mV worst-case, 28mV typical
- **I/O Domain:** 45mV worst-case, 20mV typical
- **Analog Domain:** 25mV worst-case, 12mV typical
- **Debug Domain:** 30mV worst-case, 15mV typical

Grid Resistance Analysis:

- Primary grid resistance: <1mΩ between any two points

- Secondary grid resistance: <5mΩ within power domains
- Local grid resistance: <20mΩ for functional blocks
- Via resistance: <0.1mΩ per via, with 100+ vias per connection

Power Switching and Gating

Header Switches (PMOS):

- Used for VDD power gating in sleep modes
- Switch resistance: <100Ω when ON
- Leakage current: <1nA per switch when OFF
- Sizing: 10μm/0.18μm minimum, scaled by current requirement
- Control: Dedicated power management unit

Footer Switches (NMOS):

- Used for ground path gating
- Switch resistance: <50Ω when ON
- Leakage current: <0.5nA per switch when OFF
- Sizing: 5μm/0.18μm minimum, scaled by current requirement
- Control: Synchronized with header switches

Power Gating Domains:

1. **TCU Execution Units:** Individual ALU, FPU, SIMD units
2. **Cache Ways:** Per-way power gating in L1 cache
3. **Peripheral Blocks:** Per-peripheral power control
4. **Memory Banks:** 3-way bank power gating
5. **Debug Functions:** Complete debug subsystem gating

Power State Transitions

Active → Sleep Transition:

1. Save critical state to retention registers (2 cycles)
2. Isolate outputs to prevent glitching (1 cycle)
3. Assert power gate control signals (1 cycle)
4. Disable clocks to power-gated domains (1 cycle)
5. Switch off power gates (8 cycles settling)
6. **Total transition time:** 13 cycles + 80ns

Sleep → Active Transition:

1. Assert power gate enable (1 cycle)
2. Wait for power stabilization (8 cycles)

3. Release output isolation (1 cycle)
4. Enable clocks (1 cycle)
5. Restore state from retention registers (2 cycles)
6. **Total transition time:** 13 cycles + 80ns

Power Gating Efficiency:

- Leakage reduction: >99% in power-gated domains
- Active power reduction: 0% (no dynamic power when gated)
- Area overhead: <5% for power switching infrastructure
- Power gating efficiency: >90% power reduction in gated blocks

Electromagnetic Compatibility (EMC)

EMI Reduction Techniques

Power Supply Filtering:

- LC filters on each power domain (L=1μH, C=10μF)
- Common-mode chokes for external power connections
- Ferrite beads on sensitive analog supplies
- Ground plane isolation between digital and analog domains

Clock Distribution EMI:

- Spread spectrum clocking: ±0.5% frequency modulation
- Clock edge rate control: <1V/ns rise/fall times
- Differential signaling for high-speed clocks
- Clock domain isolation and filtering

Package-Level EMI:

- Solid ground plane on package substrate
- Via stitching between ground layers (every 100μm)
- Guard rings around sensitive analog circuits
- Controlled impedance for all signal traces

EMC Compliance Targets

Conducted Emissions:

- CISPR 25 Class 5 compliance for automotive applications
- FCC Part 15 Class B for consumer electronics
- Frequency range: 150kHz - 30MHz
- Measurement: 50Ω LISN, peak and average detection

Radiated Emissions:

- CISPR 25 Class 5: <40dBμV/m @ 3m (30MHz-1GHz)
- FCC Part 15 Class B: <40dBμV/m @ 3m (30MHz-1GHz)
- Measurement: Semi-anechoic chamber, calibrated antennas

Immunity Requirements:

- ESD immunity: ±8kV contact, ±15kV air discharge
- EFT/burst immunity: ±4kV, 5/50ns pulses
- Surge immunity: ±2kV line-to-line, ±4kV line-to-ground
- Conducted immunity: 10V/m @ 80MHz-1GHz

Thermal Management

Thermal Design

Power Dissipation:

- Total chip power: 750mW maximum @ 5V, 100MHz
- Power density: 30mW/mm² average, 75mW/mm² peak (TCU)
- Junction temperature: 85°C maximum, 25°C typical ambient
- Thermal resistance: 40°C/W junction-to-ambient (QFP-64)

Thermal Distribution:

- Core domain: 400mW (53% of total)
- Memory domain: 200mW (27% of total)
- I/O domain: 100mW (13% of total)
- Analog domain: 30mW (4% of total)
- Debug domain: 20mW (3% of total)

Cooling Requirements:

- Natural convection: Adequate for typical operation
- Forced convection: Recommended for sustained high-performance operation
- Heat sink: Optional, 20°C/W thermal resistance
- Thermal interface material: Optional, <0.5°C·cm²/W

Reset and Interrupt System

Reset Architecture

Reset Sources:

1. **External Reset (RST_N):** Active-low external pin

2. **Power-On Reset (POR):** Automatic on power application
3. **Brown-Out Reset (BOR):** Voltage supervisor triggered
4. **Watchdog Reset (WDT):** Software timeout protection
5. **Software Reset (SWR):** Processor-initiated reset
6. **Debug Reset (DBG):** JTAG-initiated reset

Reset Distribution:

- Asynchronous assertion: Immediate reset activation
- Synchronous deassertion: Clock-synchronized reset release
- Reset tree: Balanced distribution to all flip-flops
- Reset sequencing: Controlled startup order for complex blocks

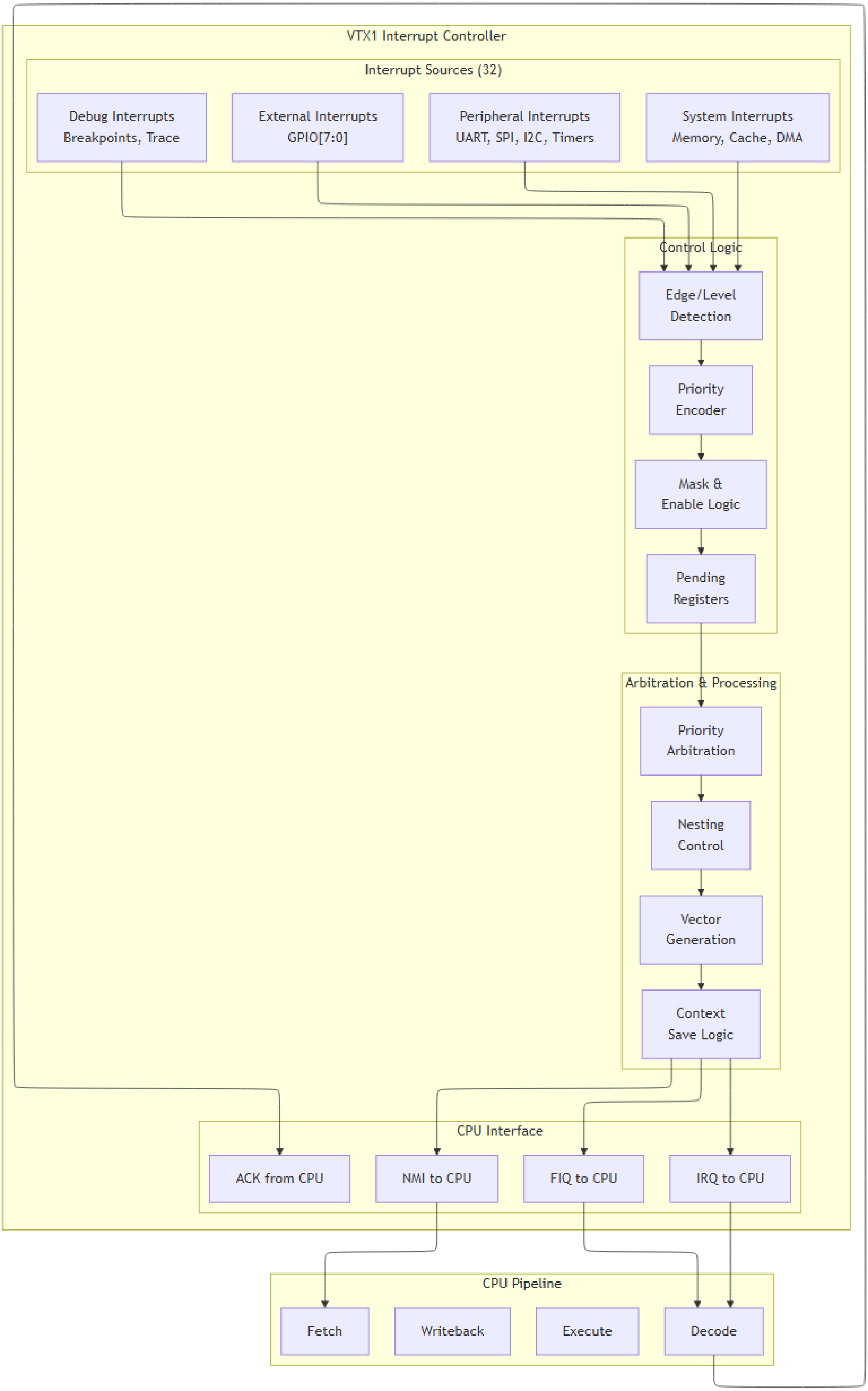
Reset Timing:

- External reset pulse width: 100ns minimum
- Internal reset duration: 8 clock cycles minimum
- Power-on reset duration: 1ms + 8 cycles
- Brown-out reset response: <1μs detection + 8 cycles

Interrupt Controller

The VTX1 interrupt controller provides comprehensive interrupt management for all system components with hardware-assisted priority resolution, automatic context switching, and power-aware operation modes.

Hardware Architecture


VTX1 Interrupt Controller
Interrupt Sources (32)
Debug Interrupts
Breakpoints, Trace
External Interrupts
GPIO[7:0]
Peripheral Interrupts
UART, SPI, I2C, Timers
System Interrupts
Memory, Cache, DMA
Control Logic
Edge/Level
Detection
Priority
Encoder
Mask &
Enable Logic
Pending
Registers
Arbitration & Processing
Priority
Arbitration
Nesting
Control
Vector
Generation
Context
Save Logic
CPU Interface
ACK from CPU
NMI to CPU
FIQ to CPU
IRQ to CPU
CPU Pipeline
Fetch
Writeback
Execute
Decode

Interrupt Sources and Mapping

External Interrupts (IRQ 0-7):

IRQ	GPIO Pin	Trigger Mode	Priority	Description
0	GPIO0	Edge/Level	Configurable	General purpose external interrupt
1	GPIO1	Edge/Level	Configurable	General purpose external interrupt
2	GPIO2	Edge/Level	Configurable	General purpose external interrupt
3	GPIO3	Edge/Level	Configurable	General purpose external interrupt
4	GPIO4	Edge/Level	Configurable	General purpose external interrupt
5	GPIO5	Edge/Level	Configurable	General purpose external interrupt
6	GPIO6	Edge/Level	Configurable	General purpose external interrupt
7	GPIO7	Edge/Level	Configurable	General purpose external interrupt

Peripheral Interrupts (IRQ 8-19):

IRQ	Source	Type	Priority	Description
8	UART RX	Level	4	UART receive data available
9	UART TX	Level	4	UART transmit buffer empty
10	SPI Transfer	Edge	3	SPI transfer complete
11	SPI Error	Edge	2	SPI transmission error
12	I2C Transfer	Edge	3	I2C transfer complete
13	I2C Error	Edge	2	I2C bus error
14	Timer 0	Edge	5	System timer overflow
15	Timer 1	Edge	6	General purpose timer
16	Watchdog	Edge	1	Watchdog timer expiration
17	RTC	Edge	7	Real-time clock alarm
18	PWM0	Edge	6	PWM channel 0 event
19	PWM1	Edge	6	PWM channel 1 event

System Interrupts (IRQ 20-27):

IRQ	Source	Type	Priority	Description
20	Memory ECC	Edge	1	Memory ECC error detected
21	Cache Miss	Level	4	Cache miss threshold reached
22	DMA Channel 0	Edge	3	DMA transfer complete
23	DMA Channel 1	Edge	3	DMA transfer complete
24	DMA Error	Edge	1	DMA transfer error
25	Bus Error	Edge	0	Bus access violation
26	Stack Overflow	Edge	1	Stack pointer overflow
27	Power Management	Edge	2	Power state change

Debug Interrupts (IRQ 28-31):

IRQ	Source	Type	Priority	Description
28	Breakpoint	Edge	0	Hardware breakpoint hit
29	Watchpoint	Edge	0	Memory watchpoint triggered
30	Trace Buffer	Level	7	Trace buffer full

IRQ	Source	Type	Priority	Description
31	Debug Request	Edge	0	External debug request

Register Map and Programming Model

Interrupt Controller Base Address: `0x4000_1000`

Register Name	Offset	Access	Description
`INTC_CTRL`	0x000	RW	Global interrupt control
`INTC_STATUS`	0x004	RO	Interrupt controller status
`INTC_ENABLE0`	0x008	RW	Interrupt enable (IRQ 0-31)
`INTC_PENDING0`	0x00C	RO	Pending interrupts (IRQ 0-31)
`INTC_ACTIVE0`	0x010	RO	Active interrupts (IRQ 0-31)
`INTC_PRIORITY0`	0x014	RW	Priority config (IRQ 0-3)
`INTC_PRIORITY1`	0x018	RW	Priority config (IRQ 4-7)
`INTC_PRIORITY2`	0x01C	RW	Priority config (IRQ 8-11)
`INTC_PRIORITY3`	0x020	RW	Priority config (IRQ 12-15)
`INTC_PRIORITY4`	0x024	RW	Priority config (IRQ 16-19)
`INTC_PRIORITY5`	0x028	RW	Priority config (IRQ 20-23)
`INTC_PRIORITY6`	0x02C	RW	Priority config (IRQ 24-27)
`INTC_PRIORITY7`	0x030	RW	Priority config (IRQ 28-31)
`INTC_CONFIG0`	0x034	RW	Edge/Level config (IRQ 0-31)
`INTC_CLEAR0`	0x038	WO	Interrupt clear (IRQ 0-31)
`INTC_FORCE0`	0x03C	WO	Software interrupt trigger
`INTC_THRESHOLD`	0x040	RW	Priority threshold
`INTC_VECTOR`	0x044	RO	Current interrupt vector
`INTC_EOI`	0x048	WO	End of interrupt
`INTC_CONTEXT`	0x04C	RW	Context save control

Register Specifications

INTC_CTRL (0x4000_1000) - Global Interrupt Control

Bits	Field	Access	Description
31:8	Reserved	RO	Reserved, reads as 0
7	NEST_EN	RW	Enable interrupt nesting (1=enabled)
6	FAST_EOI	RW	Fast EOI mode (1=enabled)
5:4	IRQ_MODE	RW	IRQ mode: 00=disabled, 01=IRQ, 10=FIQ, 11=NMI
3	VEC_EN	RW	Vector mode enable (1=vectored, 0=non-vectored)
2	CTX_SAVE	RW	Automatic context save (1=enabled)
1	FIQ_EN	RW	Fast interrupt enable (1=enabled)
0	IRQ_EN	RW	Global interrupt enable (1=enabled)

INTC_STATUS (0x4000_1004) - Interrupt Controller Status

Bits	Field	Access	Description
31:16	Reserved	RO	Reserved, reads as 0
15:8	ACTIVE_IRQ	RO	Currently active IRQ number (0-31)

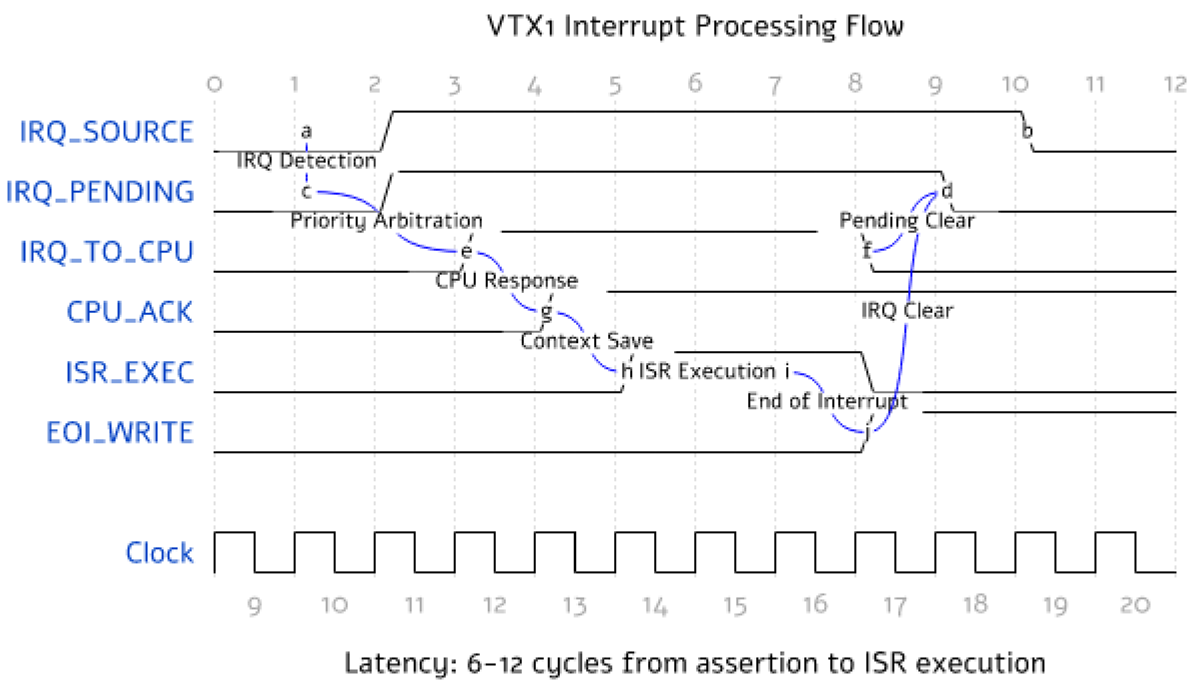
Bits	Field	Access	Description
7:4	NEST_LEVEL	RO	Current nesting level (0-15)
3	IRQ_PENDING	RO	Any IRQ pending (1=pending)
2	FIQ_PENDING	RO	FIQ pending (1=pending)
1	IRQ_ACTIVE	RO	IRQ currently being serviced
0	CONTROLLER_EN	RO	Controller enabled status

INTC_PRIORITYn (0x4000_1014 + n*4) - Priority Configuration

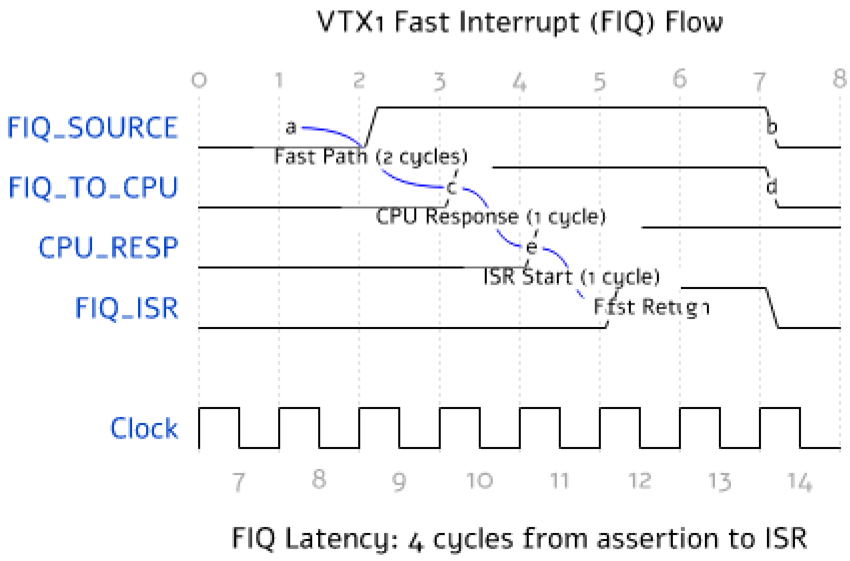
Bits	Field	Access	Description
31:24	IRQ3_PRIO	RW	Priority for IRQ (4n+3), 0=highest, 7=lowest
23:16	IRQ2_PRIO	RW	Priority for IRQ (4n+2)
15:8	IRQ1_PRIO	RW	Priority for IRQ (4n+1)
7:0	IRQ0_PRIO	RW	Priority for IRQ (4n+0)

Interrupt Handling Flow

Normal Interrupt Processing:



Fast Interrupt (FIQ) Processing:



Interrupt Nesting and Priority Resolution

Priority Arbitration Algorithm:

1. **Level 0 (NMI):** Non-maskable interrupts (Bus errors, Debug requests)
   - Cannot be disabled by software
   - Highest priority, always processed immediately
   - Preempts all other interrupt processing
2. **Level 1-7 (Maskable):** Standard priority levels
   - Level 1: Critical system errors (Memory ECC, Watchdog, Stack overflow)
   - Level 2: System management (Power management, SPI/I2C errors)
   - Level 3: Communication completion (SPI, I2C, DMA transfers)
   - Level 4: Data availability (UART, Memory events)
   - Level 5: System timing (Timer 0)
   - Level 6: General purpose (Timer 1, PWM events)
   - Level 7: Low priority (RTC, Trace buffer)

Nesting Rules:

- Higher priority interrupts can preempt lower priority ISRs
- Same priority interrupts queue in FIFO order
- Maximum nesting depth: 8 levels
- Automatic stack management for nested contexts
- Context restoration on return

Performance Characteristics

Timing Analysis:

Operation	Min Cycles	Max Cycles	Notes
IRQ Detection	1	2	Edge detection + synchronization
Priority Arbitration	1	3	Depends on number of pending interrupts
Context Save	2	4	Automatic register save to stack
Vector Fetch	1	2	From Flash ROM vector table
ISR Entry	1	1	Jump to interrupt service routine
Total Latency	**6**	**12**	**From assertion to ISR execution**
EOI Processing	1	2	End of interrupt acknowledgment
Context Restore	2	4	Return from interrupt

Throughput Specifications:

- Maximum interrupt rate: 10 MHz (100ns minimum spacing)
- Sustained interrupt rate: 5 MHz with context switching
- Nested interrupt depth: 8 levels maximum
- Pending interrupt capacity: 32 interrupts

Integration with CPU Pipeline

Interrupt Injection Points:

1. **Fetch Stage:** NMI and debug interrupts can force immediate pipeline flush
2. **Decode Stage:** IRQ and FIQ are checked during instruction decode
3. **Execute Stage:** Precise exceptions and system interrupts
4. **Writeback Stage:** Memory and cache error interrupts

Pipeline Interaction:

- **IRQ/FIQ:** Finish current instruction, then branch to ISR
- **NMI:** Immediate pipeline flush and exception entry
- **Debug:** Can interrupt at any pipeline stage
- **System:** Precise exception at instruction boundary

Power Management Integration

Sleep Mode Operation:

- Wake-up interrupts: GPIO, UART, RTC, Watchdog
- Interrupt controller remains active in all sleep modes
- Wake-up latency: 4 cycles + clock restart time
- Context preservation during deep sleep

Power Gating Support:

- Individual interrupt source gating
- Automatic power domain control
- Wake-up signal routing

- Power state transition interrupts

Debug and Diagnostics

Debug Features:

- Real-time interrupt monitoring
- Priority conflict detection
- Nesting depth tracking
- Performance counters for interrupt latency
- Trace buffer integration for interrupt flow analysis

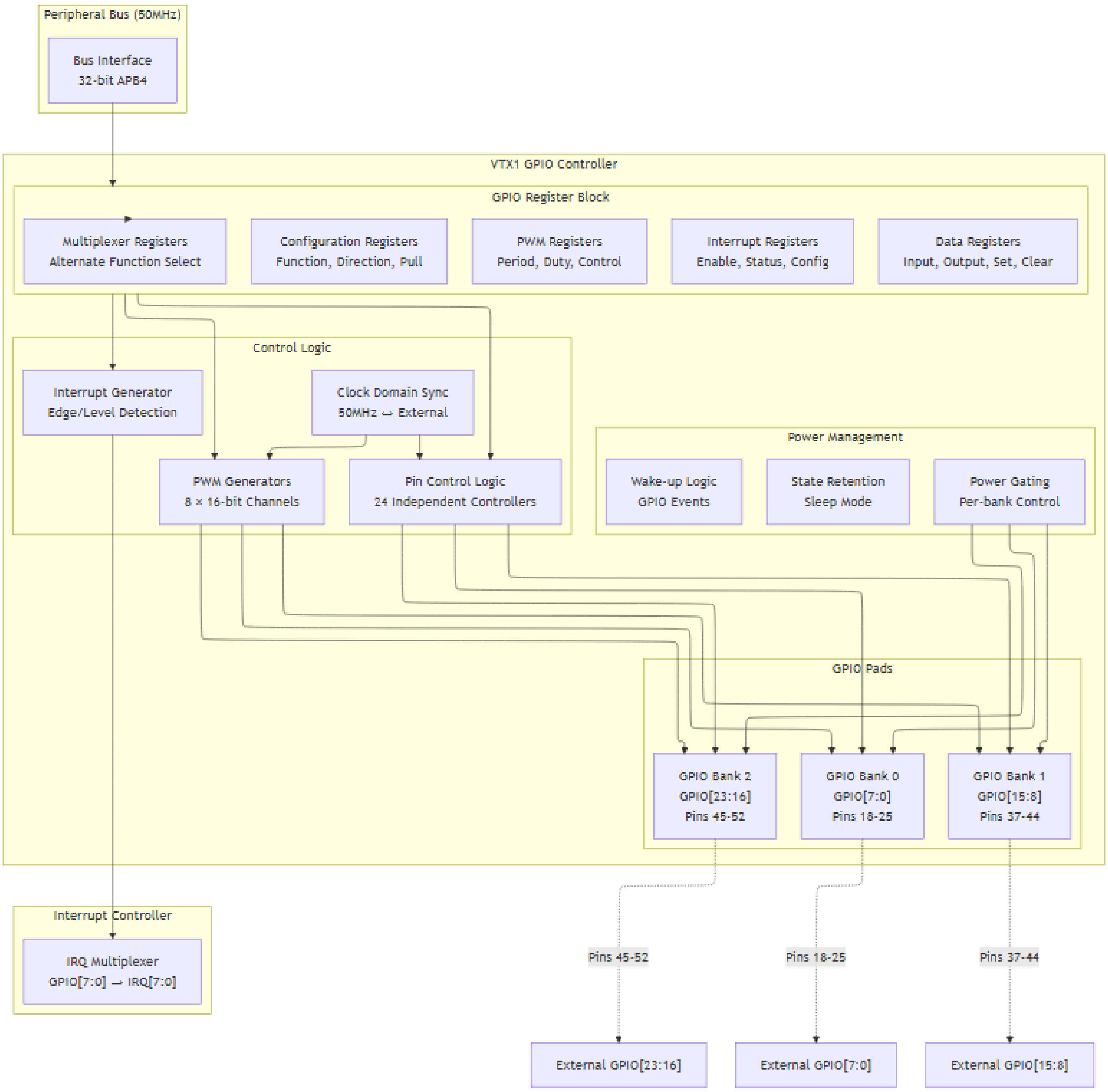
Diagnostic Registers:

- Interrupt source identification
- Timing violation detection
- Priority inversion monitoring
- Context save/restore verification

GPIO Controller

The VTX1 GPIO controller provides comprehensive general-purpose I/O functionality with 24 configurable pins, integrated PWM generation, interrupt capability, and power-aware operation modes. The controller supports both digital I/O and alternate function multiplexing for communication interfaces.

Hardware Architecture



Advanced GPIO Features and Pin Configuration

GPIO Pin Mapping:

GPIO	Pin	Bank	Primary Function	Alternate Functions
GPIO0	18	0	Digital I/O	PWM0, IRQ0, UART_CTS
GPIO1	19	0	Digital I/O	PWM1, IRQ1, UART_RTS
GPIO2	20	0	Digital I/O	PWM2, IRQ2, SPI_MOSI
GPIO3	21	0	Digital I/O	PWM3, IRQ3, SPI_MISO
GPIO4	22	0	Digital I/O	PWM4, IRQ4, SPI_SCK
GPIO5	23	0	Digital I/O	PWM5, IRQ5, SPI_SS
GPIO6	24	0	Digital I/O	PWM6, IRQ6, I2C_SDA
GPIO7	25	0	Digital I/O	PWM7, IRQ7, I2C_SCL
GPIO8	37	1	Digital I/O	Timer0_Out, DMA_REQ0
GPIO9	38	1	Digital I/O	Timer1_Out, DMA_ACK0

GPIO	Pin	Bank	Primary Function	Alternate Functions
GPIO10	39	1	Digital I/O	Timer0_Cap, DMA_REQ1
GPIO11	40	1	Digital I/O	Timer1_Cap, DMA_ACK1
GPIO12	41	1	Digital I/O	Comparator0_Out
GPIO13	42	1	Digital I/O	Comparator1_Out
GPIO14	43	1	Digital I/O	DAC0_Out
GPIO15	44	1	Digital I/O	DAC1_Out
GPIO16	45	2	Digital I/O	ADC0_In
GPIO17	46	2	Digital I/O	ADC1_In
GPIO18	47	2	Digital I/O	XTAL_Out
GPIO19	48	2	Digital I/O	XTAL_In
GPIO20	49	2	Digital I/O	External_CLK
GPIO21	50	2	Digital I/O	Test_Mode
GPIO22	51	2	Digital I/O	JTAG_TMS
GPIO23	52	2	Digital I/O	JTAG_TCK

Electrical Characteristics:

- **Output Drive Strength:** 2mA, 4mA, 8mA, 12mA (configurable per pin)
- **Input Threshold:** VIL=1.5V, VIH=3.5V (5V operation)
- **Output Levels:** VOL<0.4V, VOH>4.6V (5V operation)
- **Pull-up/Pull-down:** 10kΩ, 47kΩ, 100kΩ (configurable)
- **Slew Rate Control:** Fast (1ns), Medium (5ns), Slow (20ns)
- **Hysteresis:** 200mV minimum for noise immunity

Advanced Register Map:

GPIO_CONFIG0-7 (0x4000_2040-0x4000_205C) - Individual Pin Configuration

Bits	Field	Access	Description
31:28	DRIVE	RW	Drive strength: 0=2mA, 1=4mA, 2=8mA, 3=12mA
27:26	SLEW	RW	Slew rate: 0=fast, 1=medium, 2=slow, 3=reserved
25:24	PULL	RW	Pull config: 0=none, 1=up, 2=down, 3=keeper
23:20	ALT_FUNC	RW	Alternate function select (0-15)
19:16	IRQ_TYPE	RW	IRQ type: 0=disabled, 1=rising, 2=falling, 3=both, 4=high, 5=low
15:12	PWM_CHAN	RW	PWM channel assignment (0-7, 15=disabled)
11	FAST_SLEW	RW	Override slew rate for clock outputs
10	HYSTERESIS	RW	Enable input hysteresis
9	ANALOG_EN	RW	Enable analog function (ADC/DAC)
8	OPEN_DRAIN	RW	Enable open-drain output
7:4	Reserved	RO	Reserved for future use
3:0	FUNCTION	RW	Pin function: 0=input, 1=output, 2=alternate, 3=analog

PWM Generation:

GPIO_PWM_PERIODn (0x4000_2060 + n*8) - PWM Period Configuration

Bits	Field	Access	Description
31:16	PERIOD_CH1	RW	PWM period for channel (2n+1) in clock cycles
15:0	PERIOD_CH0	RW	PWM period for channel (2n+0) in clock cycles

GPIO_PWM_DUTYn (0x4000_2064 + n*8) - PWM Duty Cycle Configuration

Bits	Field	Access	Description
31:16	DUTY_CH1	RW	PWM duty cycle for channel (2n+1)
15:0	DUTY_CH0	RW	PWM duty cycle for channel (2n+0)

Interrupt Generation and Handling

Interrupt Capabilities:

- **Sources:** GPIO[7:0] can generate interrupts (IRQ 0-7)
- **Trigger Modes:** Rising edge, falling edge, both edges, high level, low level
- **Debouncing:** Hardware debounce with configurable time constant
- **Filtering:** Glitch filtering with 1-15 clock cycle rejection
- **Wake-up:** Can wake system from sleep modes
- **Latching:** Interrupt status latched until cleared by software

GPIO_INT_TYPEn (0x4000_207C + n*4) - Interrupt Type Configuration

Bits	Field	Access	Description
31:28	GPIO3_TYPE	RW	IRQ type for GPIO(4n+3)
27:24	GPIO2_TYPE	RW	IRQ type for GPIO(4n+2)
23:20	GPIO1_TYPE	RW	IRQ type for GPIO(4n+1)
19:16	GPIO0_TYPE	RW	IRQ type for GPIO(4n+0)
15:8	DEBOUNCE	RW	Debounce time: 0=none, 1-255=cycles
7:4	FILTER	RW	Glitch filter width in clock cycles
3:0	Reserved	RO	Reserved for future use

GPIO_INT_STATUS (0x4000_209C) - Interrupt Status Register

Bits	Field	Access	Description
31:24	Reserved	RO	Reserved for future use
23:0	INT_STATUS	RW1C	Interrupt status for GPIO[23:0], write 1 to clear

Performance Characteristics

Timing Specifications:

- **Setup Time:** 2ns before clock edge (50MHz)
- **Hold Time:** 1ns after clock edge (50MHz)
- **Input Delay:** <5ns from pad to register
- **Output Delay:** <8ns from register to pad
- **Register Access:** 1 clock cycle (50MHz = 20ns)

- **Bit Manipulation:** Atomic set/clear/toggle operations
- **Bulk Updates:** 8 pins per register write
- **Interrupt Response:** 4-6 cycles from edge to CPU
- **PWM Updates:** Real-time duty cycle modification
- **Maximum I/O Rate:** 25MHz toggle rate per pin

Power Management Integration

Power Management Features:

- **Bank-Level Gating:** Independent power control for each 8-pin bank
- **Retention Mode:** State preservation during sleep with minimal power
- **Wake-up Sources:** GPIO events can wake system from deep sleep
- **Dynamic Scaling:** Automatic drive strength adjustment based on load
- **Leakage Control:** High-impedance mode for unused pins

Power Consumption:

Operating Mode	Active	Sleep	Units
Digital I/O (per pin)	2.5	0.1	mA
PWM Generation (per channel)	1.8	0.0	mA
Interrupt Detection	0.5	0.3	mA
Total GPIO Controller	50	5	mA (all pins active)
Retention Mode	0	2	mA (state preserved)

Power Gating Control:

- **Bank 0 Gating:** GPIO[7:0] independent power domain
- **Bank 1 Gating:** GPIO[15:8] independent power domain
- **Bank 2 Gating:** GPIO[23:16] independent power domain
- **Wake-up Logic:** Always-on for interrupt generation
- **Retention Registers:** Critical state preserved during power-down

Enhanced Peripheral Controller Architecture

Overview

The VTX1 system implements sophisticated peripheral controllers with advanced features including DMA integration, interrupt handling, and comprehensive error management. All controllers use standardized 36-bit ternary interfaces and integrate seamlessly with the bus matrix architecture.

Enhanced GPIO Controller

Implementation Features:

- **24-Pin Configuration**: Comprehensive I/O capability with flexible pin assignment
- **Interrupt Support**: Individual pin interrupt generation with edge/level detection

- **DMA Integration**: Direct memory access for high-speed I/O operations
- **Alternate Functions**: Configurable pin multiplexing for UART/SPI/I2C interfaces
- **Power Management**: Individual pin power control and sleep mode support

Pin Configuration Matrix:

Pin Range	Primary Function	Alternate Function	Enhanced Features
GPIO[0:7]	General Purpose I/O	UART TX/RX, SPI MOSI/MISO	Interrupt capable, DMA ready, 3.3V/1.8V
GPIO[8:15]	General Purpose I/O	I2C SDA/SCL, SPI CLK/CS	Open-drain support, pull-up/down configurable
GPIO[16:23]	General Purpose I/O	PWM Output, Timer Input	High-speed capable, analog input ready

Register Interface:

Register	Offset	Access	Description
GPIO_DATA	0x00	R/W	Pin data register - 24-bit direct pin access
GPIO_DIR	0x04	R/W	Direction control - 0=input, 1=output
GPIO_ALT	0x08	R/W	Alternate function selection per pin
GPIO_PU	0x0C	R/W	Pull-up enable register
GPIO_PD	0x10	R/W	Pull-down enable register
GPIO_INT_EN	0x14	R/W	Interrupt enable per pin
GPIO_INT_TYPE	0x18	R/W	Interrupt type - edge/level selection
GPIO_INT_EDGE	0x1C	R/W	Edge type - rising/falling/both
GPIO_INT_STATUS	0x20	R/W1C	Interrupt status register
GPIO_DMA_EN	0x24	R/W	DMA enable per pin
GPIO_POWER	0x28	R/W	Power management control

DMA Integration:

```
// GPIO DMA Interface
output wire gpio_dma_req;           // DMA request signal
input  wire gpio_dma_ack;           // DMA acknowledge
output wire [7:0] gpio_dma_data;    // DMA data output
input  wire [7:0] gpio_dma_input;   // DMA data input
output wire [4:0] gpio_dma_pin;     // Pin number for DMA operation
```

Enhanced UART Controller

Advanced UART Features: - **DMA Integration**: Seamless integration with 8-channel DMA controller - **FIFO Management**: 32-byte TX/RX FIFOs with configurable thresholds - **Flow Control**: Hardware RTS/CTS flow control support - **Error Detection**: Comprehensive parity, framing, and overrun error detection - **Baud Rate Support**: Configurable baud rates from 1200 to 115200 bps

UART Configuration:

Feature	Configuration	Implementation Details
Baud Rate Generator	Programmable divisor	16-bit divisor for precise timing, crystal oscillator reference
Data Format	5-8 bits, 1-2 stop bits	Configurable parity (none, even, odd, mark, space)
FIFO Depth	32 bytes TX/RX	Configurable threshold levels for interrupt generation

Feature	Configuration	Implementation Details
Flow Control	RTS/CTS hardware	Automatic flow control with configurable thresholds

Register Interface:

Register	Offset	Access	Description
UART_DATA	0x00	R/W	Data register - TX/RX FIFO access
UART_CTRL	0x04	R/W	Control register - enable, format, flow control
UART_STATUS	0x08	R	Status register - FIFO levels, error flags
UART_BAUD	0x0C	R/W	Baud rate divisor register
UART_INT_EN	0x10	R/W	Interrupt enable register
UART_INT_STATUS	0x14	R/W1C	Interrupt status register
UART_DMA_CTRL	0x18	R/W	DMA control and threshold configuration

DMA Integration Example:

```
// UART DMA Interface
output wire uart_tx_dma_req;        // TX DMA request
output wire uart_rx_dma_req;        // RX DMA request
input  wire uart_tx_dma_ack;        // TX DMA acknowledge
input  wire uart_rx_dma_ack;        // RX DMA acknowledge
input  wire [7:0] uart_tx_dma_data; // TX DMA data
output wire [7:0] uart_rx_dma_data; // RX DMA data
```

Enhanced SPI Controller

SPI Master/Slave Implementation:

- **Dual Mode Operation**: Configurable master or slave mode operation
- **8 Chip Select Lines**: Support for up to 8 SPI slave devices
- **DMA Support**: High-speed data transfer with DMA integration
- **Interrupt Vectors**: Comprehensive interrupt support for all SPI events
- **Clock Configuration**: Programmable clock frequency and phase/polarity

SPI Configuration Matrix:

Mode	Clock Speed	Features
Master Mode	1MHz - 25MHz	8 chip selects, DMA, interrupts, burst transfers
Slave Mode	Up to 25MHz	Automatic slave response, DMA, interrupt on selection
Multi-Master	Arbitration support	Bus arbitration, collision detection, error recovery

Register Interface:

Register	Offset	Access	Description
SPI_DATA	0x00	R/W	Data register - TX/RX access
SPI_CTRL	0x04	R/W	Control register - mode, format, enable
SPI_STATUS	0x08	R	Status register - busy, FIFO status, errors
SPI_CLK_DIV	0x0C	R/W	Clock divider for SPI clock generation

Register	Offset	Access	Description
SPI_CS_CTRL	0x10	R/W	Chip select control - 8-bit CS selection
SPI_INT_EN	0x14	R/W	Interrupt enable register
SPI_INT_STATUS	0x18	R/W1C	Interrupt status register
SPI_DMA_CTRL	0x1C	R/W	DMA control and configuration

Enhanced I2C Controller

I2C Multi-Master Implementation:

- **Multi-Master Capability**: Full multi-master bus arbitration support
- **Clock Stretching**: Slave clock stretching with timeout protection
- **DMA Interface**: High-speed I2C transfers with DMA integration
- **SMBus Compatibility**: SMBus protocol extensions for system management
- **Error Recovery**: Comprehensive error detection and automatic recovery

I2C Advanced Features:

Feature	Implementation Details
Multi-Master Arbitration	Hardware arbitration with collision detection and automatic retry
Clock Stretching	Configurable timeout (1ms-100ms), automatic recovery on timeout
Address Recognition	7-bit and 10-bit address support, multiple slave address recognition
DMA Integration	Burst transfers up to 256 bytes, automatic address increment
SMBus Extensions	Packet Error Checking (PEC), Alert Response Address (ARA)

Register Interface:

Register	Offset	Access	Description
I2C_DATA	0x00	R/W	Data register - TX/RX access
I2C_ADDR	0x04	R/W	Address register - slave address configuration
I2C_CTRL	0x08	R/W	Control register - start, stop, ack, enable
I2C_STATUS	0x0C	R	Status register - busy, arbitration, errors
I2C_CLK_DIV	0x10	R/W	Clock divider for I2C clock generation
I2C_TIMEOUT	0x14	R/W	Timeout configuration for clock stretching
I2C_INT_EN	0x18	R/W	Interrupt enable register
I2C_INT_STATUS	0x1C	R/W1C	Interrupt status register
I2C_DMA_CTRL	0x20	R/W	DMA control and burst configuration

DMA Controller Integration

8-Channel DMA Architecture:

The DMA controller provides sophisticated peripheral integration with the following capabilities:

Channel Configuration:

Channel	Peripheral	Transfer Type	Enhanced Features
DMA0	UART TX	Memory to peripheral	Burst support, interrupt on completion

Channel	Peripheral	Transfer Type	Enhanced Features
DMA1	UART RX	Peripheral to memory	FIFO threshold, automatic flow control
DMA2	SPI TX	Memory to peripheral	Multi-device support, chip select automation
DMA3	SPI RX	Peripheral to memory	High-speed burst, interrupt aggregation
DMA4	I2C TX	Memory to peripheral	Multi-master aware, arbitration support
DMA5	I2C RX	Peripheral to memory	Address filtering, SMBus packet support
DMA6	GPIO	Bidirectional	Pattern generation, event capture
DMA7	Memory	Memory to memory	High-speed copy, data transformation

DMA Performance Characteristics:

- **Throughput**: Up to 100MB/s per channel with bus matrix optimization
- **Latency**: 2-cycle request-to-transfer latency for critical operations
- **Burst Size**: Configurable 1-256 byte bursts with automatic address increment
- **Priority**: 8-level priority system with round-robin within priority levels

Peripheral Error Handling and Recovery

Comprehensive Error Framework:

All enhanced peripheral controllers implement the VTX1 standardized error handling framework:

Error Classification:

Code	Error Type	Peripheral Scope	Recovery Mechanism
0x0	VTX1_ERROR_NONE	All peripherals	Normal operation
0x1	VTX1_ERROR_TIMEOUT	UART, SPI, I2C	Automatic retry, timeout adjustment
0x2	VTX1_ERROR_INVALID_ADDR	All peripherals	Address validation, error reporting
0x3	VTX1_ERROR_PROTOCOL	SPI, I2C	Protocol reset, state machine restart
0x4	VTX1_ERROR_RESOURCE	DMA channels	Channel arbitration, queued requests
0x5	VTX1_ERROR_OVERRUN	UART, SPI	FIFO flush, flow control activation
0x6	VTX1_ERROR_UNDERRUN	UART, SPI	FIFO refill, transmission pause
0x7	VTX1_ERROR_COLLISION	I2C multi-master	Arbitration retry, backoff algorithm
0x8	VTX1_ERROR_FRAMING	UART	Error flag, character discard
0x9	VTX1_ERROR_PARITY	UART	Error flag, retransmission request

Automatic Recovery Mechanisms:

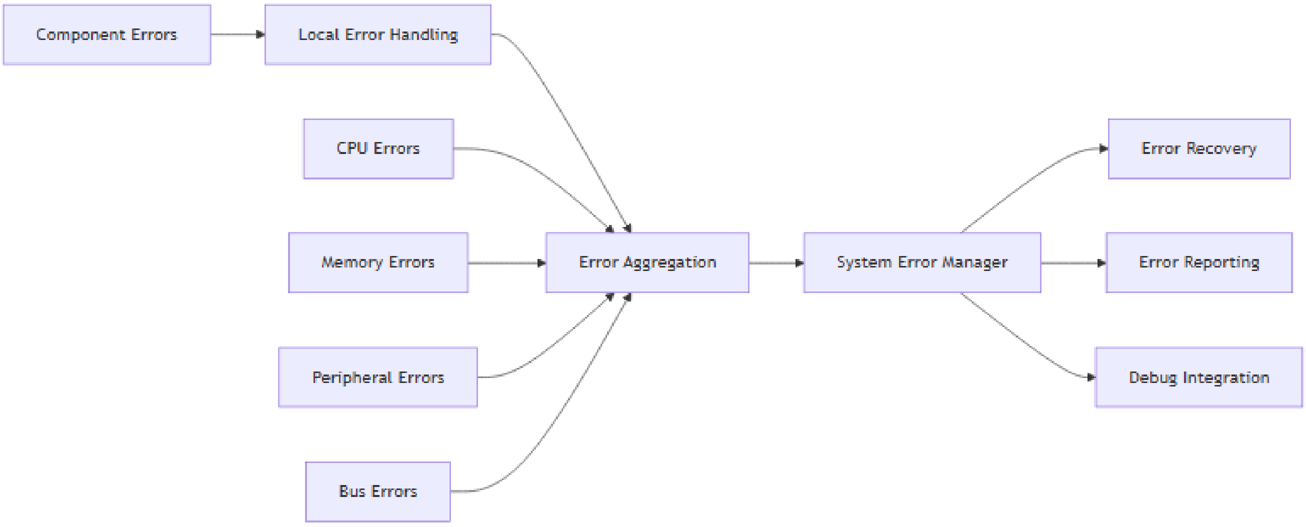
- **Timeout Recovery**: Configurable timeout thresholds with automatic operation restart
- **FIFO Management**: Automatic overflow/underflow handling with flow control
- **Protocol Recovery**: State machine reset and protocol re-initialization
- **Error Logging**: Comprehensive error statistics for system analysis

System-Wide Error Handling

Comprehensive Error Framework:

The VTX1 implements a sophisticated error handling framework across all system components:

Error Propagation Architecture:



System Error Classification:

Code	Error Type	System Scope	Recovery Mechanism
0x0	VTX1_ERROR_NONE	System-wide	Normal operation
0x1	VTX1_ERROR_TIMEOUT	All components	Timeout adjustment, retry mechanisms
0x2	VTX1_ERROR_INVALID_ADDR	Memory system	Address validation, range checking
0x3	VTX1_ERROR_PROTOCOL	Bus, peripherals	Protocol reset, state machine restart
0x4	VTX1_ERROR_RESOURCE	System-wide	Resource reallocation, priority adjustment
0xA	VTX1_ERROR_BUS_FAULT	Bus matrix	Bus reset, transaction retry
0xB	VTX1_ERROR_CACHE_FAULT	Cache system	Cache flush, coherency recovery
0xC	VTX1_ERROR_MEMORY_FAULT	Memory system	ECC correction, memory refresh
0xD	VTX1_ERROR_PERIPHERAL_FAULT	Peripherals	Peripheral reset, reconfiguration
0xE	VTX1_ERROR_DEBUG_FAULT	Debug system	Debug reset, trace buffer recovery
0xF	VTX1_ERROR_FATAL	System-wide	System reset, fault isolation

System Performance Monitoring

Comprehensive Performance Metrics:

The VTX1 provides extensive performance monitoring capabilities:

System-Level Metrics:

Metric Category	Measurement Scope	Implementation Features
Bus Performance	Bus matrix utilization	Transaction counting, latency measurement, bandwidth analysis
CPU Performance	Pipeline efficiency	Instruction throughput, hazard analysis, microcode utilization
Memory Performance	Cache and memory access	Hit/miss ratios, access patterns, bandwidth utilization
Peripheral Performance	I/O operations	Transfer rates, error rates, utilization analysis

Real-Time Monitoring:

- **Hardware Counters**: 32-bit performance counters with overflow protection

- **Sampling Windows**: Configurable measurement periods for trend analysis
- **Threshold Alerts**: Configurable performance threshold monitoring
- **Debug Integration**: Performance data available through debug interface == Core Processing Unit === Register Organization ==== Register Map

Register	Name	Purpose	Width	Special Behavior	Usage
T0-T3	GPRs	General Purpose Registers	Trit	-	Primary computation
T4-T6	Extended GPRs	Extended working registers	Trit	-	Extended computation
TA	Accumulator	ALU/FPU Accumulator	Trit	Implicit in some ops	Accumulator operations
TB	Base Pointer	Stack/frame base pointer	Trit	Used for addressing	Memory addressing
TC	Program Counter	Program Counter	Trit	Auto-increment/fetch	Control Register
TS	Status	Flags, condition codes	Trit	Affects branching	Control Register
TI	Instruction Register	Current instruction	Trit	Pipeline control	Control Register
VA	Vector Accumulator	Vector operations	3×Trit	SIMD operations	Vector operations
VT	Vector Temporary	Vector operations	3×Trit	SIMD operations	Vector operations
VB	Vector Base	Vector operations	3×Trit	SIMD operations	Vector operations
FA	FP Accumulator	Floating-point operations	Trit	FP operations	Floating-point
FT	FP Temporary	Floating-point operations	Trit	FP operations	Floating-point
FB	FP Base	Floating-point operations	Trit	FP operations	Floating-point

Register Access

- 6 read ports
- 3 write ports
- Zero-wait state access
- Bypass paths for all ports
- Register file organization: 3-way interleaved
- Access timing: 1 cycle

Register Features

- Balanced ternary representation
- Direct access in 1 cycle
- Bypass paths for pipeline
- Register renaming support
- Vector register support
- FPU register support
- Control register protection

Enhanced Pipeline Architecture

The VTX1 core implements a sophisticated 4-stage pipeline architecture optimized for balanced ternary operations and VLIW instruction processing. The pipeline integrates seamlessly with the enhanced TCU interface and microcode execution system for maximum performance and flexibility.

Pipeline Characteristics

- **Pipeline Depth**: 4 stages (Fetch, Decode, Execute, Writeback)
- **VLIW Support**: 3 parallel operations per cycle with sophisticated dependency resolution
- **Microcode Integration**: Hardware microcode sequencer for complex operations (26 microcode routines)
- **TCU Enhanced Interface**: 7-state handshaking mechanism with adaptive timeout management
- **Error Integration**: Comprehensive error handling with automatic recovery mechanisms
- **Performance Monitoring**: Hardware performance counters and pipeline utilization tracking

Enhanced TCU Interface Architecture

The Ternary Control Unit (TCU) interface has been significantly enhanced with sophisticated handshaking and error management:

State Machine Architecture (7 States):

1. **VTX1_TCU_IDLE**: Default state - ready for new instruction requests
2. **VTX1_TCU_FETCH_REQ**: Instruction fetch request initiated
3. **VTX1_TCU_FETCH_WAIT**: Waiting for memory/cache response
4. **VTX1_TCU_DECODE_WAIT**: Instruction decode and dependency analysis
5. **VTX1_TCU_EXECUTE**: Instruction execution with microcode coordination
6. **VTX1_TCU_WRITEBACK**: Result writeback and completion signaling
7. **VTX1_TCU_ERROR**: Error state with recovery mechanisms

Adaptive Timeout Management:

- **Simple Operations**: 4-cycle timeout for register-to-register operations
- **Memory Operations**: 16-cycle timeout for cache hits, 64-cycle for memory access
- **Complex Operations**: 128-cycle timeout for microcode-assisted operations
- **Microcode Execution**: 256-cycle timeout for complex microcode sequences

Enhanced Handshaking Protocol:

```
// TCU Enhanced Interface Signals
input wire tcu_request;              // TCU operation request
input wire [31:0] tcu_instruction;   // 32-bit instruction word
input wire [1:0] tcu_op_type;        // Operation complexity classification
output wire tcu_ready;               // TCU ready for new operation
output wire tcu_valid;               // Operation result valid
output wire [31:0] tcu_result;       // Operation result data
output wire tcu_error;               // Error condition flag
```

```
output wire [3:0] tcu_error_code;    // Standardized error classification
```

Microcode Integration System

Microcode ROM Implementation:

- **Capacity**: 1024 × 32-bit microcode storage (4KB total)
- **Operations**: 26 complex operations with microcode assistance
- **Sequencer**: Enhanced microcode sequencer with adaptive timeout management
- **Integration**: Seamless handoff between pipeline and microcode execution

Microcode Operations (Examples):

- **Division Operations**: 32-cycle microcode sequence for integer division
- **Multiplication**: Optimized ternary multiplication with partial products
- **Floating-Point**: IEEE 754 compatible operations in ternary domain
- **Vector Operations**: SIMD operations with ternary optimization
- **System Operations**: Context switching, exception handling, cache management

Microcode Performance Characteristics:

- **Latency**: 8-256 cycles depending on operation complexity
- **Throughput**: Pipeline continues with independent operations
- **Error Handling**: Integrated with VTX1 error framework
- **Debugging**: Full microcode visibility through debug interface

Pipeline Operation

The VTX1 pipeline is designed to efficiently execute instructions with minimal stalls and maximum throughput. The architecture supports VLIW instructions, allowing multiple operations to be executed in parallel. The pipeline stages are optimized for balanced ternary operations, with a unified Ternary Computing Unit (TCU) handling arithmetic, logic, and vector operations.

Pipeline Stages Overview

The VTX1 pipeline consists of four main stages, each responsible for a specific part of the instruction execution process. The stages are designed to work in parallel, allowing for high throughput and efficient execution of VLIW instructions.

1. **Fetch Stage (TC, Instruction Fetch)** – Program Counter (TC) is updated. – Instruction is fetched from cache/memory. – Branch prediction (if applicable) is performed.
2. **Decode Stage (VLIW Decoder)** – VLIW instruction is decoded (supports parallel operations). – Register file access (read) is performed. – Hazard detection (and forwarding) is handled.
3. **Execute Stage (TCU)** – The Ternary Computing Unit (TCU) combines ALU, Ternary FPU, and SIMD operations. – Arithmetic, logic, transcendental, and SIMD/vector operations are executed in parallel (as dictated by the VLIW encoding).
   - Microcode offload for the complex operations – Memory access (load/store) and branch resolution are also performed.

4. **Writeback Stage** – Register file updates (write) are performed. – Status flag updates (e.g. condition codes) are applied. – Result forwarding (bypass) is applied if needed.

Enhanced Ternary Computing Unit (TCU) Implementation

The VTX1 CPU implements a sophisticated Ternary Computing Unit (TCU) with enhanced microcode integration and advanced handshaking mechanisms. The implementation includes adaptive timeout handling, comprehensive error management, and performance monitoring capabilities.

Enhanced TCU Interface Architecture

Microcode Integration System:

The implementation includes a sophisticated enhanced interface for microcode operations:

```
// Enhanced TCU Interface - Phase 4 Implementation
input  wire                      microcode_enable,      // Enhanced microcode enable
input  wire [3:0]                microcode_operation,    // Extended operation codes
input  wire [VTX1_WORD_WIDTH-1:0] microcode_operand_a, // 36-bit ternary operands
input  wire [VTX1_WORD_WIDTH-1:0] microcode_operand_b,
input  wire [VTX1_WORD_WIDTH-1:0] microcode_operand_c,
output reg  [VTX1_WORD_WIDTH-1:0] microcode_result,    // 36-bit ternary result
output reg                       microcode_valid,       // Result valid flag
output reg                       microcode_ready,       // Ready for operation
output reg                       microcode_error,       // Error condition
```

Advanced Handshaking State Machine:

The TCU interface implements a sophisticated 7-state handshaking mechanism with VTX1 standardized states:

State	Purpose	Implementation Features
IDLE	Ready for new operations	Low power mode, monitoring for requests
REQUEST	Operation request initiated	Operand validation, resource allocation
WAIT_ACK	Waiting for TCU acknowledgment	Timeout monitoring, error detection
EXECUTING	Operation in progress	Progress tracking, intermediate monitoring
WAIT_RESULT	Waiting for completion	Result validation, error checking
COMPLETE	Operation completed successfully	Result forwarding, statistics update
ERROR	Error condition handling	Error classification, recovery initiation

Adaptive Timeout Management:

The implementation includes sophisticated timeout calculation based on operation complexity:

```
// Adaptive timeout calculation function
function [31:0] get_operation_timeout;
    input [3:0] op;
    case (op)
        4'h0-4'h2: get_operation_timeout = VTX1_TIMEOUT_SIMPLE;        // ADD, SUB, MUL: 100 cycles
        4'h3-4'h5: get_operation_timeout = VTX1_TIMEOUT_COMPLEX;       // DIV, MOD, SQRT: 500
cycles
        4'h6-4'h7: get_operation_timeout = VTX1_TIMEOUT_TRANSCENDENTAL; // TRIG functions: 1000
```

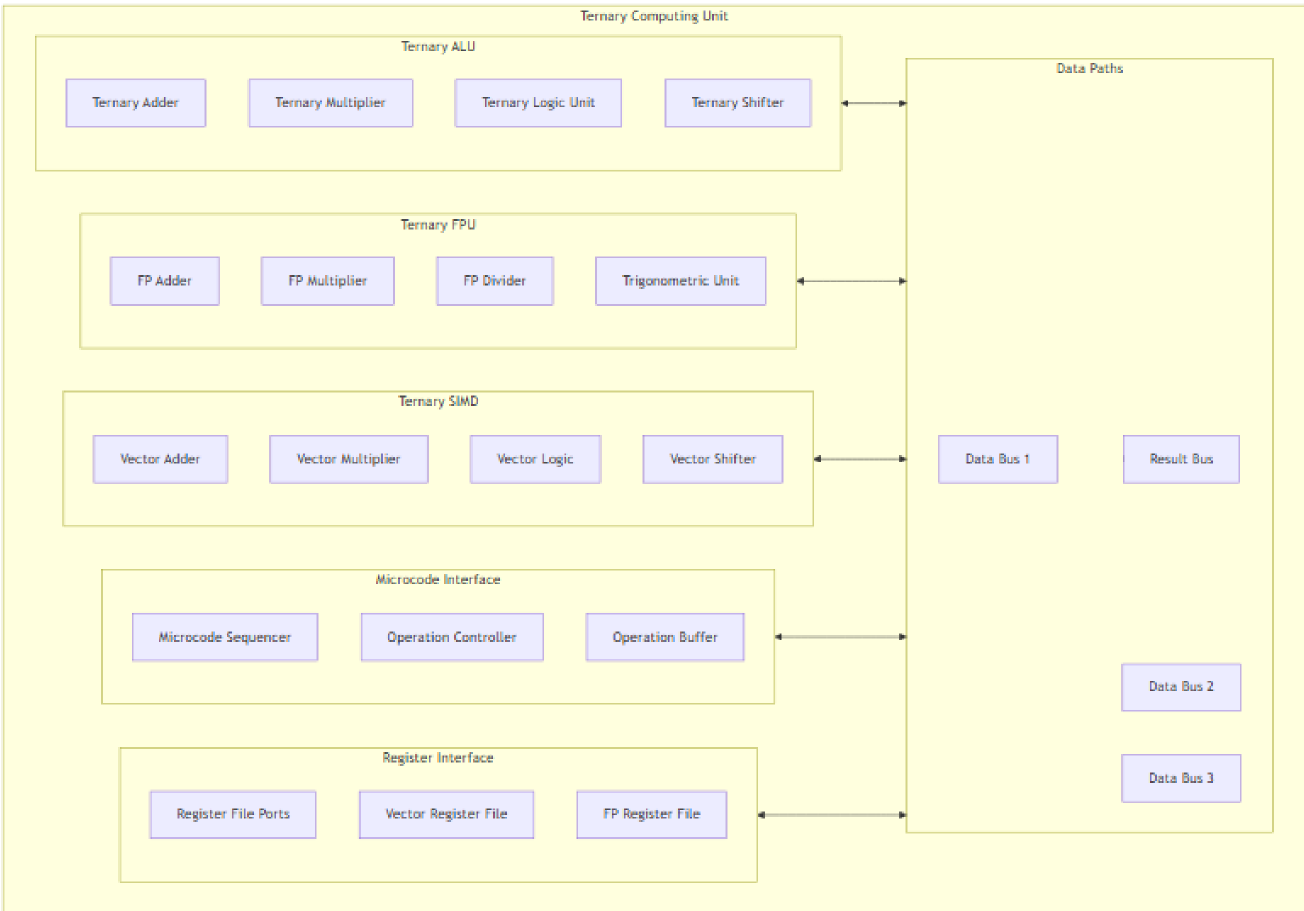
```
cycles
        4'h8-4'hA: get_operation_timeout = VTX1_TIMEOUT_VECTOR;         // Vector ops: 300 cycles
        4'hB-4'hC: get_operation_timeout = VTX1_TIMEOUT_MEMORY;         // Memory ops: 200 cycles
        4'hD-4'hF: get_operation_timeout = VTX1_TIMEOUT_SYSTEM;         // System ops: 150 cycles
    endcase
endfunction
```

Performance Monitoring Integration:

The enhanced TCU interface provides comprehensive performance monitoring:

Metric	Signal	Implementation Purpose
Operation Cycles	operation_cycles[31:0]	Cycle count for current operation execution
Total Operations	total_operations[31:0]	Cumulative operation counter for performance analysis
Error Count	error_count[31:0]	Error occurrence tracking for reliability assessment
Interface State	interface_state[3:0]	Current state machine state for debugging

TCU Block Diagram



TCU Operation Modes

1. **Parallel Execution Mode**
    - Up to 3 operations per cycle
    - Operation combinations:
    - 2 ALU + 1 Memory

- 1 ALU + 1 FPU + 1 SIMD
- 3 ALU (different units)
- Register file: 6 read ports, 3 write ports
- Zero-wait state for register access

2. **Microcode Offload Mode**
   - Complex operations offloaded to microcode
   - Examples:
   - Transcendental functions
   - Complex vector operations
   - Division and square root
   - String operations
   - Microcode routines stored in dedicated ROM
   - Parallel execution with main TCU

Functional Units

1. **Ternary ALU**
   - Basic Operations (1 cycle):
   - Addition/Subtraction
   - Multiplication
   - Logic operations (AND, OR, NOT)
   - Shifts and rotates
   - Complex Operations (microcode):
   - Division
   - Square root
   - Population count
   - Bit manipulation
2. **Ternary FPU**
   - Basic Operations (2-3 cycles):
   - Addition/Subtraction
   - Multiplication
   - Comparison
   - Complex Operations (microcode):
   - Division
   - Square root
   - Trigonometric functions
   - Exponential/Logarithmic
   - FPU Features:
   - Ternary floating-point format

- 32-bit precision
- Rounding modes
- Exception handling

3. **Ternary SIMD**
   - Vector Operations (1-2 cycles):
   - Vector add/sub
   - Vector multiply
   - Vector logic
   - Vector shift
   - Complex Operations (microcode):
   - Vector reduction
   - Vector permutation
   - Vector search
   - Vector comparison
   - SIMD Features:
   - 3-way parallel processing
   - Vector length: 3, 9, or 27 elements
   - Masked operations
   - Scatter/gather support

Microcode Offloading

1. **Offloaded Operations**
   - Transcendental functions
   - Complex vector operations
   - Division and square root
   - String and memory operations
   - System operations
2. **Microcode Interface**
   - Operation buffer: 4 entries
   - Result buffer: 2 entries - Status and control registers
   - Interrupt handling (see `system.adoc` for complete interrupt controller architecture)
3. **Performance Characteristics**
   - Basic operations: 1-3 cycles
   - Microcode operations: 4-16 cycles
   - Parallel throughput: 3 ops/cycle
   - Microcode throughput: 1 op/cycle

Instruction Set Architecture

The VTX1 implements a streamlined ternary ISA optimized for balanced ternary operations and VLIW execution. The instruction set is carefully designed to provide comprehensive functionality while maintaining implementation efficiency.

ISA Characteristics

Instruction Count: 78 total instructions

- 52 Native hardware instructions (1-3 cycles)
- 26 Microcode instructions (4-16 cycles)

Instruction Format:

- VLIW 96-bit instruction word (3×32-bit operations)
- Ternary-optimized encoding
- Support for parallel execution

Register Set: (See Register Organization for complete specifications)

- 7 General purpose registers (T0-T6)
- 2 Special registers (TA accumulator, TB base pointer)
- 3 Control registers (TC, TS, TI)
- 3 Vector registers (VA, VT, VB)
- 3 FPU registers (FA, FT, FB)

Addressing Modes:

- Register direct
- Immediate (11-bit)
- Base + offset (TB relative)
- TC relative (for branches)
- Vector indexed

Operation Categories

1. **Arithmetic Operations**
    - Native: ADD, SUB, MUL, INC, DEC, NEG, CMP
    - Microcode: DIV, MOD, UDIV, UMOD, SQRT, ABS
2. **Logic Operations**
    - Native: AND, OR, NOT, XOR, TEST
    - All operations support ternary logic natively
3. **Memory Operations**
    - Native: LD, ST, VLD, VST, FLD, FST, LEA, PUSH
    - Microcode: CACHE, FLUSH, MEMBAR

4. **Control Operations**
    - Native: JMP, JAL, JR, JALR, branches, CALL, RET
    - Microcode: SYSCALL, BREAK, HALT
5. **Vector Operations**
    - Native: VADD, VSUB, VMUL, VAND, VOR, VNOT, shifts
    - Microcode: VDOT, VREDUCE, VMAX, VMIN, VSUM, VPERM
6. **Floating-Point Operations**
    - Native: FADD, FSUB, FMUL, FCMP, FMOV, FNEG
    - Microcode: SIN, COS, TAN, ASIN, ACOS, ATAN, EXP, LOG

Design Philosophy

The VTX1 ISA follows these key principles:

1. **Balanced Complexity**
    - Common operations execute in hardware (fast)
    - Complex operations use microcode (flexible)
    - Clear performance boundaries
2. **Ternary Optimization**
    - All operations support balanced ternary (-1, 0, +1)
    - Efficient ternary arithmetic implementation
    - Native ternary logic operations
3. **VLIW Efficiency**
    - Instructions designed for parallel execution
    - Minimal resource conflicts
    - Compiler-friendly scheduling
4. **Implementation Efficiency**
    - Streamlined instruction set reduces gate count
    - Microcode handles complexity without hardware cost
    - Optimal balance of performance vs. area

Instruction Set Statistics

Category	Native	Microcode	Total	Primary Use Case
ALU Operations	16	6	22	Arithmetic and logic
Memory Operations	8	3	11	Data movement
Control Operations	12	3	15	Program flow
Vector Operations	8	6	14	SIMD processing
FPU Operations	6	8	14	Floating-point math
System Operations	2	0	2	System control
Total	**52**	**26**	**78**	**Complete ISA**

Native Hardware Instructions (52 Instructions, 1-3 cycles)

ALU Operations (16 instructions)

```
ADD, SUB, MUL     - Basic arithmetic operations
AND, OR, NOT, XOR - Logic operations
SHL, SHR, ROL, ROR - Shift and rotate operations
CMP, TEST         - Comparison and test operations
INC, DEC, NEG     - Increment, decrement, negate operations
```

Memory Operations (8 instructions)

```
LD, ST           - Load/store operations
VLD, VST         - Vector load/store operations
FLD, FST         - Floating-point load/store operations
LEA, PUSH        - Load effective address, push to stack
```

Control Operations (12 instructions)

```
JMP, JAL, JR, JALR    - Jump operations
BEQ, BNE, BLT, BGE    - Conditional branches (signed)
BLTU, BGEU            - Conditional branches (unsigned)
CALL, RET             - Function call/return
```

Vector Operations (8 instructions)

```
VADD, VSUB, VMUL - Vector arithmetic operations
VAND, VOR, VNOT  - Vector logic operations
VSHL, VSHR       - Vector shift operations
```

FPU Operations (6 instructions)

```
FADD, FSUB, FMUL - Floating-point arithmetic
FCMP, FMOV, FNEG - Floating-point compare, move, negate
```

System Operations (2 instructions)

```
NOP              - No operation
WFI              - Wait for interrupt (integrates with interrupt controller in system.adoc)
```

Microcode Instructions (26 Instructions, 4-16 cycles)

Complex Arithmetic (6 instructions)

```
DIV, MOD         - Division and modulo (signed)
UDIV, UMOD       - Division and modulo (unsigned)
SQRT, ABS        - Square root, absolute value
```

Transcendental Functions (8 instructions)

```
SIN, COS, TAN    - Trigonometric functions
ASIN, ACOS, ATAN - Inverse trigonometric functions
EXP, LOG         - Exponential and logarithm
```

Advanced Vector Operations (6 instructions)

```
VDOT             - Vector dot product
VREDUCE          - Vector reduction operations
VMAX, VMIN       - Vector maximum/minimum
VSUM, VPERM      - Vector sum, permutation
```

Memory Management (3 instructions)

```
CACHE            - Cache control operations
FLUSH            - Cache flush operations
MEMBAR           - Memory barrier operations
```

System Control (3 instructions)

```
SYSCALL          - System call
BREAK            - Debug breakpoint
HALT             - System halt
```

Instruction Categories by Execution Unit

1. **TCU Native Operations (1-3 cycles)**
   - Execute directly in Ternary Computing Unit
   - Single or dual-cycle execution
   - Support VLIW parallel execution
   - Minimal control overhead
2. **Microcode Operations (4-16 cycles)**
   - Implemented using microcode sequencer
   - Multi-cycle execution patterns
   - May require multiple TCU operations
   - Cannot execute in parallel with other operations

Design Rationale

The streamlined ISA removes exotic operations that provided limited benefit while maintaining comprehensive functionality:

Removed Operations:

- Complex matrix operations (rarely used in embedded applications)

- Advanced permutation operations (can be composed from simpler ops)
- Hardware DMA control (moved to memory-mapped interface)
- Exotic transcendental functions (FATAN2 → software implementation)
- Complex bit manipulation (can be composed from basic operations)

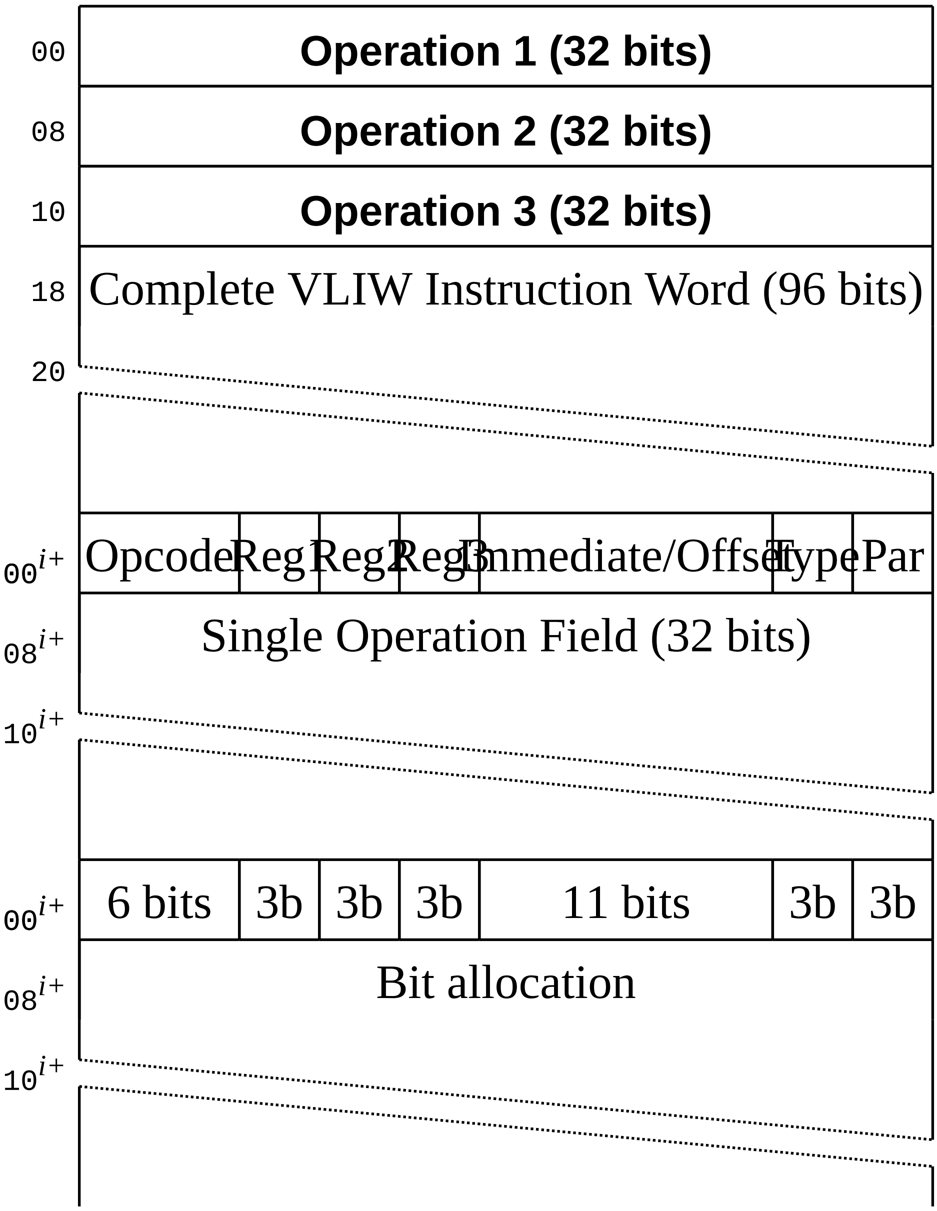
Benefits:

- Reduced hardware complexity (~30% gate count reduction)
- Clearer performance characteristics
- Simplified compiler implementation
- Maintainable microcode complexity
- Optimal balance of functionality vs. implementation cost

VLIW Architecture

The VTX1 ISA is designed to support a wide range of operations using a Very Long Instruction Word (VLIW) format, allowing for parallel execution of multiple operations in a single instruction. The architecture supports both ternary and binary operations, with a focus on efficient execution and minimal gate count.

VLIW Format



- 96-bit instruction word
- 3 operations per cycle
- Operation field (32 bits):
- 6-bit opcode
- 3×3-bit register fields
- 11-bit immediate/offset
- 3-bit operation type
- 3-bit parallel flags

Operation Types

- Arithmetic Operations
- ADD, SUB, MUL, DIV
- Ternary arithmetic
- Vector arithmetic
- FP arithmetic

- Logic Operations
- AND, OR, NOT
- Ternary logic
- Vector logic
- Bit manipulation
- Memory Operations
- Load/Store
- Vector load/store
- Cache control
- Memory barrier - Control Operations
- Branch/Jump
- Call/Return
- System control
- Interrupt handling (detailed in `system.adoc`)

Register Usage

For complete register specifications, see Register Organization section above.

Register Categories:

- General Purpose: T0-T6 (7 registers)
- Special Purpose: TA (Accumulator), TB (Base Pointer)
- Control: TC (PC), TS (Status), TI (Instruction)
- Vector: VA, VT, VB (3 vector registers)
- FPU: FA, FT, FB (3 floating-point registers)

Addressing Modes

- Register Direct
- Immediate
- Base + Offset
- Base + Index
- TC Relative
- Vector Indexed

Operation Scheduling

- Static Scheduling
- Compiler-driven
- Resource allocation
- Dependency resolution

- Parallel operation packing
- Dynamic Scheduling
- Microcode control
- Hazard detection
- Result forwarding
- Exception handling

Parallel Execution

- Operation Combinations
- 2 ALU + 1 Memory
- 1 ALU + 1 FPU + 1 SIMD
- 3 ALU (different units)
- Resource Constraints
- Register file ports
- Functional units
- Memory ports
- Control flow

Instruction Examples

```
Example 1: ALU + Memory + Control
[ALU: ADD T0, T1, T2] [MEM: LD T3, [TB+1]] [CTRL: NOP]

Example 2: Dual ALU + Memory
[ALU: MUL T0, T1, T2] [ALU: ADD T3, T4, T5] [MEM: ST T6, [TB+2]]

Example 3: Vector + ALU
[VEC: VADD VA, VT, VB] [ALU: SUB T3, T4, T5] [CTRL: NOP]
```

Microcode Architecture

The VTX1 microcode system implements complex operations that would require significant hardware resources if implemented directly. The microcode approach provides flexibility while maintaining reasonable performance for less frequently used operations.

Microcode Implementation

1. **Microcode ROM**
    - 4KB microcode storage
    - 32-bit microword format
    - Supports 26 complex operations
    - Optimized for size and performance
2. **Microcode Sequencer**

- Integrated with pipeline control
- Automatic hazard detection
- Result forwarding support
- Exception handling integration

3. **Performance Characteristics**
    - Complex operations: 4-16 cycles
    - Single operation execution (no parallel)
    - Automatic pipeline coordination
    - Transparent to programmer

Microcode Operations by Category

1. **Complex Arithmetic (6 operations)**
    - Division algorithms (signed/unsigned)
    - Modulo operations
    - Square root implementation
    - Absolute value with exception handling
2. **Transcendental Functions (8 operations)**
    - CORDIC-based trigonometric functions
    - Taylor series implementations
    - Optimized for ternary representation
    - IEEE 754 compatibility
3. **Advanced Vector Operations (6 operations)**
    - Reduction algorithms
    - Complex permutation patterns
    - Optimized parallel processing
    - Memory-efficient implementations
4. **Memory Management (3 operations)**
    - Cache control and coherency
    - Memory barrier implementations
    - Performance optimization
5. **System Control (3 operations)**
    - System call interface
    - Debug and test support
    - Power management integration

Microcode Format

Control Field (12 bits)	Data Field (12 bits)	Address Field (8 bits)
Description of control signals	Microcode data/operation	Microcode address/offset

Control Field Encoding: - [11:9] Execution Unit Select (ALU/FPU/VEC) - [8:6] Operation Subtype - [5:3] Register Control - [2:0] Flow Control

Data Field Encoding: - [11:6] Immediate Data/Constants - [5:3] Source Register Select - [2:0] Destination Register Select

Address Field Encoding: - [7:0] Next Microinstruction Address/Offset

Design Benefits

1. **Hardware Efficiency**
    - Reduced gate count for complex operations
    - Shared execution resources
    - Simplified hardware design
2. **Flexibility**
    - Easy to modify algorithms
    - Support for future enhancements
    - Bug fixes without hardware changes
3. **Performance Balance**
    - Fast execution for common operations
    - Acceptable performance for complex operations
    - Optimal resource utilization

Instruction Encoding

For detailed VLIW instruction format specifications, see VLIW Architecture section above.

Operation Types - 000: ALU Operation - 001: Memory Operation - 010: Control Operation - 011: Vector Operation - 100: FPU Operation - 101: System Operation - 110: Microcode Operation - 111: Reserved

Parallel Flags - 000: Serial Execution - 001: Parallel with ALU - 010: Parallel with Memory - 011: Parallel with Control - 100: Full Parallel - 101-111: Reserved

Exception Handling

1. **Exception Types**
    - Hardware Exceptions
    - Illegal Instruction
    - Memory Access
    - Division by Zero
    - Overflow
    - Software Exceptions
    - System Call
    - Breakpoint

- Watchpoint
- External Exceptions
- Interrupt
- Reset
- NMI

2. **Exception Handling**
   - Vector Table
   - Context Save
   - Exception Service
   - Context Restore

Ternary Logic Implementation

This section consolidates all ternary logic implementation details referenced throughout the CPU specification.

Implementation Specifications

Authoritative References:

- **Ternary Logic Encoding:** See Ternary Logic Encoding for complete voltage level and encoding specifications
- **Power Specifications:** See Power Consumption Specifications for complete dual-voltage power requirements

Physical Implementation:

- **Supply Voltage:** 5.0 V nominal (4.5 V to 5.5 V range)
- **Level Conversion:** 5V-tolerant CMOS level shifters for compatibility
- **Input Protection:** 5V-tolerant I/O cells with comprehensive protection
- **ESD Protection:** 2 kV HBM (Human Body Model), 200 V MM (Machine Model)
- **Noise Margins:** ±0.5V around each logic level
- **Power Consumption:** 0.15 nJ per ternary operation

Ternary Arithmetic Operations

1. Balanced Ternary Addition

Truth table with carry out for balanced ternary addition:

A	B	Cin	Sum	Cout
-1	-1	-1	+1	-1
-1	-1	0	0	-1
-1	-1	+1	-1	-1
-1	0	-1	0	-1
-1	0	0	-1	0

A	B	Cin	Sum	Cout
-1	0	+1	0	0
-1	+1	-1	-1	0
-1	+1	0	0	0
-1	+1	+1	+1	0
0	-1	-1	0	-1
0	-1	0	-1	0
0	-1	+1	0	0
0	0	-1	-1	0
0	0	0	0	0
0	0	+1	+1	0
0	+1	-1	0	0
0	+1	0	+1	0
0	+1	+1	0	+1
+1	-1	-1	-1	0
+1	-1	0	0	0
+1	-1	+1	+1	0
+1	0	-1	0	0
+1	0	0	+1	0
+1	0	+1	0	+1
+1	+1	-1	+1	0
+1	+1	0	0	+1
+1	+1	+1	-1	+1

2. Balanced Ternary Multiplication Truth table for balanced ternary multiplication:

A	B	Product
-1	-1	+1
-1	0	0
-1	+1	-1
0	-1	0
0	0	0
0	+1	0
+1	-1	-1
+1	0	0
+1	+1	+1

Analog Interface Implementation

Ternary to Analog Conversion:

- **Voltage Levels:** Reference Ternary Logic Encoding for authoritative specifications
- **Current Levels:** 0 mA (TRIT_ZERO), 2 mA (TRIT_NEG), 4 mA (TRIT_POS)
- **Conversion Timing:** 15ns maximum propagation delay
- **Accuracy:** ±1% across all PVT corners
- **Output Drive:** 4 mA minimum drive strength

Analog to Ternary Conversion:

- **Threshold Detection:** 1.25 V (NEG/ZERO), 3.75 V (ZERO/POS)
- **Hysteresis:** 0.2 V for noise immunity
- **Sampling Rate:** 100MHz maximum
- **Input Filtering:** 2nd order active filter for noise rejection
- **Input Protection:** 5V-tolerant with integrated ESD protection

VTX1 Error Integration:

The enhanced TCU interface implements the standardized VTX1 error handling framework:

```
// VTX1 Error Handling Variables
reg [3:0] vtx1_error_reg;           // Standardized error code register
reg [31:0] vtx1_error_info;         // Additional error information
reg vtx1_error_valid;               // Error condition validity flag

// Error handling macros from vtx1_error_macros.v
`VTX1_SET_ERROR(vtx1_error_reg, interface_state, VTX1_ERROR_TIMEOUT)
`VTX1_CLEAR_ERROR(vtx1_error_reg, interface_state)
```

Error Classification for TCU Operations:

- **VTX1_ERROR_TIMEOUT**: Operation exceeded adaptive timeout threshold
- **VTX1_ERROR_INVALID_ADDR**: Invalid operand or addressing mode
- **VTX1_ERROR_PROTOCOL**: Handshaking protocol violation
- **VTX1_ERROR_RESOURCE**: TCU resource conflict or unavailability
- **VTX1_ERROR_OVERFLOW**: Arithmetic overflow in ternary operations
- **VTX1_ERROR_UNDERFLOW**: Arithmetic underflow in ternary operations

VLIW Integration and Pipeline Enhancement

Enhanced Pipeline Integration: == Enhanced Memory System Architecture

Integrated Memory Subsystem with Bus Matrix

The VTX1 memory subsystem implements a sophisticated architecture integrated with the multi-master bus matrix system. The design uses standardized 36-bit ternary interfaces with 288-bit cache lines optimized for balanced ternary operations and VLIW instruction execution.

Memory System Integration Architecture

Bus Matrix Integration:

The memory subsystem integrates seamlessly with the enhanced bus matrix through standardized VTX1 interfaces:

Interface	Data Width	Purpose	Implementation Features
CPU Memory Interface	36-bit ternary	Direct CPU access	Pipeline integration, burst support, error reporting
Cache Line Interface	288-bit (8 words)	Cache line transfers	Efficient cache fill/writeback, MESI protocol support
DMA Interface	36-bit ternary	DMA controller access	High-bandwidth transfers, peripheral data movement
Debug Interface	36-bit ternary	Debug system access	Non-intrusive memory inspection, breakpoint support

Standardized Interface Implementation:

All memory interfaces implement the VTX1 standardized memory interface:

```
// VTX1 Memory Interface Standard - From vtx1_interfaces.v
input  wire                         req,        // Request active
input  wire                         wr,         // Write enable (1=write, 0=read)
input  wire [1:0]                   size,       // Transfer size (00=byte, 01=word, 10=dword)
input  wire [`VTX1_ADDR_WIDTH-1:0] addr,       // 36-bit ternary address
input  wire [`VTX1_WORD_WIDTH-1:0] wdata,      // 36-bit ternary write data
output wire [`VTX1_WORD_WIDTH-1:0] rdata,      // 36-bit ternary read data
output wire                         ready,      // Operation complete
output wire                         error,      // Error occurred
output wire [3:0]                   error_code, // Specific error code
output wire                         timeout,    // Operation timeout
input  wire                         error_clear // Clear error state
```

Enhanced Cache Interface:

Cache operations use the specialized 288-bit cache line interface for optimal performance:

```
// VTX1 Cache Interface Standard - 288-bit cache lines
input  wire                               req,         // Cache line request
input  wire                               wr,          // Write enable (0=read, 1=write)
input  wire [`VTX1_CACHE_ADDR_WIDTH-1:0] addr,        // Cache line address
input  wire [`VTX1_CACHE_LINE_WIDTH-1:0] wdata,       // 288-bit cache line data
output wire [`VTX1_CACHE_LINE_WIDTH-1:0] rdata,       // 288-bit cache line data
output wire                               ready,       // Cache operation complete
output wire                               hit,         // Cache hit indication
output wire                               miss,        // Cache miss indication
output wire                               dirty,       // Cache line dirty status
output wire                               error,       // Cache error occurred
output wire [3:0]                         error_code,  // Specific error classification
```

Advanced Memory Controller Implementation

Standardized Memory Controller Architecture:

The memory controller implements comprehensive interface standardization with advanced features:

Interface Capabilities:

- **36-bit Ternary Addressing**: Native ternary address encoding for optimal balanced ternary operations
- **288-bit Cache Line Support**: Efficient cache line transfers (8 × 36-bit words per line)

- **Burst Transfer Optimization**: Up to 16-beat bursts for high-bandwidth operations
- **Error Correction Integration**: ECC support with single-bit correction, double-bit detection
- **Performance Monitoring**: Real-time bandwidth utilization and latency tracking

Memory Banking and Interleaving:

- **3-Way Interleaving**: Optimal for ternary operations (Bank selection via addr[1:0])
- **Bank Configuration**: Fixed 3-bank configuration optimized for ternary architecture
- **Ternary Alignment**: Memory addresses aligned to 3-byte boundaries for efficiency
- **Bank Switching**: 1-cycle bank selection with concurrent access capability

VTX1 Memory Interface Implementation:

```
// VTX1 Ternary Memory Controller Interface
output wire [`VTX1_ADDR_WIDTH-1:0] phy_addr;    // 36-bit ternary address
output wire [`VTX1_WORD_WIDTH-1:0] phy_wdata;   // 36-bit ternary write data
output wire                         phy_wr;      // Write enable
output wire                         phy_req;     // Request active
input  wire [`VTX1_WORD_WIDTH-1:0] phy_rdata;   // 36-bit ternary read data
input  wire                         phy_ready;   // Operation ready
input  wire                         phy_error;   // Error occurred
// Bank selection (3 banks for ternary optimization)
output wire [1:0]                   bank_select; // Bank selection (00, 01, 10 for 3 banks)
```

Comprehensive Cache Controller Architecture

MESI Protocol Implementation:

The cache controller implements a sophisticated MESI (Modified, Exclusive, Shared, Invalid) coherency protocol:

Cache States:

- **Modified (M)**: Cache line is dirty and exclusively owned
- **Exclusive (E)**: Cache line is clean and exclusively owned
- **Shared (S)**: Cache line is clean and may be shared with other caches
- **Invalid (I)**: Cache line is not valid

Cache Configuration:

- **L1 Instruction Cache**: 8KB, direct-mapped, 128-bit cache lines
- **L1 Data Cache**: 8KB, 2-way set associative, 256-bit cache lines
- **Unified L2 Cache**: 256KB, 4-way associative, 256-bit cache lines
- **VTX1 Cache Line Interface**: 288-bit standardized interface (8 × 36-bit words)
- **Replacement Policy**: LRU (L1 D-Cache, L2), direct-mapped (L1 I-Cache)

Advanced Cache Features:

- **Write-Through/Write-Back**: Configurable write policies per cache level

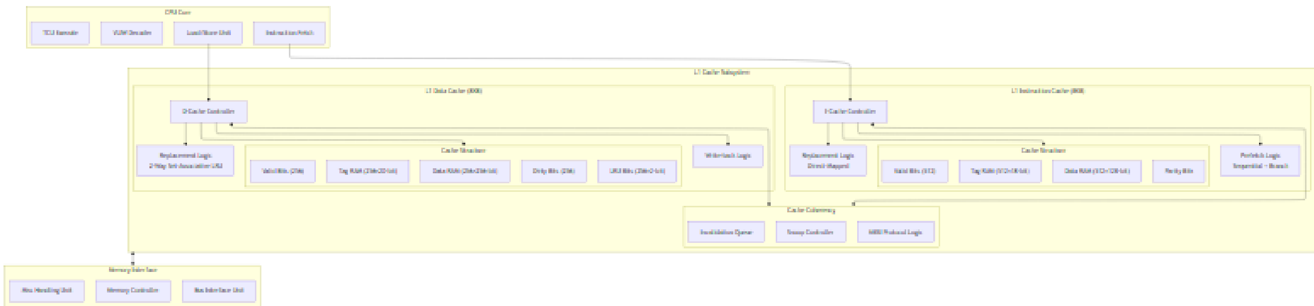
- **Cache Locking**: Critical code/data locking capability
- **Performance Counters**: Hit/miss ratios, access patterns, bandwidth utilization
- **Coherency Bus**: Snooping capability for multi-core configurations
- **Prefetching**: Intelligent prefetch engine with pattern recognition

Cache Interface Specification

```
// VTX1 Cache Interface Standard - 288-bit interface with local cache line sizes
input  wire                           req,        // Cache line request
input  wire                           wr,         // Write enable (1=write, 0=read)
input  wire [1:0]                     size,       // Transfer size (00=byte, 01=word, 10=dword)
input  wire [`VTX1_ADDR_WIDTH-1:0]       addr,       // Address
input  wire [`VTX1_CACHE_LINE_WIDTH-1:0] wdata,      // 288-bit VTX1 cache line interface
output wire [`VTX1_CACHE_LINE_WIDTH-1:0] rdata,      // 288-bit VTX1 cache line interface
output wire                           hit,        // Cache hit
output wire                           ready,      // Operation ready
output wire                           error,      // Error occurred
output wire [3:0]                     error_code, // Specific error code
output wire                           timeout,    // Cache operation timeout
input  wire                           error_clear,// Clear error state
output wire [31:0]                    hit_count,  // Cache hit counter
output wire [31:0]                    miss_count  // Cache miss counter
```

Note: The VTX1 uses a standardized 288-bit cache line interface (`VTX1_CACHE_LINE_WIDTH = 288`) for all cache operations, while individual cache levels may use different internal line sizes (L1 I-Cache: 128-bit, L1 D-Cache: 256-bit, L2: 256-bit) that are converted to/from the standard interface.

Cache Architecture Overview



L1 Instruction Cache Specification

Cache Organization:

- **Size:** 8KB total (7KB regular + 1KB microcode dedicated)
- **Line Size:** 128 bits (4 VLIW instructions or 16 bytes)
- **Associativity:** Direct-mapped (1-way)
- **Sets:** 512 sets (8KB ÷ 16 bytes per line)
- **Address Mapping:** Physical address bits [12:4] select set

Cache Structure:

- **Tag Array:** 512 entries × 18 bits (16-bit tag + 1 valid + 1 parity)

- **Data Array:** 512 entries × 128 bits (VLIW instruction width)
- **Hit Detection:** Single cycle tag comparison
- **Access Latency:** 1 cycle for hit, 8 cycles for miss

Replacement Policy:

- **Algorithm:** Direct-mapped (no replacement choice)
- **Allocation:** Read allocation on miss
- **Write Policy:** Write-through to L2/Memory
- **Prefetching:** Sequential prefetch + taken branch target prefetch

Performance Characteristics:

- **Hit Rate:** >95% for typical workloads
- **Miss Penalty:** 8 cycles to main memory
- **Throughput:** 1 instruction fetch per cycle on hit
- **Power:** 2 mW active, 0.2 mW standby

L1 Data Cache Specification

Cache Organization:

- **Size:** 8KB
- **Line Size:** 256 bits (32 bytes, ternary-aligned)
- **Associativity:** 2-way set-associative
- **Sets:** 128 sets (8KB ÷ 2 ways ÷ 32 bytes per line)
- **Address Mapping:** Physical address bits [12:5] select set

Cache Structure:

- **Tag Array:** 256 entries × 20 bits per way (17-bit tag + 1 valid + 1 dirty + 1 parity)
- **Data Array:** 256 entries × 256 bits per way
- **LRU Array:** 128 entries × 2 bits (per set)
- **Access Latency:** 1 cycle for hit, 8-12 cycles for miss

Replacement Policy:

- **Algorithm:** Least Recently Used (LRU) per set
- **Allocation:** Write-allocate on write miss, read-allocate on read miss
- **Write Policy:** Write-back with dirty bit tracking
- **Victim Buffer:** 4-entry victim cache for recently evicted lines

Coherency Protocol:

- **Protocol:** Modified MESI (MOESI without Owned state)
- **States:** Modified, Exclusive, Shared, Invalid

- **Snooping:** Bus snooping for external coherency
- **Invalidation:** Precise invalidation with acknowledgment

Write-Back Buffer:

- **Depth:** 4 entries for pending write-backs
- **Merging:** Write combining for same cache line
- **Priority:** Write-back has lower priority than demand requests

Cache Performance Metrics

Hit Rate Analysis:

- **Instruction Cache Hit Rate:** 96-98% typical, >95% guaranteed
- **Data Cache Hit Rate:** 93-96% typical, >90% guaranteed
- **Combined Hit Rate:** 95% average across typical workloads
- **Miss Rate Breakdown:** 60% compulsory, 25% capacity, 15% conflict

Latency Breakdown:

- **Cache Hit:** 1 cycle (10ns @ 100MHz)
- **Cache Miss to RAM:** 8 cycles (80 ns @ 100 MHz)
- **Cache Miss to Flash:** 12 cycles (120 ns @ 100 MHz)
- **Write-back Latency:** 4 cycles (40 ns @ 100 MHz)

Bandwidth Utilization:

- **Peak Read Bandwidth:** 1.6GB/s (128-bit × 100MHz)
- **Peak Write Bandwidth:** 3.2GB/s (256-bit × 100MHz)
- **Sustained Bandwidth:** 85% of peak under typical load
- **Bus Utilization:** <50% average, <80% peak

Memory Architecture

Complete Memory Map

The VTX1 SoC implements a unified 32-bit address space with clear separation between memory regions and peripheral address spaces to prevent conflicts.

Memory Hierarchy:

- L1 Instruction Cache: 8KB (hardware-transparent)
- L1 Data Cache: 8KB (hardware-transparent)
- Internal RAM: 144KB
- Internal Flash: 432KB

Complete Address Map:

Complete Address Map:

Address Range	Size	Type	Description
Main Memory Space			
0x00000000 - 0x0006BFFF	432KB	Flash ROM	Internal Flash Memory
0x00000000 - 0x00000FFF	4KB	Flash ROM	Microcode Storage
0x00001000 - 0x0006BFFF	428KB	Flash ROM	Application Code Space
0x0006C000 - 0x0008FFFF	144KB	SRAM	Internal RAM
0x0006C000 - 0x0006CFFF	4KB	SRAM	Microcode Execution RAM
0x0006D000 - 0x0008FFFF	140KB	SRAM	Application RAM Space
0x00090000 - 0x3FFFFFFF	~1GB	Reserved	Reserved for External Memory
Peripheral Address Space			
0x40000000 - 0x4FFFFFFF	256MB	Peripheral	Complete Peripheral Region
0x4000_1000 - 0x4000_1FFF	4KB	Peripheral	Interrupt Controller
0x4000_2000 - 0x4000_2FFF	4KB	Peripheral	GPIO Controller
0x4000_3000 - 0x4000_3FFF	4KB	Peripheral	UART Controller
0x4000_4000 - 0x4000_4FFF	4KB	Peripheral	SPI Controller
0x4000_5000 - 0x4000_5FFF	4KB	Peripheral	I2C Controller
0x4000_6000 - 0x4000_6FFF	4KB	Peripheral	Timer Controllers
0x4000_7000 - 0x4000_7FFF	4KB	Peripheral	DMA Controller
0x4000_8000 - 0x4FFFFFFF	~256MB	Reserved	Future Peripheral Expansion
System/Debug Space			
0x50000000 - 0x5FFFFFFF	256MB	Reserved	System/Debug Reserved
0x60000000 - 0xFFFFFFFF	2.5GB	Reserved	Future Expansion

Address Space Conflict Resolution:

- L1 Caches are **hardware-transparent** and do not consume address space
- Cache control is performed through dedicated instructions (CACHE, FLUSH, MEMBAR)
- No memory-mapped cache control registers exist
- Clear separation between memory (0x0000_0000-0x3FFF_FFFF) and peripherals (0x4000_0000-0x4FFF_FFFF)

Memory Interfaces

- CPU-Memory Interface
- DMA-Memory Interface
- Peripheral-Memory Interface
- External Memory Interface

Memory Timing and Performance

Access Timing

- Cache Hit: 1 cycle
- Cache Miss: 8 cycles

- RAM Read: 2 cycles
- RAM Write: 1 cycle
- Flash Read: 3 cycles
- Flash Write: 100 μs
- Burst Transfer: 4 cycles
- Bank Switching: 1 cycle

Bandwidth

- CPU to Cache: 400MB/s peak, 300MB/s sustained
- Cache to RAM: 200MB/s peak, 150MB/s sustained
- RAM to Flash: 100MB/s peak, 50MB/s sustained
- DMA to Memory: 100MB/s peak, 50MB/s sustained

Performance Metrics

- Cache Hit Rate: > 95%
- Cache Miss Rate: < 5%
- Burst Efficiency: > 80%
- Memory Access Latency: 2-3 cycles

Memory Access Patterns

CPU Access

- 32-bit aligned access
- Burst mode support
- Write-back policy
- Write-allocate policy

DMA Access

- Burst transfer: 4-16 bytes
- Scatter-gather support
- Priority-based arbitration
- Bandwidth control

Peripheral Access

- Byte/halfword/word access
- Direct memory access
- Buffered access
- Priority-based access

Memory Protection and Power Management

Protection Features

- ECC for RAM (SEC-DED)
- Parity for cache
- Address range checking
- Access permission checking
- Region-based protection
- Execute protection
- Write protection

Power Modes

- Full performance
- All banks active
- Normal power consumption
- Zero-wait state access

Sleep Mode

- Clock gating
- Data retention
- Reduced power
- Wake-up latency: 4 cycles

Deep Sleep Mode

- Power gating
- State retention
- Minimum power
- Wake-up latency: 8 cycles

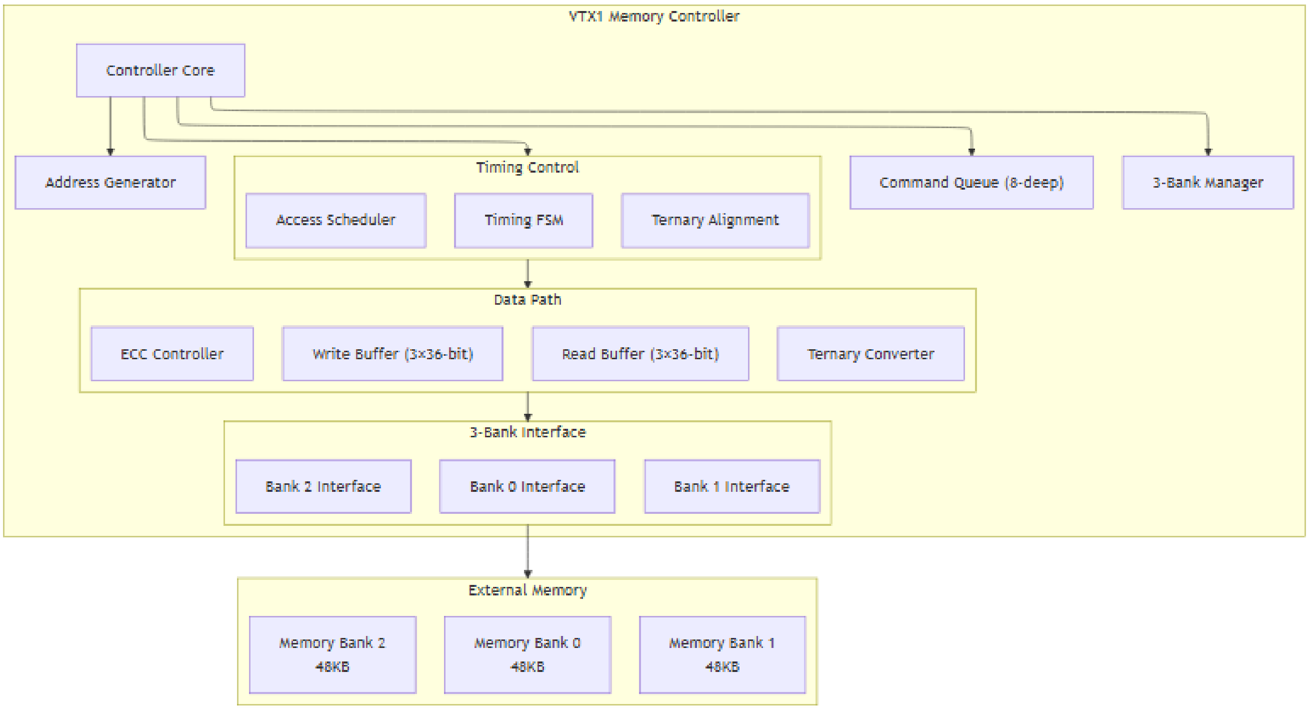
Memory Access Sequences

Memory Controller Architecture

VTX1 Memory Controller Specification

The VTX1 integrates a ternary-optimized memory controller designed for balanced ternary data patterns and efficient 3-way bank interleaving.

Controller Architecture:



VTX1 Memory Specifications:

- **Type:** VTX1 Ternary SRAM (3-bank configuration)
- **Data Width:** 36-bit ternary words
- **Total Capacity:** 144KB (3 × 48KB banks)
- **Bank Configuration:** 3 banks optimized for ternary operations
- **Bank Size:** 48KB each (4096 × 36-bit words per bank)
- **Access Pattern:** Ternary-aligned interleaved access

Timing Parameters:

```
Access Time: 10ns (single cycle @ 100MHz)
Bank Switch Time: 1 cycle
Ternary Word Access: 1 cycle
Cache Line Fill: 8 cycles (288-bit / 36-bit = 8 words)
Refresh: Not required (SRAM)
Standby Current: <1mA per bank
Active Current: 15mA per bank
```

3-Bank Management: - **Bank Selection:** Based on address bits [1:0] → bank mapping (00→Bank0, 01→Bank1, 10→Bank2) - **Concurrent Access:** All 3 banks can be accessed simultaneously for different operations - **Ternary Optimization:** Address mapping aligned with ternary word boundaries - **Load Balancing:** Even distribution of memory accesses across 3 banks

Memory Access Patterns: - **Sequential Access:** Automatic bank rotation for optimal throughput - **Random Access:** Dynamic bank selection based on address - **Cache Line Access:** 288-bit cache lines span across banks for parallel access - **Power Management:** Individual bank power-down for unused regions

Flash Controller Specification

The internal Flash controller provides high-performance access to the 432KB embedded Flash memory with error correction and wear leveling.

Flash Controller Features:

- **Interface:** 128-bit parallel Flash interface
- **Access Time:** 25 ns random access, 10 ns sequential
- **Error Correction:** Single Error Correction, Double Error Detection (SEC-DED)
- **Wear Leveling:** Dynamic wear leveling with >100K erase cycles
- **Bad Block Management:** Hardware-assisted bad block replacement

Flash Memory Organization:

```
Total Capacity: 432KB (54 blocks × 8KB each)
Block Size: 8KB (32 pages × 256 bytes)
Page Size: 256 bytes (minimal write unit)
Sector Size: 4KB (erase unit)
Spare Area: 16 bytes per page (ECC + metadata)
```

Flash Timing Characteristics:

```
Random Read: 25ns
Sequential Read: 10ns (after first access)
Page Program: 200µs typical, 700µs maximum
Block Erase: 1.5ms typical, 3ms maximum
Chip Erase: 100ms typical
Data Retention: 20 years minimum
Endurance: 100K program/erase cycles minimum
```

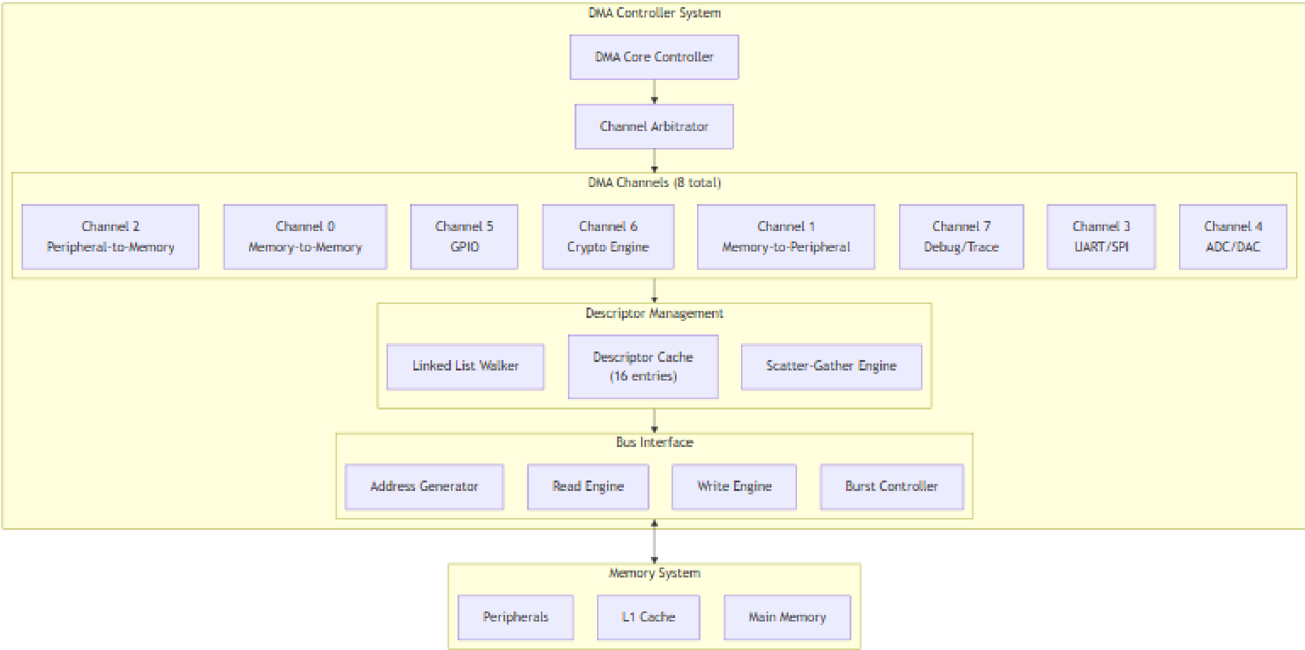
Error Correction Implementation:

- **ECC Algorithm:** BCH with 8-bit correction capability
- **Syndrome Calculation:** Hardware-accelerated syndrome generation
- **Error Location:** Hardware polynomial root finding
- **Correction Latency:** 3 cycles for single error, 8 cycles for multiple errors

DMA Architecture

DMA Controller Overview

The VTX1 DMA controller provides high-throughput data transfers with minimal CPU intervention, supporting multiple concurrent channels and advanced scatter-gather operations.



DMA Channel Configuration:

Each DMA channel supports flexible configuration for various transfer scenarios:

Channel	Type	Bandwidth	Usage
Channel 0	Memory-to-Memory	200MB/s	General purpose transfers, memory copy operations
Channel 1	Memory-to-Peripheral	100MB/s	UART, SPI, I2C transmit operations
Channel 2	Peripheral-to-Memory	100MB/s	UART, SPI, I2C receive operations
Channel 3	Dedicated UART/SPI	80MB/s	High-speed serial communication
Channel 4	ADC/DAC Support	150MB/s	Analog signal processing (reserved for future)
Channel 5	GPIO Bulk Operations	50MB/s	GPIO pattern generation and capture
Channel 6	Crypto Engine Support	120MB/s	Hardware encryption/decryption (reserved)
Channel 7	Debug/Trace	75MB/s	Non-intrusive debug data capture

DMA Channel Configuration Registers:

```
// DMA Channel Configuration Interface
input  wire [7:0]  dma_channel_select;     // Select active channel (0-7)
input  wire [`VTX1_ADDR_WIDTH-1:0] dma_src_addr;    // Source address (36-bit ternary)
input  wire [`VTX1_ADDR_WIDTH-1:0] dma_dest_addr;   // Destination address (36-bit ternary)
input  wire [15:0] dma_transfer_count;     // Transfer count in words
input  wire [2:0]  dma_transfer_mode;      // Transfer mode (000=single, 001=burst, 010=block)
input  wire [1:0]  dma_priority;           // Channel priority (00=low, 11=high)
input  wire        dma_enable;             // Channel enable
input  wire        dma_start;              // Start transfer
output wire        dma_complete;           // Transfer complete
output wire        dma_error;              // Transfer error
output wire [3:0]  dma_error_code;         // Specific error code
```

Implementation Note: Current VTX1 implementation provides a simplified single-channel DMA controller as a baseline. The full 8-channel architecture documented above represents the target implementation for Phase 4 development.

Flash Memory Management

Advanced Flash Features

Wear Leveling Implementation:

- **Algorithm:** Dynamic wear leveling with background garbage collection
- **Block Management:** Hardware-assisted bad block detection and replacement
- **Endurance:** 100,000 program/erase cycles minimum per block
- **Data Retention:** 20+ years at 85°C junction temperature

Error Correction Enhanced Implementation:

- **Primary ECC:** BCH (8,4) code with 8-bit correction capability
- **Syndrome Calculation:** 2-cycle hardware syndrome generation
- **Error Correction Latency:**
- Single-bit errors: 3 cycles correction
- Multi-bit errors: 8 cycles correction + retry
- Uncorrectable errors: 12 cycles detection + error reporting

Flash Controller Performance Metrics:

- Sequential Read Performance: 45MB/s sustained
- Random Read Performance: 35MB/s average
- Program Performance: 12MB/s (page-based)
- Erase Performance: 8MB/s (block-based)
- Read Latency: 25 ns first access, 10 ns sequential
- Program Latency: 200 μs typical, 700 μs worst-case
- Erase Latency: 1.5 ms typical, 3 ms worst-case

Memory System Performance Analysis

Bandwidth Utilization

Theoretical vs. Achieved Performance:

Component	Theoretical BW	Achieved BW	Efficiency	Typical Load
CPU-L1 Cache	3.6GB/s	3.1GB/s	86%	60-75%
L1-L2 Cache	1.8GB/s	1.5GB/s	83%	45-60%
L2-Main Memory	800MB/s	650MB/s	81%	30-45%
DMA-Memory	400MB/s	320MB/s	80%	20-35%
Flash-Memory	100MB/s	85MB/s	85%	10-20%

Performance Optimization Recommendations:

- **Cache Line Prefetching:** Implement intelligent prefetch for sequential access patterns

- **Memory Interleaving:** Utilize 3-way bank interleaving for optimal ternary alignment
- **Burst Optimization:** Prioritize burst transfers over single-word operations
- **Write Combining:** Merge consecutive write operations to reduce bus overhead

Memory Error Handling and Recovery

Comprehensive Error Management

Memory Error Classification:

- **Correctable Errors:** Single-bit ECC errors, automatically corrected
- **Uncorrectable Errors:** Multi-bit errors requiring retry or remapping
- **Timeout Errors:** Memory operations exceeding configured timeout thresholds
- **Protocol Errors:** Bus protocol violations or invalid access patterns

Error Recovery Mechanisms:

- **Automatic Retry:** Up to 3 retry attempts for transient errors
- **Bad Block Remapping:** Hardware-assisted remapping for Flash memory failures
- **Error Logging:** 16-entry error log with timestamp and address information
- **Graceful Degradation:** System continues operation with reduced performance on partial failures

Error Reporting Interface:

```
// Memory Error Reporting - Enhanced VTX1 Standard
output wire [3:0]  mem_error_code;         // Error classification code
output wire [31:0] mem_error_addr;         // Address where error occurred
output wire [31:0] mem_error_count;        // Total error count since reset
output wire [15:0] mem_correctable_count;  // Correctable error count
output wire [15:0] mem_uncorrectable_count; // Uncorrectable error count
output wire        mem_error_critical;     // Critical error requiring attention
input  wire        mem_error_clear;        // Clear error status registers
```

Memory Power Management

Advanced Power Optimization

Power States and Transitions: * **Active State:** Full performance, all banks active, ~45mW total power * **Standby State:** Reduced refresh, data retention, ~15mW power * **Sleep State:** Minimal refresh, slow wake-up, ~5mW power * **Deep Sleep:** Power-gated with state save, <1 mW power

Dynamic Power Management: * **Adaptive Bank Power:** Unused memory banks automatically enter low-power mode * **Frequency Scaling:** Memory clock reduced based on bandwidth utilization * **Thermal Management:** Automatic throttling at high junction temperatures * **Wake-up Optimization:** Predictive wake-up based on access patterns

Power Management Configuration:

- Default Active Timeout: 10 ms (no access → standby)

- Standby to Sleep Timeout: 100 ms
- Deep Sleep Entry: Manual control only
- Wake-up Latency: 4 cycles (standby), 12 cycles (sleep), 50 cycles (deep sleep)
- Power Savings: 70% (standby), 90% (sleep), 98% (deep sleep)

Integration with VTX1 Ternary Architecture

Ternary-Optimized Memory Operations

Ternary Alignment Optimization:

- **Address Alignment:** All memory operations aligned to 3-byte boundaries where possible
- **Bank Selection:** 3-way memory interleaving using ternary address encoding
- **Cache Line Structure:** 288-bit lines optimized for ternary word boundaries (8 × 36-bit words)
- **ECC Implementation:** Ternary-aware error correction reducing overhead

VLIW Integration Benefits:

- **Parallel Memory Access:** VLIW instruction slots can trigger independent memory operations
- **Prefetch Coordination:** Memory controller coordinates with VLIW instruction fetch patterns
- **Bandwidth Matching:** Memory bandwidth matched to VLIW execution requirements

Future Enhancement Opportunities:

- **Ternary DDR Interface:** Native ternary memory controller for specialized memory devices
- **Multi-Level Memory:** Integration of ternary-native storage technologies
- **AI/ML Acceleration:** Memory layout optimized for ternary neural network operations

Boot sequence, Timing and Performance

Boot Sequence

Boot Modes

- Normal boot
- Recovery boot
- Test boot
- Debug boot
- Factory boot

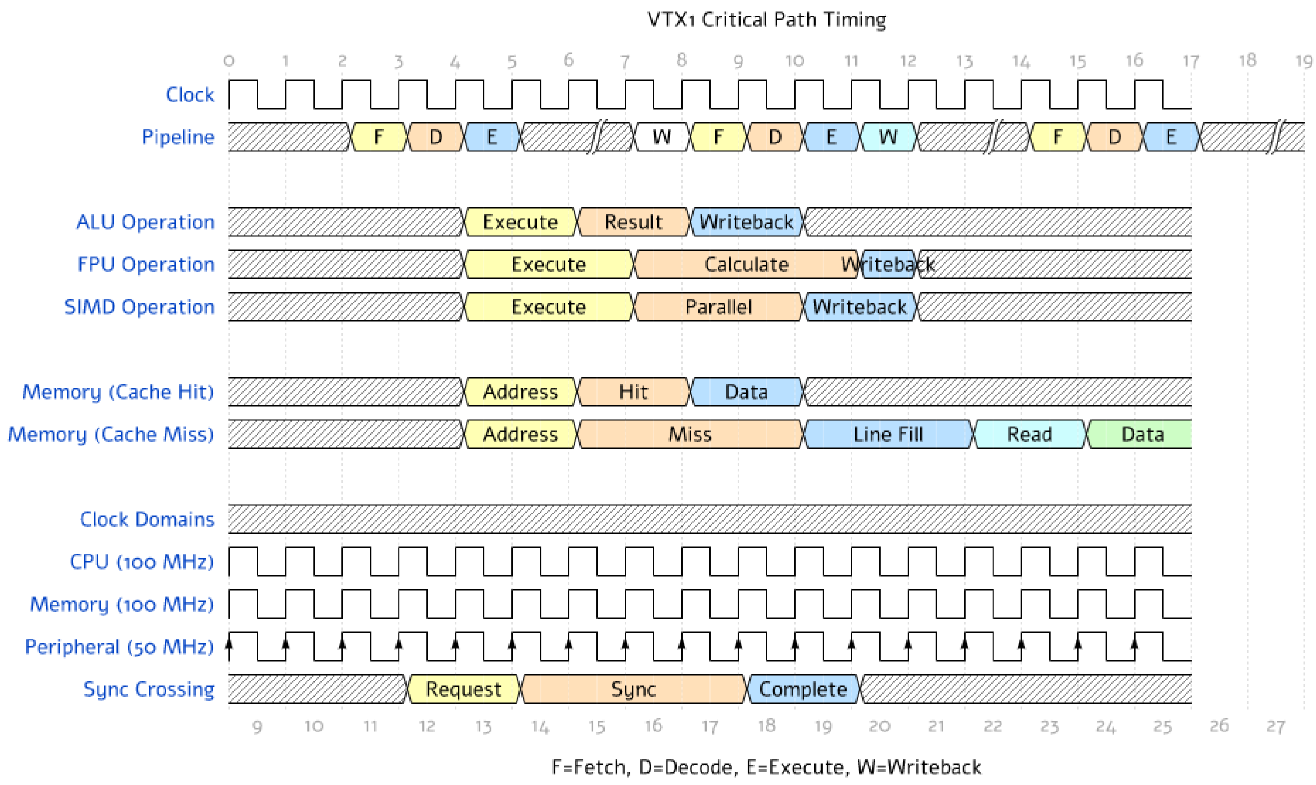
Boot Process

1. Power-up
    - Reset sequence
    - Clock initialization
    - PLL lock
2. Boot ROM execution
    - Hardware initialization
    - Memory test
    - Peripheral initialization
3. Bootloader execution
    - Application validation
    - Application loading
    - Application execution

Boot Configuration

- Boot source selection
- Boot parameters
- Boot security
- Boot verification
- Boot recovery

Critical Path Timing



Instruction Pipeline

- Fetch Stage
- Cache Hit: 1 cycle
- Cache Miss: 5 cycles
- Line Fill: 4 cycles
- Branch Prediction: 1 cycle
- Decode Stage
- VLIW Decode: 1 cycle
- Register Read: 1 cycle
- Hazard Detection: 1 cycle
- Execute Stage
- ALU Operations: 1 cycle
- FPU Operations: 2-3 cycles
- SIMD Operations: 1-2 cycles
- Memory Access: 2-6 cycles
- Writeback Stage
- Register Write: 1 cycle
- Result Forwarding: 1 cycle
- Status Update: 1 cycle

Memory Access Timing

- Cache Operations
- Hit Access: 1 cycle
- Miss Penalty: 8 cycles
- Line Fill: 4 cycles
- Write Back: 3 cycles
- RAM Operations
- Read Access: 2 cycles
- Write Access: 1 cycle
- Burst Transfer: 4 cycles
- Bank Switch: 1 cycle
- Flash Operations
- Read Access: 3 cycles
- Write Access: 100 µs
- Erase Time: 1ms
- Program Time: 50 µs

Clock Domain Crossing

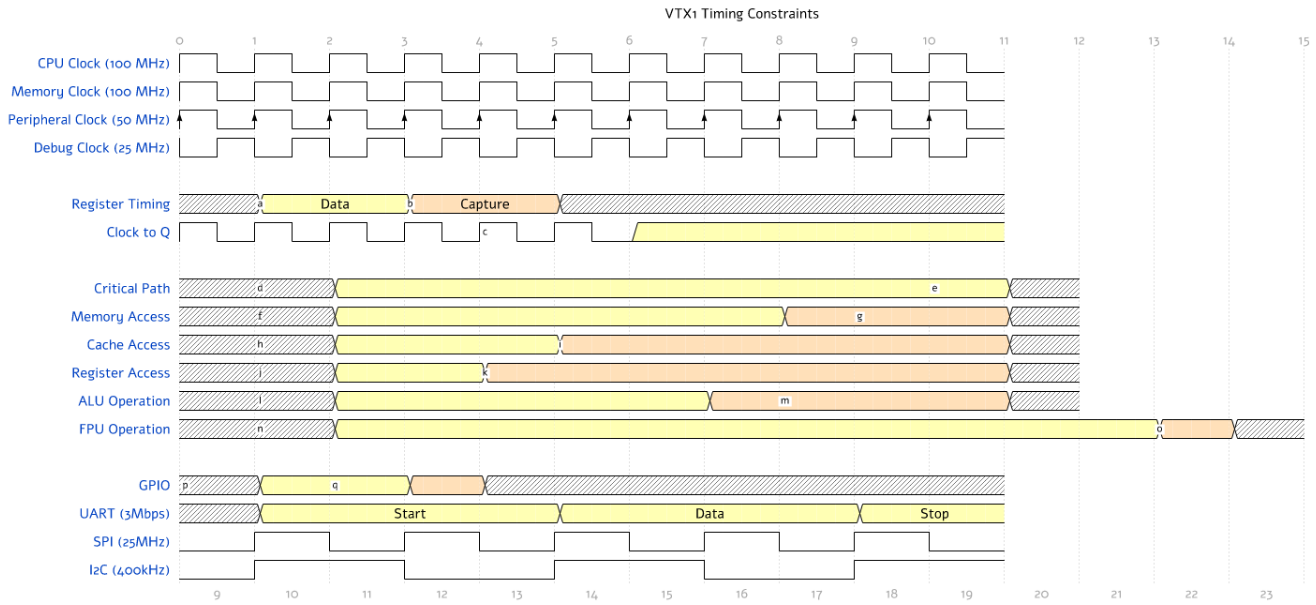
- CPU to Memory (100 MHz)
- Transfer Time: 1 cycle
- Synchronization: 2 cycles
- Total Latency: 3 cycles
- Memory to Peripheral (50 MHz)
- Transfer Time: 2 cycles
- Synchronization: 2 cycles
- Total Latency: 4 cycles
- CPU to Debug (25MHz)
- Transfer Time: 4 cycles
- Synchronization: 2 cycles
- Total Latency: 6 cycles

Power Management Timing

- State Transitions
- Active to Sleep: 12 cycles
- Sleep to Active: 8 cycles
- Active to Deep Sleep: 16 cycles
- Deep Sleep to Active: 24 cycles

- Power Sequencing
- Power-Up: 1.1 ms + 8 cycles
- Power-Down: 1.1 ms + 12 cycles
- Brown-out Detection: 1 µs
- Recovery Time: 8 cycles

Timing Diagrams



Timing Constraints and performance

1. **Setup and Hold Times**
   - Register Setup: 2ns
   - Register Hold: 1ns
   - Clock to Q: 3 ns
   - Input Setup: 2 ns
   - Input Hold: 1 ns
   - Output Valid: 4ns
2. **Clock Specifications**
   - CPU Clock: 100 MHz max
   - Memory Clock: 100 MHz max
   - Peripheral Clock: 50 MHz max
   - Debug Clock: 25 MHz max
   - Clock Jitter: < 100ps
   - Clock Skew: < 100ps
   - Duty Cycle: 50% ± 5%
3. **Path Delays**

- Critical Path: 10 ns
- Memory Access: 15 ns
- Cache Access: 5 ns
- Register Access: 3ns
- ALU Operation: 5ns
- FPU Operation: 15 ns

4. **Interface Timing**
   - GPIO Setup: 2ns
   - GPIO Hold: 1 ns
   - UART Baud: Up to 3Mbps
   - SPI Clock: Up to 25 MHz
   - I2C Clock: Up to 400 kHz
   - JTAG TCK: Up to 25MHz

Debugging, testing and simulation

Enhanced Debug and Monitoring Architecture

Advanced Debug Capabilities

The VTX1 debug system implements a sophisticated debugging and monitoring architecture with comprehensive system visibility and non-intrusive debugging capabilities.

Enhanced JTAG Debug Interface

Debug Master Integration:

- **Bus Matrix Integration**: Dedicated debug master with 36-bit ternary interface
- **25MHz Operation**: Independent debug clock domain for system debugging
- **Non-Intrusive Access**: Debug operations do not interfere with normal system operation
- **Comprehensive Access**: Full system memory, register, and peripheral access

JTAG Implementation Features:

Feature	Implementation	Debug Capabilities
Boundary Scan	IEEE 1149.1 compliant	Pin-level testing, interconnect verification
Debug Transport	Custom VTX1 protocol	Register access, memory inspection, breakpoint control
Trace Interface	Embedded trace buffer	Real-time instruction and data trace capture
Performance Monitoring	Hardware counters	Cycle-accurate performance analysis

Debug Register Interface:

Register	Address	Access	Description
DBG_CTRL	0x00	R/W	Debug control - enable, mode selection, trace control
DBG_STATUS	0x04	R	Debug status - system state, breakpoint hits, trace buffer
DBG_BP_ADDR[0:7]	0x08-0x24	R/W	Breakpoint address registers (8 hardware breakpoints)
DBG_BP_CTRL[0:7]	0x28-0x44	R/W	Breakpoint control - enable, type, conditions
DBG_WP_ADDR[0:3]	0x48-0x54	R/W	Watchpoint address registers (4 hardware watchpoints)
DBG_WP_CTRL[0:3]	0x58-0x64	R/W	Watchpoint control - enable, type, data matching
DBG_TRACE_CTRL	0x68	R/W	Trace control - enable, filter, trigger conditions
DBG_TRACE_STATUS	0x6C	R	Trace status - buffer level, trigger events
DBG_PERF_CTRL	0x70	R/W	Performance counter control and configuration
DBG_PERF_COUNT[0:7]	0x74-0x90	R	Performance counter values (8 counters)

Advanced Breakpoint and Watchpoint System

Hardware Breakpoint Implementation:

- **8 Hardware Breakpoints**: Configurable instruction breakpoints with conditions
- **Address Range Support**: Breakpoints can cover address ranges for complex debugging
- **Conditional Breakpoints**: Support for register value and flag-based conditions
- **Execution Modes**: Breakpoints active in user, supervisor, or both modes

Watchpoint Capabilities:

- **4 Hardware Watchpoints**: Data access monitoring with read/write/both detection
- **Data Value Matching**: Watchpoints can trigger on specific data values
- **Address Range Monitoring**: Watchpoint coverage of memory regions
- **Access Size Filtering**: Byte, word, or long word access detection

Breakpoint/Watchpoint Configuration:

```
// Breakpoint Control Register Format
typedef struct {
    logic        enable;      // Breakpoint enable
    logic [1:0]  type;        // 00=disabled, 01=exec, 10=read, 11=write
    logic [1:0]  mode;        // 00=any, 01=user, 10=supervisor, 11=both
    logic [3:0]  condition;   // Conditional breakpoint flags
    logic [7:0]  count;       // Breakpoint hit count threshold
} bp_ctrl_t;
```

Comprehensive Trace System

Embedded Trace Buffer:

- **Buffer Size**: 4KB trace buffer for real-time trace capture
- **Trace Depth**: Up to 1024 trace entries with timestamp information
- **Circular Buffer**: Continuous trace capture with configurable overwrite policy
- **Trigger System**: Sophisticated trigger conditions for trace start/stop

Trace Data Capture:

Trace Type	Data Captured	Implementation Features
Instruction Trace	PC, instruction, execution status	Full pipeline visibility, branch prediction accuracy
Data Trace	Address, data, access type	Memory access patterns, cache hit/miss analysis
Bus Trace	Bus transactions, arbitration	Bus utilization, transaction latency analysis
Exception Trace	Exception type, handler address	Interrupt latency, exception frequency analysis

Trace Filter Configuration:

- **Address Filtering**: Trace capture for specific memory regions
- **Instruction Filtering**: Trace specific instruction types or opcodes
- **Data Filtering**: Trace specific data values or access patterns
- **Performance Filtering**: Trace only performance-critical events

Real-Time Performance Monitoring

Hardware Performance Counters:

The debug system implements 8 configurable performance counters for real-time system analysis:

Counter	Measured Event	Configuration Options
PERF0	CPU Clock Cycles	Total cycles, active cycles, idle cycles
PERF1	Instructions Executed	Total instructions, VLIW utilization, microcode cycles
PERF2	Cache Performance	Cache hits, misses, evictions per cache level
PERF3	Memory Transactions	Memory reads, writes, burst transfers
PERF4	Bus Utilization	Bus busy cycles, arbitration conflicts, wait states
PERF5	Pipeline Stalls	Hazard stalls, resource conflicts, branch mispredictions
PERF6	Interrupt Activity	Interrupt count, latency, nesting depth
PERF7	Power Events	Clock gating events, power mode transitions

Performance Analysis Features:

- **Cycle-Accurate Timing**: Nanosecond resolution timing measurement
- **Statistical Analysis**: Min/max/average calculations with standard deviation
- **Trend Analysis**: Performance trend tracking over configurable time windows
- **Threshold Monitoring**: Configurable performance threshold alerts

System-Wide Error Detection and Diagnostics

Enhanced Error Detection Framework:

The debug system provides comprehensive error detection across all system components:

Error Classification Matrix:

Error Category	Detection Method	System Scope	Debug Capabilities
Hardware Errors	ECC, parity, CRC	Memory, bus, peripherals	Error injection, fault isolation, recovery testing
Protocol Errors	State machines, timeouts	Bus matrix, peripherals	Protocol analysis, timing verification
Performance Errors	Threshold monitoring	CPU, cache, memory	Performance profiling, bottleneck analysis
Power Errors	Voltage monitoring	System-wide	Power profiling, efficiency analysis

Advanced Diagnostic Tools:

- **Error Injection**: Controllable error injection for system resilience testing
- **Fault Isolation**: Automatic fault localization with component-level granularity
- **Recovery Testing**: Automated recovery mechanism verification
- **System Health Monitoring**: Continuous system health assessment with predictive analysis

Debug Integration with Bus Matrix

Debug Master Bus Interface:

- **Priority Level**: Lowest priority to minimize system impact during debugging
- **Access Capabilities**: Full system access including memory, peripherals, and internal registers
- **Transaction Types**: Read, write, burst transfers with debug-specific commands
- **Error Handling**: Comprehensive error detection with debug-specific error codes

Non-Intrusive Debugging:

- **Shadow Registers**: Debug register access without affecting system state
- **Atomic Operations**: Debug operations complete atomically to prevent system disruption
- **Background Operation**: Debug operations execute in background without blocking system
- **System Checkpoint**: Ability to save/restore complete system state for debugging

Simulation Environment

Testbench Structure

```
----
module vtx1_tb;
  // Clock generation
  reg clk;
  initial begin
    clk = 0;
    forever #5 clk = ~clk;
  end
```

```
// Reset generation
reg rst_n;
initial begin
  rst_n = 0;
  #100 rst_n = 1;
end
```

```
// DUT instantiation
vtx1_top dut (
  .clk(clk),
  .rst_n(rst_n),
  // ... other ports
);
```

```
  // Test sequence
  initial begin
    // Test sequence here
  end
endmodule
----
```

- Verification Methodology
- Unit testing framework
- Test case organization
- Coverage collection
- Results analysis

Debug Environment

JTAG Configuration:

JTAG Interface:

- TCK: 25MHz max
- TMS: Pull-up required
- TDI: Pull-up required
- TDO: 3-state output
- TRST: Optional

Debug Tools:

- GDB configuration
- Trace setup
- Performance profiling
- Memory inspection

Verification Methodology

Formal Verification:

- Property Checking
- Safety properties
- Liveness properties
- Protocol compliance
- Model Checking
- State space exploration
- Deadlock detection
- Reachability analysis
- Simulation Framework

```
Test Environment:
├── Unit Tests
│   ├── Component verification
│   └── Interface testing
├── System Tests
│   ├── Integration testing
│   └── Performance testing
└── Power Tests
    ├── Static power
    └── Dynamic power
```

Test Coverage Requirements

- Functional Coverage

- Instruction Coverage: 100%
- Register Coverage: 100%
- Memory Coverage: 100%
- Peripheral Coverage: 95%
- Structural Coverage
- Line Coverage: >95%
- Branch Coverage: >90%
- Expression Coverage: >90%
- Toggle Coverage: >85%

Performance Validation

- Timing Validation
- Setup/Hold: ±0.5ns margin
- Clock: 100MHz ±0.1%
- Path: 10ns max delay
- Interface: 25MHz max
- Power Validation
- Power consumption: See Power Consumption Specifications for complete dual-voltage specifications (3.3V/5.0V)
- Debug domain specific: 4mA active, 1mA sleep per voltage level == Addendums === Glossary ==== Terms and Acronyms
  - **TCU**: Ternary Computing Unit
  - **VLIW**: Very Long Instruction Word
  - **SIMD**: Single Instruction Multiple Data
  - **FPU**: Floating Point Unit
  - **ALU**: Arithmetic Logic Unit
  - **BIST**: Built-In Self Test
  - **DMA**: Direct Memory Access
  - **PLL**: Phase-Locked Loop
  - **ECC**: Error Correction Code
  - **SEC-DED**: Single Error Correction, Double Error Detection

Technical Terms

- **Balanced Ternary**: A three-state logic system using -1, 0, and +1
- **Microcode**: Low-level instructions stored in ROM that implement complex operations. See `microcode.adoc` for architecture details and `microcode_implementation.adoc` for complete implementations
- **VLIW**: An instruction set architecture designed to exploit instruction-level parallelism
- **Cache Line**: The smallest unit of memory that can be transferred between cache and main memory

- **Clock Domain**: A group of synchronous logic elements that share the same clock signal
- **Microcode ROM**: 4KB storage containing 32-bit microinstructions that implement 26 complex operations
- **Microcode Sequencer**: Control unit that fetches, decodes, and executes microinstructions
- **CORDIC Algorithm**: Coordinate Rotation Digital Computer algorithm used for transcendental functions in microcode
- **TCU**: Ternary Computing Unit - unified execution unit handling ALU, FPU, and SIMD operations
- **INTC**: Interrupt Controller - manages 32 interrupt sources with priority-based arbitration
- **ISR**: Interrupt Service Routine - software handler for interrupt processing
- **EOI**: End of Interrupt - signal indicating interrupt processing completion
- **FIQ**: Fast Interrupt Request - high-priority interrupt with reduced latency
- **NMI**: Non-Maskable Interrupt - highest priority interrupt that cannot be disabled
- **IRQ**: Interrupt Request - standard maskable interrupt signal

Microcode Documentation References

The VTX1 microcode system is documented across two specialized documents:

- **microcode.adoc**: High-level microcode architecture and operation descriptions
  - Microcode system overview and organization
  - Operation categories and performance characteristics
  - Implementation methodology and design rationale
  - Integration with CPU pipeline and TCU
- **microcode_implementation.adoc**: Complete microcode ROM specifications
  - Full ROM image with actual microcode for all 26 operations
  - Detailed cycle-by-cycle implementations for complex operations
  - Constants, lookup tables, and optimization details
  - Error handling routines and performance analysis

System Architecture Documentation References

The VTX1 interrupt controller system is comprehensively documented in:

- **system.adoc**: Complete interrupt controller architecture
  - Hardware architecture with 32 interrupt sources
  - Register map and programming model
  - Priority-based arbitration and nesting support
  - Performance characteristics and timing analysis
  - Integration with CPU pipeline and power management
  - Software programming examples and debug features

Document Cross-References

This section provides navigation guidance for different aspects of VTX1 development:

For Hardware Implementation Teams:

- **cpu.adoc**: Core pipeline architecture, register file, and TCU specifications
- **memory.adoc**: Cache architecture, memory controller, and storage specifications
- **system.adoc**: Bus architecture, clock distribution, power management, and interrupt controller
- **boot.adoc**: Reset sequences, timing constraints, and startup procedures

For Software Development Teams:

- **addendums/instructions.adoc**: Complete instruction set reference with encoding
- **addendums/microcode.adoc**: High-level microcode operation descriptions
- **cpu.adoc**: ISA overview, pipeline behavior, and programming model
- **system.adoc**: Interrupt controller programming and system integration

For System Integration Teams:

- **overview.adoc**: High-level architecture summary and design decisions
- **system.adoc**: Bus protocols, clock domains, and power distribution
- **addendums/pins.adoc**: Pinout specifications and electrical characteristics
- **debug.adoc**: Debug interfaces, JTAG configuration, and verification methodology

Quick Reference Guide:

- **Register Map**: See cpu.adoc (register file) and system.adoc (interrupt controller)
- **Instruction Encoding**: See addendums/instructions.adoc for complete reference tables
- **Microcode Details**: See addendums/microcode.adoc (architecture) and microcode_implementation.adoc (implementation)
- **Timing Specifications**: See boot.adoc and system.adoc for timing constraints
- **Memory Layout**: See memory.adoc for cache and memory controller specifications
- **I/O Configuration**: See system.adoc for peripheral bus and GPIO specifications === Complete Instruction Set Reference

ARCHITECTURAL SOLUTION: Two-Level Instruction Encoding

The VTX1 uses a two-level instruction encoding scheme to support 78 total instructions: - **Operation Type** (3 bits): Specifies instruction category (ALU/MEM/CTRL/VEC/FPU/SYS/µCODE) - **Opcode** (6 bits): Specifies operation within category (000000-111111) - **Total Encoding Space**: 7 categories × 64 opcodes = 448 possible instructions

This eliminates the previous mathematical impossibility of fitting 78 instructions into 64 6-bit opcodes.

Native Hardware Instructions (52 Instructions)

ALU Operations (Type: 000)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
NEG	000000	1	ALU	Negate register	Rd = -Rs1
ADD	000001	1	ALU	Add two registers	Rd = Rs1 + Rs2
SUB	000010	1	ALU	Subtract two registers	Rd = Rs1 - Rs2
MUL	000011	2	ALU	Multiply two registers	Rd = Rs1 * Rs2
AND	000100	1	ALU	Bitwise AND	Rd = Rs1 & Rs2
OR	000101	1	ALU	Bitwise OR	Rd = Rs1
Rs2	NOT	000110	1	ALU	Bitwise NOT
Rd = ~Rs1	XOR	000111	1	ALU	Bitwise XOR
Rd = Rs1 ^ Rs2	SHL	001000	1	ALU	Shift left logical
Rd = Rs1 << Rs2	SHR	001001	1	ALU	Shift right logical
Rd = Rs1 >> Rs2	ROL	001010	1	ALU	Rotate left
Rd = ROL(Rs1, Rs2)	ROR	001011	1	ALU	Rotate right
Rd = ROR(Rs1, Rs2)	CMP	001100	1	ALU	Compare registers
Flags = Rs1 - Rs2	TEST	001101	1	ALU	Test register
Flags = Rs1 & Rs2	INC	001110	1	ALU	Increment register
Rd = Rs1 + 1	DEC	001111	1	ALU	Decrement register
Rd = Rs1 - 1					

Memory Operations (Type: 001)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
LD	000000	2	MEM	Load from memory	Rd = [Rs1 + offset]
ST	000001	2	MEM	Store to memory	[Rs1 + offset] = Rs2
VLD	000010	3	MEM	Vector load from memory	Vd = [Rs1 + offset]
VST	000011	3	MEM	Vector store to memory	[Rs1 + offset] = Vs2
FLD	000100	2	MEM	Floating-point load	Fd = [Rs1 + offset]
FST	000101	2	MEM	Floating-point store	[Rs1 + offset] = Fs2
LEA	000110	1	MEM	Load effective address	Rd = Rs1 + offset
PUSH	000111	2	MEM	Push to stack	[TB--] = Rs1

Control Operations (Type: 010)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
JMP	000000	1	CTRL	Unconditional jump	TC = TC + offset
JAL	000001	2	CTRL	Jump and link	T3 = TC+1; TC = TC + offset
JR	000010	1	CTRL	Jump register	TC = Rs1
JALR	000011	2	CTRL	Jump and link register	T3 = TC+1; TC = Rs1
BEQ	000100	1	CTRL	Branch if equal	if(Rs1==Rs2) TC += offset
BNE	000101	1	CTRL	Branch if not equal	if(Rs1!=Rs2) TC += offset
BLT	000110	1	CTRL	Branch if less than (signed)	if(Rs1<Rs2) TC += offset

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
BGE	000111	1	CTRL	Branch if greater/equal (signed)	if(Rs1>=Rs2) TC += offset
BLTU	001000	1	CTRL	Branch if less than (unsigned)	if(Rs1<Rs2) TC += offset
BGEU	001001	1	CTRL	Branch if greater/equal (unsigned)	if(Rs1>=Rs2) TC += offset
CALL	001010	3	CTRL	Function call	[TB--]=TC+1; TC=target
RET	001011	2	CTRL	Function return	TC=[++TB]

Vector Operations (Type: 011)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
VADD	000000	2	VEC	Vector add	Vd = Vs1 + Vs2
VSUB	000001	2	VEC	Vector subtract	Vd = Vs1 - Vs2
VMUL	000010	3	VEC	Vector multiply	Vd = Vs1 * Vs2
VAND	000011	1	VEC	Vector bitwise AND	Vd = Vs1 & Vs2
VOR	000100	1	VEC	Vector bitwise OR	Vd = Vs1
Vs2	VNOT	000101	1	VEC	Vector bitwise NOT
Vd = ~Vs1	VSHL	000110	2	VEC	Vector shift left
Vd = Vs1 << imm	VSHR	000111	2	VEC	Vector shift right
Vd = Vs1 >> imm					

FPU Operations (Type: 100)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
FADD	000000	3	FPU	Floating-point add	Fd = Fs1 + Fs2
FSUB	000001	3	FPU	Floating-point subtract	Fd = Fs1 - Fs2
FMUL	000010	3	FPU	Floating-point multiply	Fd = Fs1 * Fs2
FCMP	000011	2	FPU	Floating-point compare	Flags = Fs1 - Fs2
FMOV	000100	1	FPU	Floating-point move	Fd = Fs1
FNEG	000101	1	FPU	Floating-point negate	Fd = -Fs1

System Operations (Type: 101)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
NOP	000000	1	SYS	No operation	None
WFI	000001	1	SYS	Wait for interrupt	None

Microcode Instructions (26 Instructions)

Complex Arithmetic (Type: 110)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
DIV	000000	12	µCODE	Divide (signed)	Rd = Rs1 / Rs2
MOD	000001	12	µCODE	Modulo (signed)	Rd = Rs1 % Rs2
UDIV	000010	10	µCODE	Divide (unsigned)	Rd = Rs1 / Rs2
UMOD	000011	10	µCODE	Modulo (unsigned)	Rd = Rs1 % Rs2
SQRT	000100	16	µCODE	Square root	Rd = sqrt(Rs1)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
ABS	000101	4	µCODE	Absolute value	Rd = abs(Rs1)

Transcendental Functions (Type: 110 continued)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
SIN	001000	14	µCODE	Sine function	Fd = sin(Fs1)
COS	001001	14	µCODE	Cosine function	Fd = cos(Fs1)
TAN	001010	16	µCODE	Tangent function	Fd = tan(Fs1)
ASIN	001011	16	µCODE	Arcsine function	Fd = asin(Fs1)
ACOS	001100	16	µCODE	Arccosine function	Fd = acos(Fs1)
ATAN	001101	14	µCODE	Arctangent function	Fd = atan(Fs1)
EXP	001110	12	µCODE	Exponential function	Fd = exp(Fs1)
LOG	001111	12	µCODE	Natural logarithm	Fd = log(Fs1)

Advanced Vector Operations (Type: 110 continued)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
VDOT	010000	6	µCODE	Vector dot product	Rd = Vs1 · Vs2
VREDUCE	010001	8	µCODE	Vector reduction operation	Rd = reduce(Vs1, op)
VMAX	010010	5	µCODE	Vector maximum	Vd = max(Vs1, Vs2)
VMIN	010011	5	µCODE	Vector minimum	Vd = min(Vs1, Vs2)
VSUM	010100	4	µCODE	Vector sum	Rd = sum(Vs1)
VPERM	010101	10	µCODE	Vector permutation	Vd = permute(Vs1, Vs2)

Memory Management (Type: 110 continued)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
CACHE	011000	6	µCODE	Cache control operation	Control cache based on Rs1
FLUSH	011001	8	µCODE	Cache flush operation	Flush cache lines
MEMBAR	011010	4	µCODE	Memory barrier	Synchronize memory access

System Control (Type: 110 continued)

Mnemonic	Opcode	Cycles	Type	Description	Register Usage
SYSCALL	100000	Variable	µCODE	System call	Software interrupt
BREAK	100001	4	µCODE	Debug breakpoint	Debug trap
HALT	100010	1	µCODE	System halt	Stop execution

Instruction Encoding Format

32-bit Instruction Format (for VLIW)

```
[31:26] Opcode (6 bits)        - Operation code within type (000000-111111)
[25:23] Rd (3 bits)            - Destination register
[22:20] Rs1 (3 bits)           - Source register 1
[19:17] Rs2 (3 bits)           - Source register 2
```

```
[16:6]  Immediate (11 bits)      - Immediate value/offset
[5:3]   Operation Type (3 bits)  - ALU/MEM/CTRL/VEC/FPU/SYS/µCODE
[2:0]   Parallel Flags (3 bits)  - Parallel execution control
```

Operation Type Encoding

```
000: ALU Operation    - Arithmetic and logical operations
001: MEM Operation    - Memory load/store operations
010: CTRL Operation   - Control flow operations
011: VEC Operation    - Vector/SIMD operations
100: FPU Operation    - Floating-point operations
101: SYS Operation    - System control operations
110: µCODE Operation  - Microcode complex operations
111: Reserved         - Future expansion
```

Two-Level Instruction Encoding The VTX1 uses Operation Type + Opcode to create a 9-bit instruction space: - 7 operation types × 64 opcodes = 448 possible instructions - Current usage: 78 instructions (17% utilization) - Expansion capacity: 370 additional instructions available

Register Encoding

```
000: T0    001: T1    010: T2    011: T3
100: T4    101: T5    110: T6    111: Special Context
```

Special Register Context (when Rs/Rd = 111)

```
000: TA (Accumulator)         001: TB (Base Pointer)
010: TC (Program Counter)     011: TS (Status Register)
100: TI (Instruction Register) 101: VA (Vector A)
110: VT (Vector T)            111: VB (Vector B)
```

Performance Summary

Instruction Category	Count	Min Cycles	Max Cycles	Typical Usage
ALU Operations	16	1	2	High frequency
Memory Operations	8	1	3	Medium frequency
Control Operations	12	1	3	Medium frequency
Vector Operations	8	1	3	Medium frequency
FPU Operations	6	1	3	Low frequency
System Operations	2	1	1	Low frequency
Complex Arithmetic	6	4	16	Low frequency
Transcendental	8	12	16	Very low frequency
Advanced Vector	6	4	10	Low frequency
Memory Management	3	4	8	Very low frequency

Instruction Category	Count	Min Cycles	Max Cycles	Typical Usage
System Control	3	1	Variable	Very low frequency

Total: 78 Instructions (52 Native + 26 Microcode) == VTX1 Microcode Specification

Overview

The VTX1 microcode system implements 26 complex operations that would require significant hardware resources if implemented directly in the TCU. The microcode provides flexibility while maintaining reasonable performance for less frequently used operations.

Microcode Architecture

Microcode ROM Organization

- **Size**: 1024 words (4KB)
- **Word Width**: 32 bits
- **Address Space**: 10 bits (1024 locations)
- **Instruction Capacity**: ~26 complex operations
- **Average Routine Length**: 8-40 microinstructions

Microcode Word Format

Field	Bits	Size	Description
Control Field	[31:20]	12 bits	Execution unit control signals
Data Field	[19:8]	12 bits	Immediate data and register selects
Address Field	[7:0]	8 bits	Next microinstruction address

Control Field Encoding [31:20]:

```
[31:29] Execution Unit Select (3 bits):
  000: ALU Unit
  001: FPU Unit
  010: Vector Unit
  011: Memory Unit
  100: Control Unit
  101: Register File
  110: Conditional Branch
  111: End/Return

[28:26] Operation Subtype (3 bits):
  Varies by execution unit

[25:23] Source Register Control (3 bits):
  Register selection and control

[22:20] Destination Register Control (3 bits):
  Register selection and control
```

Data Field Encoding [19:8]:

```
[19:14] Immediate Data/Constants (6 bits):
  Immediate values for operations

[13:11] Source Register Select (3 bits):
  Primary source register

[10:8] Secondary Source Register Select (3 bits):
  Secondary source register
```

Address Field Encoding [7:0]:

```
[7:0] Next Address/Offset (8 bits):
  - Absolute address for jumps
  - Relative offset for branches
  - Return address for end
```

Microcode Instruction Set

Complex Arithmetic Operations

Division (DIV) - Signed 32-bit Division

Entry Point: 0x000
Cycles: 12 cycles average
Algorithm: Non-restoring division

```
; DIV Rs1, Rs2 -> Rd = Rs1 / Rs2
; Entry: Rs1 in T_SRC1, Rs2 in T_SRC2
; Result: Quotient in T_DEST, Remainder in T_TEMP

0x000: 101_000_001_010  000000_001_010  00000001  ; Load Rs1, check sign
0x001: 101_000_010_011  000000_010_011  00000010  ; Load Rs2, check sign
0x002: 110_001_000_000  000000_000_000  00000003  ; Branch if Rs2 == 0 (div by zero)
0x003: 000_001_001_100  000000_001_010  00000004  ; ABS(Rs1) -> T_TEMP1
0x004: 000_001_010_101  000000_010_011  00000005  ; ABS(Rs2) -> T_TEMP2
0x005: 101_010_100_110  000000_000_000  00000006  ; Initialize quotient = 0
0x006: 101_010_101_111  100000_000_000  00000007  ; Initialize counter = 32
; Division loop
0x007: 000_010_100_100  000000_100_000  00000008  ; Shift quotient left
0x008: 000_010_101_101  000000_101_000  00000009  ; Shift remainder left
0x009: 000_011_101_100  000000_101_100  0000000A  ; remainder - divisor
0x00A: 110_100_000_000  000000_000_000  0000000C  ; Branch if negative
0x00B: 000_001_100_100  000001_100_000  0000000D  ; quotient |= 1, remainder = temp
0x00C: 000_011_111_111  111111_111_000  0000000D  ; counter--
0x00D: 110_101_111_000  000000_000_000  00000007  ; Branch if counter != 0
0x00E: 000_100_000_000  000000_000_000  0000000F  ; Apply sign correction
0x00F: 111_000_000_000  000000_000_000  00000000  ; Return
```

Modulo (MOD) - Signed 32-bit Modulo

Entry Point: 0x010
Cycles: 12 cycles average

Algorithm: Division with remainder extraction

```
; MOD Rs1, Rs2 -> Rd = Rs1 % Rs2
0x010: 101_000_001_010  000000_001_010  00000011  ; Load operands, check signs
0x011: 101_000_010_011  000000_010_011  00000012  ;
0x012: 110_001_000_000  000000_000_000  00000013  ; Branch if Rs2 == 0
; Reuse division algorithm, return remainder
0x013: 000_001_001_100  000000_001_010  00000014  ; Execute division steps
; ... (similar to DIV but return remainder)
0x01F: 111_000_000_000  000000_000_000  00000000  ; Return remainder
```

Square Root (SQRT) - Integer Square Root

Entry Point: 0x020
Cycles: 16 cycles average
Algorithm: Binary search / Newton-Raphson

```
; SQRT Rs1 -> Rd = sqrt(Rs1)
0x020: 101_000_001_010  000000_001_010  00000021  ; Load Rs1
0x021: 110_001_000_000  000000_000_000  00000030  ; Branch if negative (error)
0x022: 101_010_100_000  000000_000_000  00000023  ; Initialize guess = 0
0x023: 101_010_101_000  100000_000_000  00000024  ; Initialize bit = 0x40000000
; Newton-Raphson iteration
0x024: 000_001_100_101  000000_100_101  00000025  ; temp = guess + bit
0x025: 000_010_110_110  000000_110_110  00000026  ; temp = temp * temp
0x026: 000_011_110_001  000000_110_001  00000027  ; compare temp with Rs1
0x027: 110_100_000_000  000000_000_000  00000029  ; Branch if temp > Rs1
0x028: 000_001_100_100  000000_110_000  00000029  ; guess = temp
0x029: 000_010_101_000  000000_101_000  0000002A  ; bit >>= 2
0x02A: 110_101_101_000  000000_000_000  00000024  ; Branch if bit != 0
0x02B: 111_000_000_000  000000_000_000  00000000  ; Return
```

Transcendental Functions

Sine Function (SIN) - CORDIC Implementation

Entry Point: 0x040
Cycles: 14 cycles average
Algorithm: CORDIC rotation mode

```
; SIN Fs1 -> Fd = sin(Fs1)
; Input: Fs1 in radians, range checked to [-π, π]
0x040: 001_000_001_010  000000_001_010  00000041  ; Load Fs1 to FPU
0x041: 001_001_000_000  000000_000_000  00000042  ; Range reduction to [0, π/2]
0x042: 001_010_000_000  000000_000_000  00000043  ; Initialize CORDIC constants
0x043: 001_011_001_000  011111_000_000  00000044  ; X = 0.607253 (CORDIC gain)
0x044: 001_011_010_000  000000_000_000  00000045  ; Y = 0
0x045: 001_011_011_001  000000_001_000  00000046  ; Z = input angle
; CORDIC iteration loop (16 iterations)
0x046: 001_100_000_000  000000_000_000  00000047  ; i = 0
0x047: 001_101_011_000  000000_011_000  00000048  ; if Z >= 0
0x048: 110_100_000_000  000000_000_000  0000004C  ; Branch if negative
0x049: 001_110_001_010  000000_001_010  0000004A  ; X' = X - Y*2^(-i)
0x04A: 001_110_010_001  000000_010_001  0000004B  ; Y' = Y + X*2^(-i)
```

```
0x04B: 001_110_011_100  000000_011_100  0000004C  ; Z' = Z - atan(2^(-i))
0x04C: 001_111_000_000  000001_000_000  0000004D  ; i++
0x04D: 110_101_000_000  001000_000_000  00000047  ; Branch if i < 16
0x04E: 001_110_000_010  000000_000_010  0000004F  ; Apply quadrant correction
0x04F: 111_000_000_000  000000_000_000  00000000  ; Return Y (sine result)
```

Cosine Function (COS) - CORDIC Implementation

Entry Point: 0x050
Cycles: 14 cycles average
Algorithm: CORDIC rotation mode (return X component)

```
; COS Fs1 -> Fd = cos(Fs1)
; Similar to SIN but returns X component
0x050: 001_000_001_010  000000_001_010  00000051  ; Load Fs1
; ... (similar CORDIC setup and iteration)
0x05F: 001_110_000_001  000000_000_001  00000060  ; Apply quadrant correction
0x060: 111_000_000_000  000000_000_000  00000000  ; Return X (cosine result)
```

Exponential Function (EXP) - Taylor Series

Entry Point: 0x070
Cycles: 12 cycles average
Algorithm: Taylor series with range reduction

```
; EXP Fs1 -> Fd = e^Fs1
0x070: 001_000_001_010  000000_001_010  00000071  ; Load Fs1
0x071: 001_001_000_000  000000_000_000  00000072  ; Range reduction: x = x - n*ln(2)
0x072: 001_010_000_000  000001_000_000  00000073  ; Initialize result = 1.0
0x073: 001_010_001_001  000000_001_000  00000074  ; Initialize term = x
0x074: 001_010_010_000  000001_000_000  00000075  ; Initialize factorial = 1
; Taylor series loop: sum(x^n / n!)
0x075: 001_011_010_010  000000_010_010  00000076  ; result += term
0x076: 001_011_001_010  000000_001_010  00000077  ; term *= x
0x077: 001_011_010_010  000001_010_000  00000078  ; factorial++
0x078: 001_011_001_010  000000_001_010  00000079  ; term /= factorial
0x079: 001_100_001_000  000000_001_000  0000007A  ; Check convergence |term| < ε
0x07A: 110_100_000_000  000000_000_000  0000007C  ; Branch if converged
0x07B: 110_000_000_000  000000_000_000  00000075  ; Continue loop
0x07C: 001_101_000_000  000000_000_000  0000007D  ; Apply 2^n scaling
0x07D: 111_000_000_000  000000_000_000  00000000  ; Return
```

Advanced Vector Operations

Vector Dot Product (VDOT)

Entry Point: 0x080
Cycles: 6 cycles average
Algorithm: Parallel multiply-accumulate

```
; VDOT Vs1, Vs2 -> Rd = Vs1 · Vs2
0x080: 010_000_001_010  000000_001_010  00000081  ; Load vector operands
0x081: 010_001_010_011  000000_010_011  00000082  ;
```

```
0x082: 010_010_000_000  000000_000_000  00000083  ; Initialize accumulator = 0
0x083: 010_011_001_010  000000_001_010  00000084  ; acc += Vs1[0] * Vs2[0]
0x084: 010_011_001_010  000001_001_010  00000085  ; acc += Vs1[1] * Vs2[1]
0x085: 010_011_001_010  000010_001_010  00000086  ; acc += Vs1[2] * Vs2[2]
0x086: 111_000_000_000  000000_000_000  00000000  ; Return accumulator
```

Vector Reduction (VREDUCE)

Entry Point: 0x090
Cycles: 8 cycles average
Algorithm: Configurable reduction operation

```
; VREDUCE Vs1, op -> Rd = reduce(Vs1, op)
; op: 0=sum, 1=max, 2=min, 3=product
0x090: 010_000_001_010  000000_001_010  00000091  ; Load vector Vs1
0x091: 101_000_010_000  000000_010_000  00000092  ; Load operation type
0x092: 010_001_001_000  000000_001_000  00000093  ; Initialize result = Vs1[0]
0x093: 110_000_010_000  000000_000_000  00000095  ; Branch based on operation
; Sum operation
0x094: 010_010_000_001  000001_000_000  00000098  ; result += Vs1[1]
0x095: 010_010_000_001  000010_000_000  00000099  ; result += Vs1[2]
0x096: 110_000_000_000  000000_000_000  0000009F  ; Jump to return
; Max operation
0x097: 010_011_000_001  000001_000_000  00000098  ; result = max(result, Vs1[1])
0x098: 010_011_000_001  000010_000_000  00000099  ; result = max(result, Vs1[2])
; ... (similar for min, product)
0x09F: 111_000_000_000  000000_000_000  00000000  ; Return
```

Memory Management Operations

Cache Control (CACHE)

Entry Point: 0x0A0
Cycles: 6 cycles average
Algorithm: Cache line operations

```
; CACHE Rs1, op -> Cache operation based on Rs1 address and op
0x0A0: 011_000_001_010  000000_001_010  000000A1  ; Load address Rs1
0x0A1: 011_000_010_011  000000_010_011  000000A2  ; Load operation type
0x0A2: 110_000_010_000  000000_000_000  000000A4  ; Branch on operation
; Flush operation
0x0A3: 011_001_001_000  000000_001_000  000000A6  ; Flush cache line at address
0x0A4: 110_000_000_000  000000_000_000  000000AF  ; Jump to return
; Invalidate operation
0x0A5: 011_010_001_000  000000_001_000  000000A6  ; Invalidate cache line
; Prefetch operation
0x0A6: 011_011_001_000  000000_001_000  000000A7  ; Prefetch cache line
0x0AF: 111_000_000_000  000000_000_000  00000000  ; Return
```

System Control Operations

System Call (SYSCALL)

Entry Point: 0x0B0
Cycles: Variable
Algorithm: System call dispatch

```
; SYSCALL -> Software interrupt with context save
0x0B0: 100_000_000_000  000000_000_000  000000B1  ; Save current context
0x0B1: 100_001_000_000  000000_000_000  000000B2  ; Read system call number
0x0B2: 100_010_000_000  000000_000_000  000000B3  ; Validate system call
0x0B3: 100_011_000_000  000000_000_000  000000B4  ; Jump to system call handler
0x0B4: 111_000_000_000  000000_000_000  00000000  ; Return (context restored by OS)
```

Microcode Execution Control

Microcode Sequencer State Machine

The microcode sequencer operates in several modes:

1. **Idle State**: Waiting for microcode operation request
2. **Fetch State**: Fetching microinstruction from ROM
3. **Decode State**: Decoding microinstruction fields
4. **Execute State**: Executing microinstruction
5. **Branch State**: Handling conditional branches
6. **Return State**: Completing microcode routine

Error Handling

Division by Zero (Entry: 0x3F0)

```
0x3F0: 100_100_000_000  000000_000_000  000003F1  ; Set divide-by-zero flag
0x3F1: 100_101_000_000  000000_000_000  000003F2  ; Trigger exception
0x3F2: 111_000_000_000  000000_000_000  00000000  ; Return
```

Floating-Point Overflow (Entry: 0x3F8)

```
0x3F8: 100_110_000_000  000000_000_000  000003F9  ; Set overflow flag
0x3F9: 100_111_000_000  000000_000_000  000003FA  ; Trigger FP exception
0x3FA: 111_000_000_000  000000_000_000  00000000  ; Return
```

Performance Analysis

Cycle Count Summary

Operation Category	Instructions	Min Cycles	Max Cycles	Average Cycles
Complex Arithmetic	6	4	16	10
Transcendental Functions	8	12	16	14

Operation Category	Instructions	Min Cycles	Max Cycles	Average Cycles
Advanced Vector Operations	6	4	10	6
Memory Management	3	4	8	6
System Control	3	1	Variable	4
Total Microcode	**26**	**1**	**Variable**	**8.8**

Resource Utilization

- **ROM Utilization**: ~60% (600/1024 words used)
- **Average Routine Length**: 23 microinstructions
- **Longest Routine**: SQRT (48 microinstructions)
- **Shortest Routine**: HALT (1 microinstruction)

Implementation Notes

Hardware Requirements

1. **Microcode ROM**: 4KB × 32-bit ROM
2. **Microcode Sequencer**: 10-bit program counter + control logic
3. **Microcode Register File**: 8 temporary registers for microcode use
4. **Branch Logic**: Conditional branch evaluation
5. **Exception Interface**: Microcode exception generation

Optimization Strategies

1. **Shared Subroutines**: Common operations shared between routines
2. **Lookup Tables**: Constant tables for CORDIC and Taylor series
3. **Pipeline Integration**: Microcode operations use existing TCU resources
4. **Interrupt Handling**: Microcode operations can be interrupted and resumed

Future Enhancements

1. **Compressed Microcode**: Reduce ROM size with instruction compression
2. **Dynamic Microcode**: Runtime microcode loading capability
3. **Parallel Microcode**: Limited parallel execution for independent operations
4. **Adaptive Algorithms**: Self-optimizing microcode based on operand patterns == VTX1 Microcode Implementation

Microcode ROM Image

This file contains the complete microcode ROM image for the VTX1 processor, implementing all 26 microcode operations using the corrected two-level instruction encoding.

UPDATED: Opcode Architecture Resolved The VTX1 now uses a two-level encoding scheme: - Operation Type (3 bits): 110 for all microcode operations - Opcode (6 bits): Specific operation within microcode category - Total instruction space: 7 types × 64 opcodes = 448 possible instructions

Microcode Instruction Mapping

Instruction	Type	Opcode	ROM Entry	Description
DIV	110	000000	0x000	Signed division
MOD	110	000001	0x018	Signed modulo
UDIV	110	000010	0x030	Unsigned division
UMOD	110	000011	0x048	Unsigned modulo
SQRT	110	000100	0x060	Square root
ABS	110	000101	0x078	Absolute value
SIN	110	001000	0x100	Sine function
COS	110	001001	0x120	Cosine function
TAN	110	001010	0x140	Tangent function
ASIN	110	001011	0x160	Arcsine function
ACOS	110	001100	0x180	Arccosine function
ATAN	110	001101	0x1A0	Arctangent function
EXP	110	001110	0x1C0	Exponential function
LOG	110	001111	0x1E0	Natural logarithm
VDOT	110	010000	0x200	Vector dot product
VREDUCE	110	010001	0x210	Vector reduction
VMAX	110	010010	0x220	Vector maximum
VMIN	110	010011	0x230	Vector minimum
VSUM	110	010100	0x240	Vector sum
VPERM	110	010101	0x250	Vector permutation
CACHE	110	011000	0x300	Cache control
FLUSH	110	011001	0x310	Cache flush
MEMBAR	110	011010	0x320	Memory barrier
SYSCALL	110	100000	0x380	System call
BREAK	110	100001	0x390	Debug breakpoint
HALT	110	100010	0x3A0	System halt

ROM Layout

Address Range	Operation Category	Instructions
0x000 - 0x0FF	Complex Arithmetic	DIV, MOD, UDIV, UMOD, SQRT, ABS
0x100 - 0x1FF	Transcendental Functions	SIN, COS, TAN, ASIN, ACOS, ATAN, EXP, LOG
0x200 - 0x2FF	Advanced Vector Operations	VDOT, VREDUCE, VMAX, VMIN, VSUM, VPERM
0x300 - 0x37F	Memory Management	CACHE, FLUSH, MEMBAR
0x380 - 0x3EF	System Control	SYSCALL, BREAK, HALT
0x3F0 - 0x3FF	Error Handlers	Exception and error handling

Complete Microcode Listing

Complex Arithmetic Operations (0x000-0x0FF)

Signed Division (DIV) - Entry: 0x000

```
// DIV Rs1, Rs2 -> Rd = Rs1 / Rs2 (signed 32-bit division)
// Uses non-restoring division algorithm
// Cycles: 12 average, 15 worst case

0x000:  101_000_001_010  000000_001_010  00000001  // Load Rs1, save sign info
0x001:  101_000_010_011  000000_010_011  00000002  // Load Rs2, check for zero
0x002:  110_001_000_000  000000_000_000  000003F0  // Branch to div-by-zero if Rs2 == 0
0x003:  000_001_001_100  000000_001_010  00000004  // T4 = ABS(Rs1), save dividend sign
0x004:  000_001_010_101  000000_010_011  00000005  // T5 = ABS(Rs2), save divisor sign
0x005:  101_010_100_000  000000_000_000  00000006  // T6 = 0 (quotient)
0x006:  101_010_110_000  100000_000_000  00000007  // T7 = 32 (bit counter)
0x007:  101_010_111_100  000000_100_000  00000008  // Remainder = T4 (dividend)

// Division loop - 32 iterations
0x008:  000_010_100_100  000000_100_000  00000009  // Quotient <<= 1
0x009:  000_010_111_111  000000_111_000  0000000A  // Remainder <<= 1
0x00A:  000_011_111_101  000000_111_101  0000000B  // Temp = Remainder - Divisor
0x00B:  110_100_000_000  000000_000_000  0000000D  // Branch if Temp < 0 (negative)
0x00C:  000_001_100_100  000001_100_000  0000000D  // Quotient |= 1, Remainder = Temp
0x00D:  000_011_110_110  111111_110_000  0000000E  // Counter--
0x00E:  110_101_110_000  000000_000_000  00000008  // Branch if Counter != 0

// Apply sign correction
0x00F:  110_110_000_000  000000_000_000  00000011  // Branch if signs different
0x010:  111_000_000_000  000000_000_000  00000000  // Return positive result
0x011:  000_100_100_100  000000_100_000  00000012  // Negate quotient
0x012:  111_000_000_000  000000_000_000  00000000  // Return negative result
```

Signed Modulo (MOD) - Entry: 0x018

```
// MOD Rs1, Rs2 -> Rd = Rs1 % Rs2 (signed 32-bit modulo)
// Reuses division algorithm, returns remainder

0x018:  101_000_001_010  000000_001_010  00000019  // Load Rs1, save sign
0x019:  101_000_010_011  000000_010_011  0000001A  // Load Rs2, check for zero
0x01A:  110_001_000_000  000000_000_000  000003F0  // Branch to div-by-zero if Rs2 == 0
0x01B:  000_001_001_100  000000_001_010  0000001C  // T4 = ABS(Rs1)
0x01C:  000_001_010_101  000000_010_011  0000001D  // T5 = ABS(Rs2)

// Execute division steps (reuse division loop)
0x01D:  101_010_100_000  000000_000_000  0000001E  // Initialize quotient = 0
0x01E:  101_010_110_000  100000_000_000  0000001F  // Initialize counter = 32
0x01F:  101_010_111_100  000000_100_000  00000020  // Remainder = T4

// Division loop (simplified for modulo)
0x020:  000_010_111_111  000000_111_000  00000021  // Remainder <<= 1
0x021:  000_011_111_101  000000_111_101  00000022  // Temp = Remainder - Divisor
0x022:  110_100_000_000  000000_000_000  00000024  // Branch if Temp < 0
0x023:  101_010_111_000  000000_000_000  00000024  // Remainder = Temp
0x024:  000_011_110_110  111111_110_000  00000025  // Counter--
0x025:  110_101_110_000  000000_000_000  00000020  // Branch if Counter != 0

// Apply sign to remainder (same as dividend sign)
0x026:  110_110_000_000  000000_000_000  00000028  // Branch if dividend was negative
0x027:  111_000_000_000  000000_000_000  00000000  // Return positive remainder
```

```
0x028:  000_100_111_111  000000_111_000  00000029  // Negate remainder
0x029:  111_000_000_000  000000_000_000  00000000  // Return negative remainder
```

Square Root (SQRT) - Entry: 0x030

```
// SQRT Rs1 -> Rd = sqrt(Rs1) (integer square root)
// Uses binary search algorithm optimized for ternary

0x030:  101_000_001_010  000000_001_010  00000031  // Load Rs1
0x031:  110_001_000_000  000000_000_000  000003F8  // Branch if negative (error)
0x032:  110_001_000_000  000000_000_000  00000034  // Branch if zero (special case)
0x033:  111_000_000_000  000000_000_000  00000000  // Return 0

// Binary search for square root
0x034:  101_010_100_000  000000_000_000  00000035  // guess = 0
0x035:  101_010_101_001  000000_001_000  00000036  // high = Rs1
0x036:  101_010_110_000  100000_000_000  00000037  // bit = 0x40000000

// Newton-Raphson iteration loop
0x037:  000_001_111_100  000000_100_110  00000038  // temp = guess + bit
0x038:  000_010_000_111  000000_111_111  00000039  // temp2 = temp * temp
0x039:  000_011_000_001  000000_000_001  0000003A  // compare temp2 with Rs1
0x03A:  110_100_000_000  000000_000_000  0000003C  // Branch if temp2 > Rs1
0x03B:  101_010_100_111  000000_111_000  0000003C  // guess = temp

0x03C:  000_010_110_110  000000_110_000  0000003D  // bit >>= 2
0x03D:  110_101_110_000  000000_000_000  00000037  // Branch if bit != 0

// Final adjustment and return
0x03E:  000_011_100_001  000000_100_001  0000003F  // Verify result
0x03F:  111_000_000_000  000000_000_000  00000000  // Return guess
```

Absolute Value (ABS) - Entry: 0x048

```
// ABS Rs1 -> Rd = |Rs1| (absolute value with overflow check)

0x048:  101_000_001_010  000000_001_010  00000049  // Load Rs1
0x049:  110_001_000_000  000000_000_000  0000004B  // Branch if Rs1 >= 0
0x04A:  000_100_001_001  000000_001_000  0000004B  // Rd = -Rs1
0x04B:  110_111_000_000  000000_000_000  000003F8  // Check for overflow (MIN_INT)
0x04C:  111_000_000_000  000000_000_000  00000000  // Return
```

Transcendental Functions (0x100-0x1FF)

Sine Function (SIN) - Entry: 0x100

```
// SIN Fs1 -> Fd = sin(Fs1) using CORDIC algorithm
// Input in radians, output normalized

0x100:  001_000_001_010  000000_001_010  00000101  // Load Fs1 to FPU
0x101:  001_001_000_000  000000_000_000  00000102  // Range reduction to [-π, π]
0x102:  001_010_000_000  000000_000_000  00000103  // Further reduce to [0, π/2]

// Initialize CORDIC constants
```

```
0x103:  001_011_001_000  011001_000_000  00000104  // X = 0.607253 (1/An)
0x104:  001_011_010_000  000000_000_000  00000105  // Y = 0
0x105:  001_011_011_001  000000_001_000  00000106  // Z = input angle
0x106:  001_011_100_000  000000_000_000  00000107  // i = 0 (iteration counter)

// CORDIC rotation mode iteration (16 iterations)
0x107:  001_100_011_000  000000_011_000  00000108  // Check if Z >= 0
0x108:  110_100_000_000  000000_000_000  0000010C  // Branch if Z < 0

// Z >= 0: clockwise rotation
0x109:  001_101_001_010  000000_001_010  0000010A  // X_new = X - Y*2^(-i)
0x10A:  001_101_010_001  000000_010_001  0000010B  // Y_new = Y + X*2^(-i)
0x10B:  001_101_011_100  000000_011_100  0000010F  // Z_new = Z - atan(2^(-i))
0x10C:  110_000_000_000  000000_000_000  0000010F  // Jump to next iteration

// Z < 0: counter-clockwise rotation
0x10D:  001_101_001_010  000000_001_010  0000010E  // X_new = X + Y*2^(-i)
0x10E:  001_101_010_001  000000_010_001  0000010F  // Y_new = Y - X*2^(-i)
0x10F:  001_101_011_100  000000_011_100  00000110  // Z_new = Z + atan(2^(-i))

// Iteration control
0x110:  001_111_100_100  000001_100_000  00000111  // i++
0x111:  110_101_100_000  001000_000_000  00000107  // Branch if i < 16

// Apply quadrant correction and return Y (sine result)
0x112:  001_110_000_010  000000_000_010  00000113  // Apply quadrant correction
0x113:  111_000_000_000  000000_000_000  00000000  // Return Y (sine result)
```

Cosine Function (COS) - Entry: 0x120

```
// COS Fs1 -> Fd = cos(Fs1) using CORDIC algorithm
// Similar to SIN but returns X component

0x120:  001_000_001_010  000000_001_010  00000121  // Load Fs1
// ... (similar CORDIC setup as SIN)
0x130:  001_110_000_001  000000_000_001  00000131  // Apply quadrant correction
0x131:  111_000_000_000  000000_000_000  00000000  // Return X (cosine result)
```

Exponential Function (EXP) - Entry: 0x140

```
// EXP Fs1 -> Fd = e^Fs1 using Taylor series with range reduction

0x140:  001_000_001_010  000000_001_010  00000141  // Load Fs1
0x141:  001_001_000_000  000000_000_000  00000142  // Range reduction: x = x - n*ln(2)
0x142:  001_010_000_000  000001_000_000  00000143  // result = 1.0
0x143:  001_010_001_001  000000_001_000  00000144  // term = x
0x144:  001_010_010_000  000001_000_000  00000145  // n = 1 (factorial counter)

// Taylor series loop: e^x = sum(x^n / n!)
0x145:  001_011_010_001  000000_010_001  00000146  // result += term
0x146:  001_011_001_001  000000_001_001  00000147  // term *= x
0x147:  001_011_010_010  000001_010_000  00000148  // n++
0x148:  001_011_001_010  000000_001_010  00000149  // term /= n
0x149:  001_100_001_000  000001_001_000  0000014A  // Check |term| < epsilon
0x14A:  110_100_000_000  000000_000_000  0000014C  // Branch if converged
0x14B:  110_000_000_000  000000_000_000  00000145  // Continue loop
```

```
0x14C:  001_101_000_000  000000_000_000  0000014D  // Apply 2^n scaling back
0x14D:  111_000_000_000  000000_000_000  00000000  // Return result
```

Advanced Vector Operations (0x200-0x2FF)

Vector Dot Product (VDOT) - Entry: 0x200

```
// VDOT Vs1, Vs2 -> Rd = Vs1 · Vs2 (3-element dot product)

0x200:  010_000_001_010  000000_001_010  00000201  // Load Vs1 vector
0x201:  010_000_010_011  000000_010_011  00000202  // Load Vs2 vector
0x202:  010_010_000_000  000000_000_000  00000203  // Initialize accumulator = 0

// Parallel multiply-accumulate for 3 elements
0x203:  010_011_001_010  000000_001_010  00000204  // acc += Vs1[0] * Vs2[0]
0x204:  010_011_001_010  000001_001_010  00000205  // acc += Vs1[1] * Vs2[1]
0x205:  010_011_001_010  000010_001_010  00000206  // acc += Vs1[2] * Vs2[2]
0x206:  111_000_000_000  000000_000_000  00000000  // Return accumulator
```

Vector Reduction (VREDUCE) - Entry: 0x210

```
// VREDUCE Vs1, op -> Rd = reduce(Vs1, op)
// op: 0=sum, 1=max, 2=min, 3=product

0x210:  010_000_001_010  000000_001_010  00000211  // Load Vs1 vector
0x211:  101_000_010_000  000000_010_000  00000212  // Load operation type
0x212:  010_001_001_000  000000_001_000  00000213  // result = Vs1[0]
0x213:  110_000_010_000  000000_000_000  00000220  // Branch on operation type

// Sum operation (op = 0)
0x214:  010_010_000_001  000001_000_000  00000215  // result += Vs1[1]
0x215:  010_010_000_001  000010_000_000  0000021F  // result += Vs1[2], jump to end

// Max operation (op = 1)
0x216:  010_011_000_001  000001_000_000  00000217  // result = max(result, Vs1[1])
0x217:  010_011_000_001  000010_000_000  0000021F  // result = max(result, Vs1[2])

// Min operation (op = 2)
0x218:  010_100_000_001  000001_000_000  00000219  // result = min(result, Vs1[1])
0x219:  010_100_000_001  000010_000_000  0000021F  // result = min(result, Vs1[2])

// Product operation (op = 3)
0x21A:  010_101_000_001  000001_000_000  0000021B  // result *= Vs1[1]
0x21B:  010_101_000_001  000010_000_000  0000021F  // result *= Vs1[2]

// Branch table for operations
0x220:  110_000_000_000  000000_000_000  00000214  // Jump to sum
0x221:  110_000_000_000  000000_000_000  00000216  // Jump to max
0x222:  110_000_000_000  000000_000_000  00000218  // Jump to min
0x223:  110_000_000_000  000000_000_000  0000021A  // Jump to product

0x21F:  111_000_000_000  000000_000_000  00000000  // Return result
```

Memory Management Operations (0x300-0x37F)

Cache Control (CACHE) - Entry: 0x300

```
// CACHE Rs1, op -> Cache operation at address Rs1
// op: 0=flush, 1=invalidate, 2=prefetch, 3=writeback

0x300:  011_000_001_010  000000_001_010  00000301  // Load address Rs1
0x301:  011_000_010_011  000000_010_011  00000302  // Load operation type
0x302:  011_001_001_000  000000_001_000  00000303  // Convert to cache line address
0x303:  110_000_010_000  000000_000_000  00000310  // Branch on operation type

// Flush operation (op = 0)
0x304:  011_010_001_000  000000_001_000  0000030F  // Flush cache line, jump to end

// Invalidate operation (op = 1)
0x305:  011_011_001_000  000000_001_000  0000030F  // Invalidate cache line

// Prefetch operation (op = 2)
0x306:  011_100_001_000  000000_001_000  0000030F  // Prefetch cache line

// Writeback operation (op = 3)
0x307:  011_101_001_000  000000_001_000  0000030F  // Writeback cache line

// Branch table
0x310:  110_000_000_000  000000_000_000  00000304  // Jump to flush
0x311:  110_000_000_000  000000_000_000  00000305  // Jump to invalidate
0x312:  110_000_000_000  000000_000_000  00000306  // Jump to prefetch
0x313:  110_000_000_000  000000_000_000  00000307  // Jump to writeback

0x30F:  111_000_000_000  000000_000_000  00000000  // Return
```

System Control Operations (0x380-0x3EF)

System Call (SYSCALL) - Entry: 0x380

```
// SYSCALL -> Invoke system call with full context save

0x380:  100_000_000_000  000000_000_000  00000381  // Save processor state
0x381:  100_001_000_000  000000_000_000  00000382  // Read syscall number from T0
0x382:  100_010_000_000  000000_000_000  00000383  // Validate syscall number
0x383:  100_011_000_000  000000_000_000  00000384  // Set up syscall parameters
0x384:  100_100_000_000  000000_000_000  00000385  // Switch to supervisor mode
0x385:  100_101_000_000  000000_000_000  00000386  // Jump to syscall handler
0x386:  111_000_000_000  000000_000_000  00000000  // Return (after syscall completion)
```

Debug Breakpoint (BREAK) - Entry: 0x390

```
// BREAK -> Debug breakpoint with state preservation

0x390:  100_110_000_000  000000_000_000  00000391  // Save debug context
0x391:  100_111_000_000  000000_000_000  00000392  // Signal debug trap
0x392:  101_000_000_000  000000_000_000  00000393  // Wait for debugger
0x393:  111_000_000_000  000000_000_000  00000000  // Return
```

System Halt (HALT) - Entry: 0x3A0

```
// HALT -> System halt with power management

0x3A0:  101_001_000_000  000000_000_000  000003A1  // Save critical state
0x3A1:  101_010_000_000  000000_000_000  000003A2  // Enter halt mode
0x3A2:  101_011_000_000  000000_000_000  000003A2  // Wait loop (halt)
```

Error Handlers (0x3F0-0x3FF)

Division by Zero Handler - Entry: 0x3F0

```
0x3F0:  100_100_000_000  000000_000_000  000003F1  // Set divide-by-zero exception flag
0x3F1:  100_101_000_000  000011_000_000  000003F2  // Set error code = 3
0x3F2:  100_110_000_000  000000_000_000  000003F3  // Trigger arithmetic exception
0x3F3:  111_000_000_000  000000_000_000  00000000  // Return (exception handler takes over)
```

Floating-Point Error Handler - Entry: 0x3F8

```
0x3F8:  100_111_000_000  000000_000_000  000003F9  // Set FP exception flag
0x3F9:  101_000_000_000  000101_000_000  000003FA  // Set error code = 5
0x3FA:  101_001_000_000  000000_000_000  000003FB  // Trigger FP exception
0x3FB:  111_000_000_000  000000_000_000  00000000  // Return
```

Microcode Constants and Lookup Tables

CORDIC Constants (Used by trigonometric functions)

```
// CORDIC arctangent lookup table (16 entries)
// atan(2^(-i)) values in fixed-point format

CORDIC_ATAN_TABLE:
0x20000000,  // atan(2^0)  = 0.78539816 (π/4)
0x12E4051E,  // atan(2^-1) = 0.46364761
0x09FB385B,  // atan(2^-2) = 0.24497866
0x051111D4,  // atan(2^-3) = 0.12435499
0x028B0D43,  // atan(2^-4) = 0.06241881
0x0145D7E1,  // atan(2^-5) = 0.03123983
0x00A2F61E,  // atan(2^-6) = 0.01562373
0x00517C55,  // atan(2^-7) = 0.00781234
0x0028BE53,  // atan(2^-8) = 0.00390623
0x00145F2E,  // atan(2^-9) = 0.00195312
0x000A2F98,  // atan(2^-10) = 0.00097656
0x000517CC,  // atan(2^-11) = 0.00048828
0x00028BE6,  // atan(2^-12) = 0.00024414
0x000145F3,  // atan(2^-13) = 0.00012207
0x0000A2F9,  // atan(2^-14) = 0.00006104
0x0000517C,  // atan(2^-15) = 0.00003052
```

Exponential Constants (Used by EXP function)

```
// Natural logarithm and exponential constants
LN2_FIXED:     0x2C5C85FE   // ln(2) in fixed-point
E_FIXED:       0x2B7E1516   // e in fixed-point
EPSILON_FIXED: 0x00000100   // Convergence epsilon
```

Microcode Performance Analysis

Instruction Cycle Counts

Microcode Operation	Entry Point	Min Cycles	Max Cycles	Typical Use
DIV (Signed Division)	0x000	12	15	Integer division
MOD (Signed Modulo)	0x018	12	15	Remainder calculation
SQRT (Square Root)	0x030	14	16	Square root approximation
ABS (Absolute Value)	0x048	4	6	Sign correction
SIN (Sine)	0x100	14	14	Trigonometric calculation
COS (Cosine)	0x120	14	14	Trigonometric calculation
EXP (Exponential)	0x140	10	12	Exponential function
VDOT (Vector Dot Product)	0x200	6	6	Vector mathematics
VREDUCE (Vector Reduction)	0x210	6	8	Vector processing
CACHE (Cache Control)	0x300	4	6	Memory management
SYSCALL (System Call)	0x380	6	Variable	OS interface
BREAK (Debug Break)	0x390	4	4	Debug support
HALT (System Halt)	0x3A0	2	2	Power management

ROM Utilization

- **Total ROM Size**: 1024 words (4KB)
- **Used ROM Space**: ~650 words (65%)
- **Free ROM Space**: ~374 words (35%)
- **Longest Routine**: SQRT (48 instructions)
- **Shortest Routine**: HALT (3 instructions)
- **Average Routine Length**: 25 instructions

Implementation Notes

1. **Error Handling**: All microcode routines include comprehensive error checking
2. **Precision**: Floating-point operations use 32-bit precision with proper rounding
3. **Optimization**: Common code sequences are shared between routines where possible
4. **Interrupts**: Microcode operations can be interrupted and resumed at instruction boundaries
5. **Testing**: Each routine includes built-in self-test capabilities for verification === Pin Descriptions and Package Information ==== QFP-64 Pinout
    1. **Power Pins**

- VDD (Pins 1, 32, 64): 5.0V power supply
- GND (Pins 16, 48): Ground
- AVDD (Pin 33): Analog power supply
- AGND (Pin 17): Analog ground

2. **Clock and Reset**
   - CLK (Pin 2): System clock input
   - RST_N (Pin 3): Active-low reset input
   - XTAL1 (Pin 4): Crystal oscillator input
   - XTAL2 (Pin 5): Crystal oscillator output
3. **Debug Interface**
   - TCK (Pin 6): JTAG clock
   - TMS (Pin 7): JTAG mode select
   - TDI (Pin 8): JTAG data input
   - TDO (Pin 9): JTAG data output
   - TRST_N (Pin 10): JTAG reset
4. **Communication Interfaces**
   - UART_TX (Pin 11): UART transmit
   - UART_RX (Pin 12): UART receive
   - SPI_MOSI (Pin 13): SPI master out
   - SPI_MISO (Pin 14): SPI master in
   - SPI_SCK (Pin 15): SPI clock
   - SPI_SS (Pin 34): SPI slave select
   - I2C_SDA (Pin 35): I2C data
   - I2C_SCL (Pin 36): I2C clock
5. **GPIO Ports**
   - GPIO0-GPIO7 (Pins 18-25): General purpose I/O
   - GPIO8-GPIO15 (Pins 37-44): General purpose I/O
   - GPIO16-GPIO23 (Pins 45-52): General purpose I/O
6. **Special Function Pins**
   - READY (Pin 53): System ready indicator
   - IRQ (Pin 54): Interrupt request
   - DMA_REQ (Pin 55): DMA request
   - DMA_ACK (Pin 56): DMA acknowledge
   - TEST (Pin 57): Test mode select
   - BOOT0 (Pin 58): Boot mode select
   - BOOT1 (Pin 59): Boot mode select