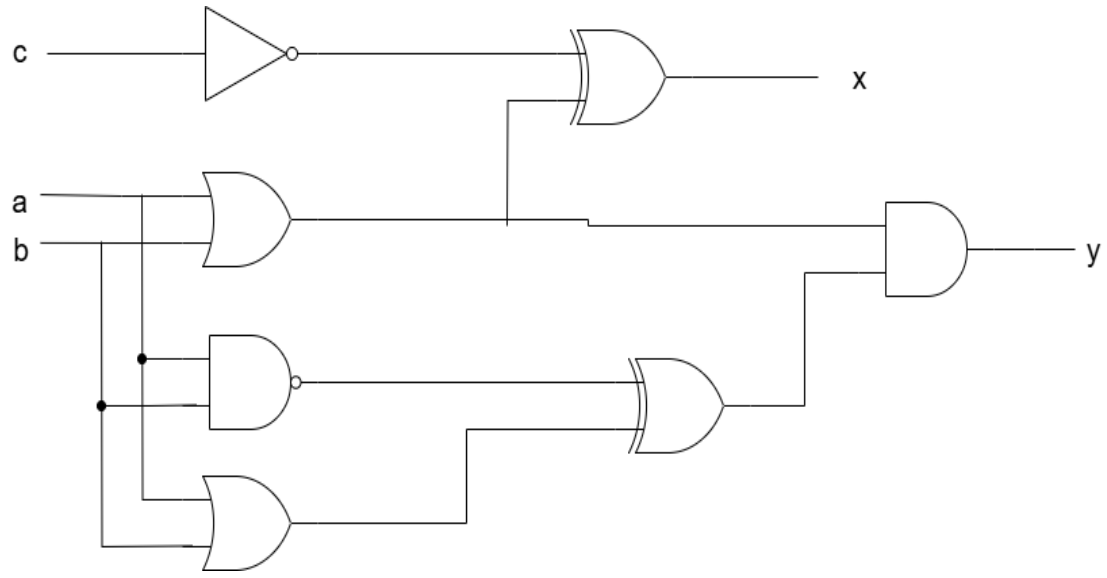
Name: Abubaker khan EE-272L Digital Systems Design

Reg. No.: 069 Marks Obtained: _____

Lab Manual

DSD Lab Manual Evaluation Rubrics

Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization (CLO1)	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation (CLO2)	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA (CLO2)	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

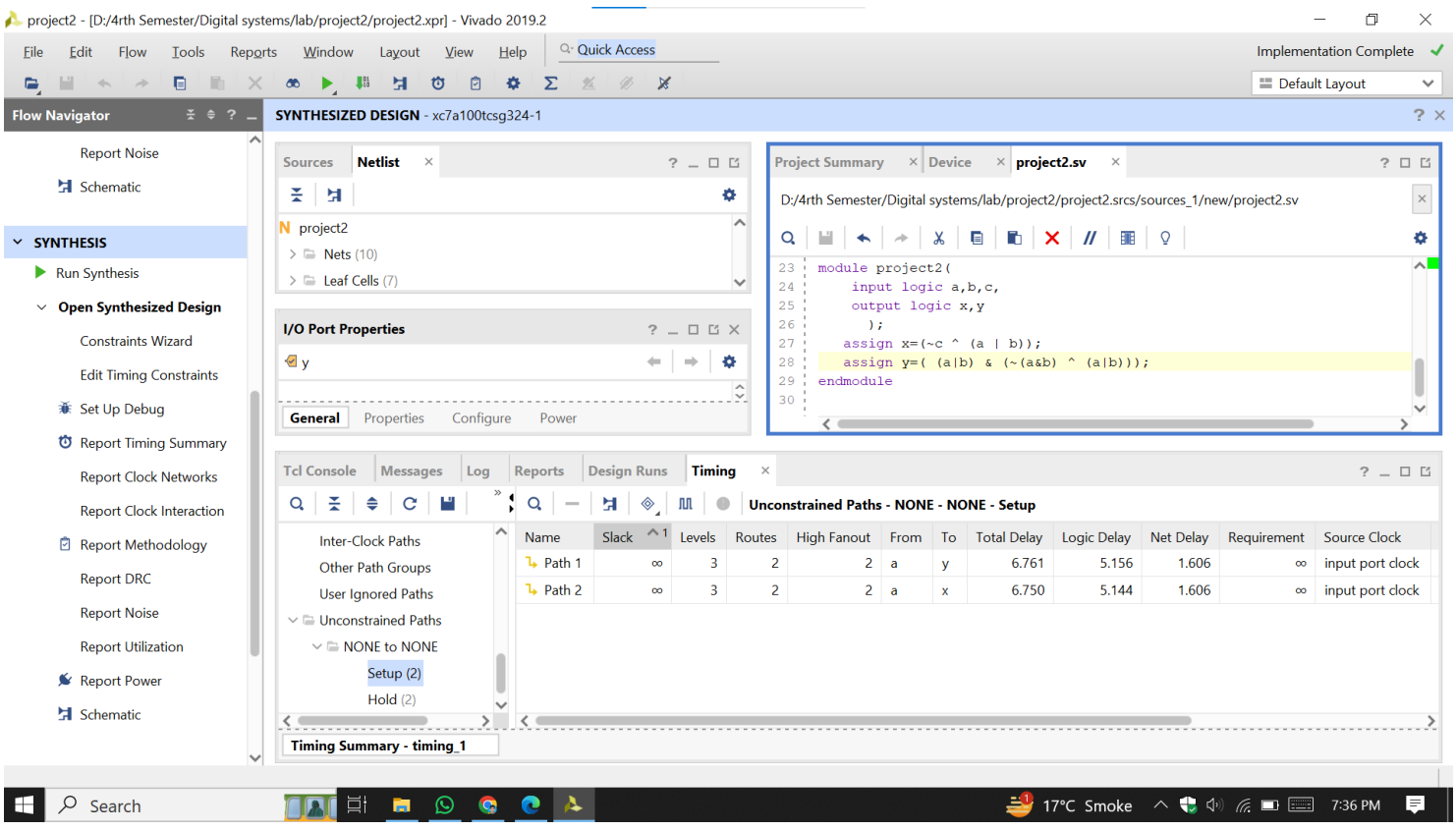


1. (a) Truth table of the circuit

a	b	c	x	y
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

(b) Maximum combinational delay in Synthesis

The maximum combinational delay is 6.761 from a to y.



(c) Resource Utilization:

```
142
143 | 7. Primitives
144 | -------------
145
146 | +----------+------+---------------------+
147 | | Ref Name | Used | Functional Category |
148 | +----------+------+---------------------+
149 | | IBUF     |    3 |                  IO |
150 | | OBUF     |    2 |                  IO |
151 | | LUT3     |    1 |                 LUT |
152 | | LUT2     |    1 |                 LUT |
153 | +----------+------+---------------------+
154
155
```

As we can see that 3 input and 2 output buffer while 1 LUT3 (3-input Look-Up Table) and 1 LUT2 (2-input Look-Up Table).

2. System Verilog code:

```
module project2(
   input logic a,b,c,
   output logic x,y
    );
  assign x  =  (~c ^ (a | b));
  assign y  =  ( (a|b) & (~(a&b) ^ (a|b)));
endmodule
```

3. Synthesize the circuit for the starter kit available in the lab.