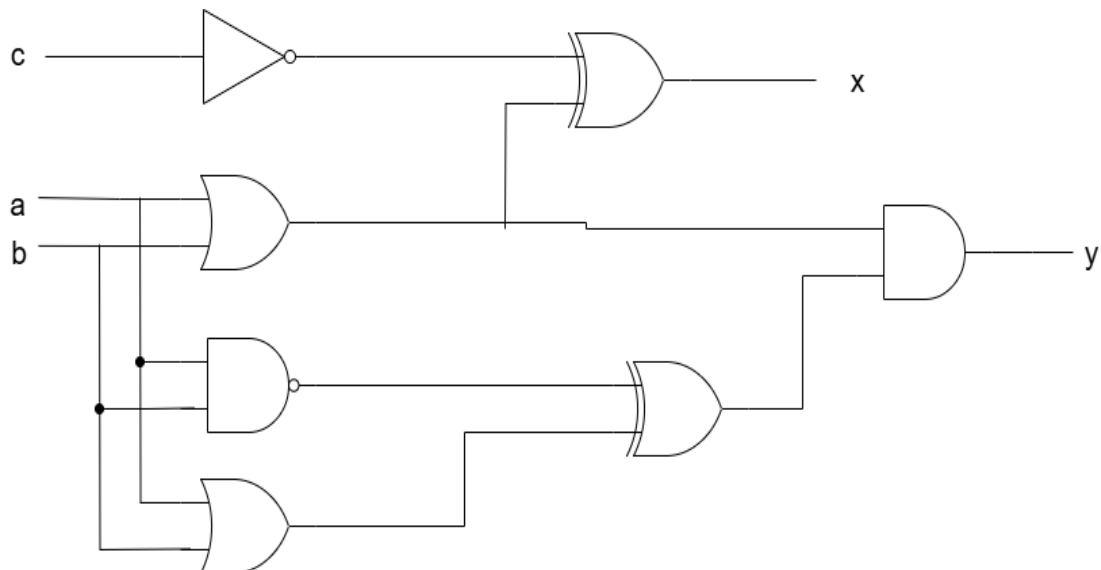


**Lab Manual****DSD Lab Manual Evaluation Rubrics**

Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization (CLO1)	3		No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working
Simulation (CLO2)	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA (CLO2)	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.



## 1. (a) Truth table of the circuit

a	b	c	x	y
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

## (b) Maximum combinational delay in Synthesis

The maximum combinational delay is 6.761 from a to y.

The screenshot displays the Vivado 2019.2 IDE interface for a project named 'project2'. The main window shows the 'SYNTHESIZED DESIGN' for the device 'xc7a100tcsq324-1'. The 'Project Summary' window is open, showing the source file 'project2.sv' with the following Verilog code:

```
23 module project2(  
24     input logic a,b,c,  
25     output logic x,y  
26 );  
27     assign x=(~c ^ (a | b));  
28     assign y=( (a|b) & ~(a&b) ^ (a|b));  
29 endmodule  
30
```

The 'Timing' window is also open, showing the 'Unconstrained Paths - NONE - NONE - Setup' report. The report lists two paths:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	2	a	y	6.761	5.156	1.606	∞	input port clock
Path 2	∞	3	2	2	a	x	6.750	5.144	1.606	∞	input port clock

The 'Timing Summary - timing\_1' window is also visible at the bottom.

### (c) Resource Utilization:

```
142 |
143 | 7. Primitives
144 | -----
145 |
146 | +-----+-----+-----+
147 | | Ref Name | Used | Functional Category |
148 | +-----+-----+-----+
149 | | IBUF      | 3   | IO                  |
150 | | OBUF      | 2   | IO                  |
151 | | LUT3      | 1   | LUT                  |
152 | | LUT2      | 1   | LUT                  |
153 | +-----+-----+-----+
154 |
155 |
```

Ref Name	Used	Functional Category
IBUF	3	IO
OBUF	2	IO
LUT3	1	LUT
LUT2	1	LUT

As we can see that 3 input and 2 output buffer while 1 LUT3 (3-input Look-Up Table) and 1 LUT2 (2-input Look-Up Table).

### 2. System Verilog code:

```
module project2(
    input logic a,b,c,
    output logic x,y
);
    assign x = (~c ^ (a | b));
    assign y = ( (a|b) & ~(a&b) ^ (a|b));
endmodule
```

### 3. Synthesize the circuit for the starter kit available in the lab.