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ULTRA-FAST SWITCHING UTILIZING AN IVA TOPOLOGY FOR CHOPPER APPLICATIONS*

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Abstract

Recent trends in power electronics indicate increasing demand for fast response switching networks with sub nanosecond switching speed at a variety of voltages. Gate driving networks meet the desired switching speeds using COTS (Commercial Off-The Shelf) parts. This work describes an IVA (Inductive Voltage Adder) system capable of producing a rise and fall time in the single digits of ns with a projected voltage output of 2 kV, using a gate driving topology to drive GaN (Gallium Nitride) HEMTs (High Electron Mobility Transistor). These rapid switching systems are proposed to be used in the LAMP (LANSCE Accelerator Modernization Project) chopper by enabling effective production of clean beam to select target stations, producing the necessary output.

INTRODUCTION

Fast response switching circuits provide the necessary rise and fall time that ordinary switching circuits can't withstand. Whereas the automotive industry, for example, can average between 10s to 100s of nanoseconds for their required rise and fall times. Fast response switching circuits that are incorporated in high efficiency pulsed power systems, such as high-powered accelerators, require faster turn on times that fall in the single digits of nanoseconds.

With the required voltage being 2 kV and the GaN devices' limit being 650 V, the addition of an IVA topology was utilized to electrically add the outputs of the GaN devices in series. With the use of 4, 1:1, pulse transformers, representing the IVA in the system, the output of each GaN device gets electromagnetically coupled to the secondary side of the transformer, then added up with the rest of signals.

IVA CONCEPT

Fundamentals

IVAs are systems that inductively add multiple pulse forming network outputs through a network of transformers with their secondaries connected in series. Each of these stages are coupled with its respective stage with a 1:1 transformer allowing the voltage pulse to travel through the transformer, theoretically undisrupted [1]. These series connections of 1:1 transformers output the addition of each stage in the IVA and supply an external load with the added signals.

Most IVAs are designed using metal rings connected to the input signal, the primary in this case, and a metal stalk that acts as the secondary. This stalk and core design produces the required inductive values but adds on a level of complexity that is eliminated with the use of the pulse transformers.

Design Specifications

An IVA typically has a metal ring and core [stalk], creating inductive values on the IVA, the IVA used here implements the use of a 1:1 pulse transformer to recreate the ring and stalk. The use of a 1:1 pulse transformer, compared to a ring and stalk, allows for the same inductive reaction to take place, but with less complexity due to the less complex nature of the design requirements of this project.

With the design of these boards having a maximum voltage output of 650 Volts, due to the GaN FETs internal limitation, the addition of an IVA effectively replaces the need for a higher voltage and more complex board. The IVA inductively adds the outputs of each stage allowing, for example, 4 separate 500-Volt stages to have a final output of 2 kV. Due to the magnetic properties of the transformer core, the voltage pulse is inductively coupled to the secondary winding, enabling the voltage from each stage to combine constructively at the IVA output.

OVERALL SYSTEM DESIGN

The overall system design of this project utilizes a 4 stage IVA design, with each stage producing an output wave of 500 V. One PCB holds all 4 driving networks and the multi staged IVA.

Gate Driver Network Design and Analysis

The gate driver network utilizes the properties of the LMG1020 gate driver and added embedded networks. An EZDrive and RL peaking circuit are utilized to meet the requirements for the output waveforms of the IVA system.

The LMG1020 has a low propagation delay for its turn-on and turn-off time, 2.5 and 2.6 ns respectively, and an ultra-fast output rise and fall time, 375 and 350 ps respectively. These fast turn on and off times allow the LMG1020 to comfortably produce the needed drive allowing the GaN FETs to output these single digits turn on times.

The EZDrive circuit is a level shift network used to help control slew rate and optimize the output signals leading into the gate of a FET. The network has a high impedance resistor, recommended value of 10 kΩ, to keep driving voltage steady and a capacitor in parallel, recommended value of 47 nf, to hold negative voltage for when the FET turns off. Along with the above components there is a Zener diode clamping network used to clamp the positive and negative gate voltage, connected from the output of the resistor and to the Kelvin source of the FET [2]. The EZDrive circuit and its values are shown in Fig. 1.

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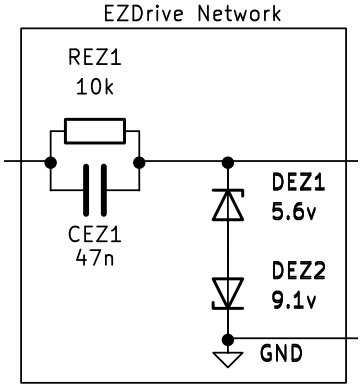

Figure 1: External EZDrive circuit.

Below can be seen how the EZDrive circuit is added to the gate driving network in whole (Fig. 2).

The RL peaking network is a resistor and inductor in series, leading from the drain or source of the FET to ground (Fig. 3). The addition of these elements allows for the charge current to pass through this network and not the load. This secondary path allows for the current in the system to be dumped to ground when and if the load becomes an open circuit.

Based on the polarity of the inputted waveform, the orientation of this network changes. With a positively polarized waveform, this RL peaking network is connected from source to ground, leaving the drain untouched. This allows the output to follow the main current path feeding signal into the drain and keeping the source grounded.

In effort to keep a modular design for a multipurpose board, the RL network can be added to either the source and ignored at the drain, or likewise, the drain and shorting the source to ground.

With a negatively polarized waveform, the RL peaking network is connected from the drain to ground, and the source is shorted directly to ground [3].

Along with the additional current path, the addition of these components, specifically the resistor, helps to handle the load pulse due to the orientation of the connection. This forces the network to use heavy pulse rated components,

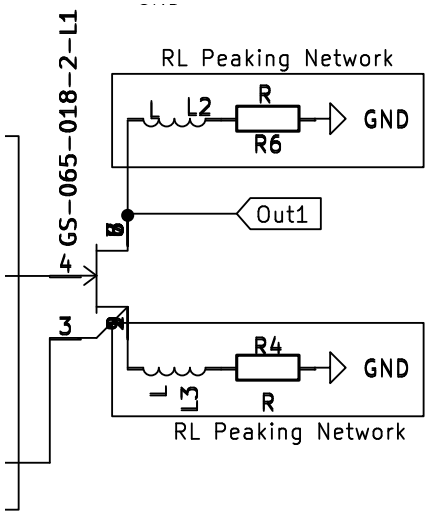

Figure 3: RL peaking network with modularity able to connect to source or drain.

voltage pulses feeding their inputs. The output letting the output to not be negatively affected by this addition.

IVA Design and Analysis

The IVA portion of this PCB houses the multi-stage inductive adder network responsible for accumulating the outputs of the gate driven signals and directing them to the load.

The IVA utilizes 4 pulse transformers, each with individual isolated of the drain, of the GaN HEMT, connects to the positive lead of a high voltage input, giving the FET the needed voltage to push out high amplitude voltage waveforms. The negative lead of the high voltage input connects to the positive lead of the primary winding on the pulse transformer.

The primary windings negative lead gets tied to the source of the GaN HEMT, connecting the source to ground and completing the necessary current loop for proper MOSFET switching. This allows the GaN HEMT to produce the required voltage waveforms.

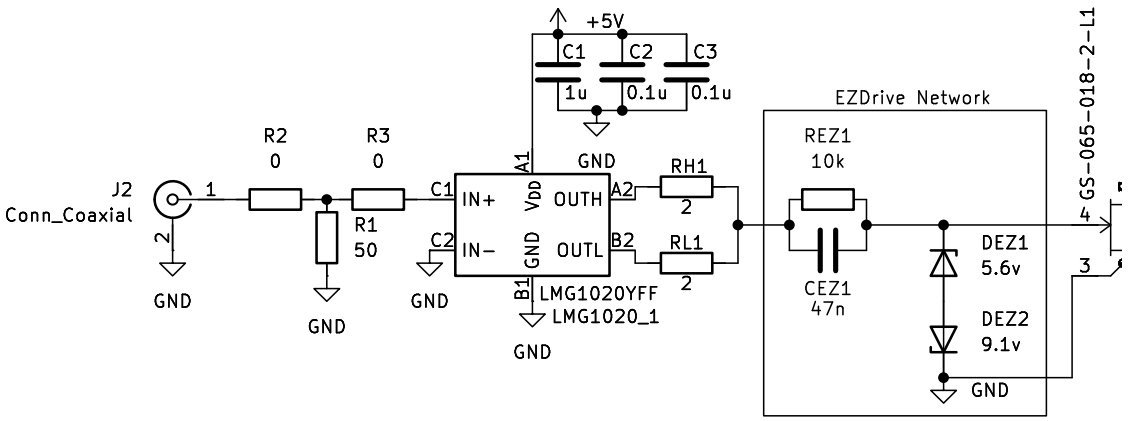

Figure 2: EZDrive circuit added into main gate driving network. The output can be seen to feed into the gate of the FET and the Kelvin source (ground).

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Full System Design

There is a need for four gate driving networks, LMG1020 and GaN FET, and one, four stage, IVA network. This ensures that each stage of the IVA has an input signal able to be added and sent to the load of the system. For design requirements that differ from those above, this can be made to incorporate more than four stages. The system layout can be seen in the diagram below (Fig. 4), the gate driving network in dashed lines and the IVA network in dotted.

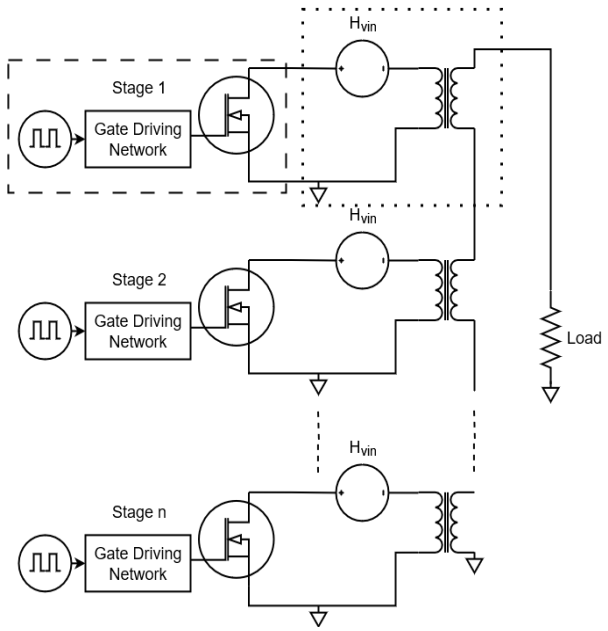

Figure 4: Full system design layout with n staged gate driving networks and IVAs.

TESTING

To test this design, an identical input signal into each of the driver networks is needed, allowing continuity across each stage of the IVA. For the signal into the system, multi output T connectors can be used to effectively send the same signal to each SMA input. A single low voltage power supply, 15 Volts regulated down to 5 Volts, is used for the input power to the gate driver chips. Additionally, the use of four external high voltage power supplies, up to 500 Volts, are used to provide the drain the voltage required to produce the desired output.

As stated above, depending on the polarity of the input pulse, the addition of the RL peaking network should be adjusted accordingly. Along with the addition, if needed, values of both the resistor and the inductor will depend on the desired output of the system.

The output is connected to a 50 **Ω**, N-type, coax connector. This connector allows for the added signal, out of the IVA, to be transmitted to an oscilloscope or load.

CONCLUSION

This paper describes the idea and possible solution for the addition of multiple gate driven signals into an IVA system, capable of outputting 2 kV with projected rise and fall times in the single digits of ns. With the components and added internal circuits, the EZDrive and RL peaking, picked to combat any parasitic $\frac{di}{dt}$ in the system. This modular design allows for future work and development of this project to be effortless, with a clear indication of the main goal. As work continues, testing of a physical system will prove to show how this design works allowing a better understanding of how this simplified IVA network performs.

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