ISBN: 978-3-95450-261-5 ISSN: 2673-7000 doi: 10.18429/JACoW-NAPAC2025-MOP043

FPGA IMPLEMENTATION OF A DIGITAL SIGNAL COMPONENT SEPARATOR AND A DISTURBANCE COMPENSATOR FOR THE LANSCE 805 MHz SOLID-STATE HIGH POWER RF AMPLIFIER*

S. Kwon†, J. T. M. Lyles, M. Brown, M. Sanchez Barrueta, J. T. Bradley III, W. Hall, S. J. Russell, J. A. Valladares, P. J. Van Rooy, P. Torrez, Los Alamos National Laboratory, Los Alamos, NM, USA

Abstract

Because of aging, and product discontinuity, LANSCE is investigating the replacement of high power RF amplifiers. A promising candidate is the GaN solid-state power amplifier (SSPA). For a high drain voltage, the drain power dissipation of SSPA is increased as the operating efficiency becomes low. The outphasing technique provides high efficiency operation of the SSPA. The signal component separator (SCS) of the outphasing amplifier converts one Amplitude Modulation-Phase Modulation (AM-PM) signal to two PM only signals. In this paper, the digital implementations of the two-way digital SCS and the four-way digital SCS are addressed. In addition, feedback linearizers are designed and implemented to suppress the input disturbances that exist on the signal forward paths of the outphasing amplifiers.

INTRODUCTION

The high power RF amplifiers, klystrons, of LANSCE 805 MHz CCLs have been operating for more than 5 decades. Because of aging, and product discontinuity, LANSCE is investigating the replacement of high power RF amplifiers. One of the highly promising amplifiers are the GaN amplifiers [1]. Currently, an available GaN amplifier can produce 5 kW pulsed RF power. Hence, in order to produce the equivalent or better performance than a LANSCE klystron of which peak power is 1.25 MW, a multitude of Solid-State Power Amplifiers (SSPA) are to be combined together. For a high drain voltage, the drain power dissipation is increased as the operating efficiency becomes low [1]. In order to operate the SSPA at high efficiency, the amplifier is operated as close as possible to the 1 dB compression zone. The outphasing technique can provide this requirement of the SSPA operation. In the outphasing amplifier, the Amplitude Modulation-Phase Modulation (AM-PM) input signal is converted to con-stant envelope PM signals, so that each amplifier of the forward signal path linearly amplifies constant envelope PM input signals [2, 3]. The combiner sums the amplified PM signals, yielding the signal of linear amplification of the outphasing amplifier input signal.

The core part of the outphasing amplifier is the signal component separator (SCS) that converts the AM-PM input signal to constant envelope PM signals. Most SCS techniques are implemented on the analog circuits [2]. In this paper, a digital signal component separator (DSCS) in Inphase/Quadrature (I/Q) coordinated is addressed. The DSCS is implemented on an Intel Stratix III commercial board which supports four 150 MSPS ADCs and four 250 MSPS DACs.

In addition to the DSCS, a compensator for the slowly varying amplitude and phase disturbances that may exist on the RF forward paths are investigated. The sources of these disturbances may be the parameter drifts of the amplifiers themselves, droops and ripples of DC power source, or temperature variation caused by the imperfect cooling system. In this outphasing amplifier design, a digital feedback linearizer is implemented to compensate for these disturbances. The disturbance suppression performance of the feedback linearizer is verified on a low power testbench and the results are reported.

OUTPHASING AMPLIFIER AND SIGNAL COMPONENT SEPARATOR

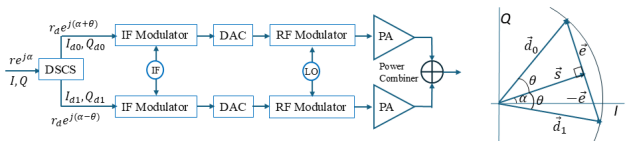

Figure 1: Two-way DSCS outphasing amplifier schematic and vector diagram.

The phase modulated components are generated using vector decomposition of the baseband signal in I/Q coordinate.

Consider the phasor diagram shown in Fig. 1. The input vector $\vec{s}$ can be expressed as the complex form in I/Q coordinate as:

$$\vec{s} = re^{j\alpha} = I + jQ \tag{1}$$

$$|\vec{s}| = r \leq 1, \alpha = \text{atan}\left(\frac{Q}{I}\right)$$

When the vector $\vec{s}$ is projected to the unit circle, the projecting vector is defined by:

$$\vec{e} = e_I + je_Q \tag{2}$$

$$e_I = -\sin(\alpha)\sqrt{1-r^2}$$

$$e_Q = +\cos(\alpha)\sqrt{1-r^2}$$

and the two signals of two-way SCS are given by:

$$\vec{d}_0 = r_d e^{j(\alpha+\theta)} = I_{d0} + jQ_{d0} \tag{3}$$

$$\vec{d}_1 = r_d e^{j(\alpha-\theta)} = I_{d1} + jQ_{d1} \tag{4}$$

* Work supported by LANL LDRD DI.
† skwon@lanl.gov

ISBN: 978-3-95450-261-5 ISSN: 2673-7000 doi: 10.18429/JACoW-NAPAC2025-MOP043

where

$$\theta = \text{atan}\left(\frac{\sqrt{1-r^2}}{r}\right)$$

$$I_{d0} = I + e_I, Q_{d0} = Q + e_Q$$

$$I_{d1} = I - e_I, Q_{d1} = Q - e_Q$$

The angle θ between $\vec{s}$ and $\vec{d}_0$, and between $\vec{s}$ and $\vec{d}_1$, is factored by the magnitude r of the source signal. The two-way SCS can be easily extended to the four-way SCS as shown in Fig. 2. The DSCS output vectors are:

$$\vec{d}_A = r_s e^{j(\alpha+\theta+\varphi)} = I_A + jQ_A$$
$$\vec{d}_B = r_s e^{j(\alpha+\theta-\varphi)} = I_B + jQ_B$$
$$\vec{d}_C = r_s e^{j(\alpha-\theta+\varphi)} = I_C + jQ_C$$
$$\vec{d}_D = r_s e^{j(\alpha-\theta-\varphi)} = I_D + jQ_D$$

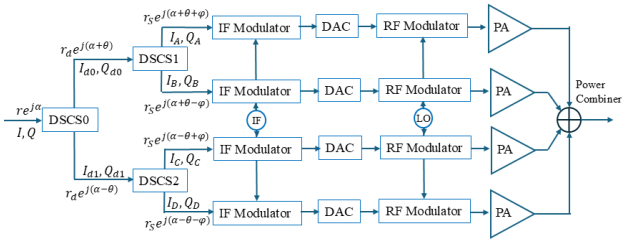

Figure 2: Four-way DSCS outphasing amplifier.

Both the two-way SCS and the four-way SCS and the IF modulators are implemented on the Intel Stratix III 3SL150 FPGA board with 150 MSPS ADCs and 250 MSPS DACs. The RF frequency of LANSCE CCLs is 805 MHz and the intermediate frequency of the LANSCE digital field control system is 25.15625 MHz [4].

For the IF modulators, the Intel FPGA NCO (numerically controlled oscillator) IP is used to generate IF signal. For the RF modulators, an analog front end of the LANSCE low level RF system is used. CORDICs (COordinate Rotation Digital Computer) are implemented on the FPGA to calculate the phase/amplitude of the I/Q vector and the square root.

Figure 3 and Fig. 4 respectively show the oscilloscope captured RF signals of the two-way and the four-way DSCS outphasing amplifiers. The baseband I/Q input signal for DSCS is generated on the FPGA, so that it mimics the baseband control signal of LANSCE digital low level RF control system for the LBEG H- beam loading. The combiner constructs the AM-PM RF signal that has the same shape of the AM-PM RF signal of the DSCS input. The RF modulation signals of the baseband DSCS outputs are constant envelope PM signals, which drive the power amplifiers of each signal forward path.

FEEDBACK LINEARIZER

By the DSCS, the AM-PM signal is converted to constant envelope PM signals, which is amplified by the intermediate

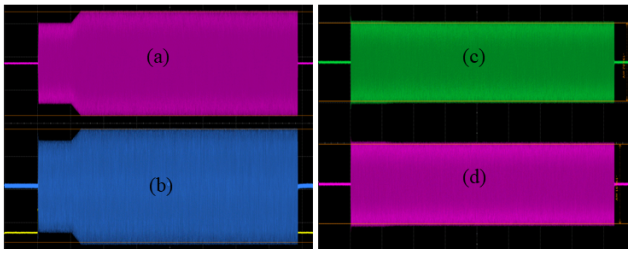

Figure 3: Oscilloscope captured waveforms of two-way DSCS outphasing amplifier. (a) AM-PM RF signal of the baseband control signal; (b) Combiner output RF signal; (c-d) two RF modulation signals of the baseband DSCS outputs.

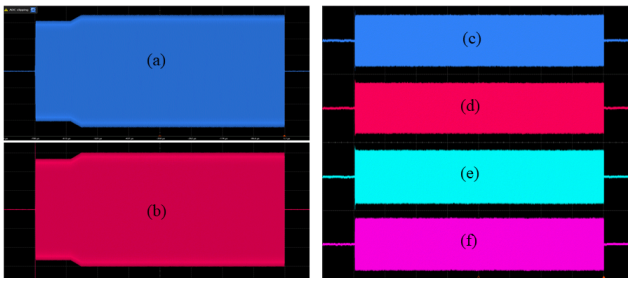

Figure 4: Oscilloscope capture waveforms of Four-way DSCS Outphasing Amplifier. (a) AM-PM RF signal of the baseband control signal; (b) Combiner output RF signal; (c-f) PM RF signals of 4 baseband DSCS outputs.

amplifiers to operate the power amplifiers in their compression zone for high efficiency. This operation leads to nonlinear distortions at the outputs. This issue can be corrected by a linearizer. On the other hand, there exist the both amplitude and phase drifts on the forward path of signals, due to the temperature drift, power supply droop, high power supply ripples, etc. These input disturbances can be suppressed by feedback control. Then, a feedback linearizer provides both the linearization and the input disturbance suppression.

Consider the functional block diagram shown in Fig. 5. In Fig. 5, r_0, r_1, are 2-dimensional I/Q vector outputs of DSCS, u_0, u_1 are 2-dimensional I/Q vector outputs of the feedback linearizers, d_{in0}, d_{in1} are 2-dimensional I/Q vector of input disturbances, and G_0, G_1 are 2-by-2 diagonal transfer matrices of the power amplifiers in I/Q coordinate. The possible crosscouplings in the I/Q coordinate power amplifiers are lumped to the input disturbances d_{in0}, d_{in1}.

The output u_0 of the feedback linearizer C_0 is expressed as:

$$u_0 = (I_2 + C_0G_0)^{-1} C_0r_0 - (I_2 + C_0G_0)^{-1} C_0G_0d_{in0}$$

where I_2 is 2-by-2 identity matrix. When the feedback controller is tuned to satisfy $|C_0(\omega)| \gg 1$, u_0 is approximated as:

$$u_0 \approx G_0^{-1}r_0 - d_{in0}. \quad (5)$$

Since u_0, r_0 are known and the transfer matrix G_0 of the power amplifier is identified by step response method, the

ISBN: 978-3-95450-261-5 ISSN: 2673-7000 doi: 10.18429/JACoW-NAPAC2025-MOP043

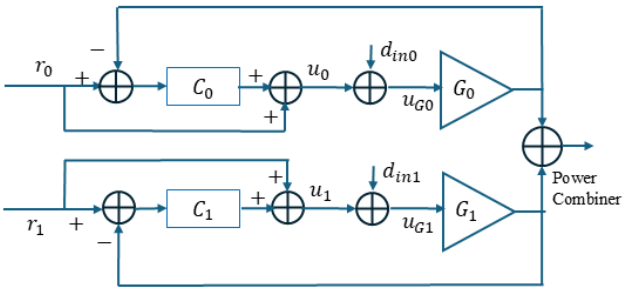

Figure 5: Functional block diagram of two-way DSCS outphasing amplifier with feedback linearizers.

feedback linearizer can estimate the input disturbance:

$$\hat{d}_{in0} \approx G_0^{-1} r_0 - u_0. \tag{6}$$

Using the same approach, u_1 is approximated as:

$$u_1 \approx G_1^{-1} r_1 - d_{in1} \tag{7}$$

and the estimate of the input disturbance d_{in1} becomes:

$$\hat{d}_{in1} \approx G_1^{-1} r_1 - u_1. \tag{8}$$

The feedback linearizers implemented in this paper are of Proportional Integral (PI) type. Since the input disturbances are slowly varying, by a proper tuning of the error integral gain, $|C_0(\omega)| \gg 1$ is achieved at low frequency and (5), (7) are achieved. Note that from (5), (7), the approximations of the amplifier inputs u_{G0}, u_{G1} are obtained.

$$u_{G0} \approx G_0^{-1} r_0 \tag{9}$$

$$u_{G1} \approx G_1^{-1} r_1 \tag{10}$$

Since r_0, r_1 are baseband DSCS output I/Q signals and their amplitudes are constants, the amplitudes of the driving RF signals of the amplifiers are constant. Figure 6 shows the oscilloscope captured RF signals for two-way DSCS outphasing amplifier with PI feedback linearizers. The input disturbances are 4.8 kHz ±10% sinusoidal amplitude ripples. The RF modulation signals of the PI feedback linearizer outputs shown in Fig. 6(e) and Fig. 6(f), compensate for the input disturbances and as a result, the amplitudes of the RF modulation signals of the amplifier inputs are constant as shown in Fig. 6(g) and Fig. 6(h).

SUMMARY

In this paper, a digital implementation of the signal component separator (SCS) is addressed. Two-way DSCS and the four-way DSCS are implemented on the FPGA. The digitization of SCS on the FPGA provides high flexibility of design, modification, parameter adjustment. On the other hand, digital PI feedback linearizers are implemented to suppress the high voltage droop, amplitude and phase drift due to possible imperfect cooling system. The performances of the DSCSs and the feedback linearizers are verified at the low power testbench.

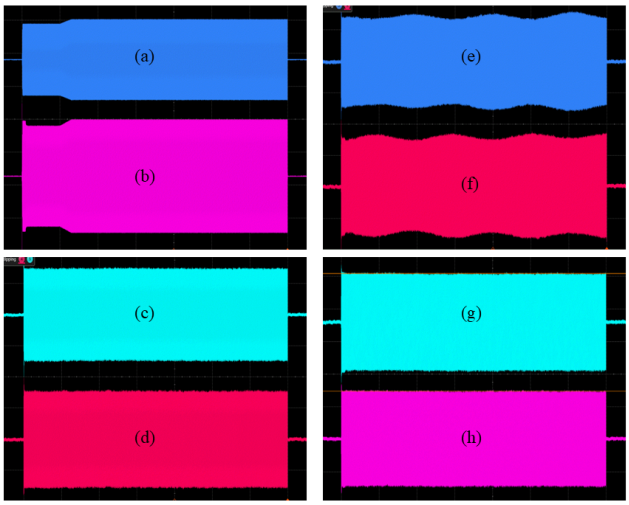

Figure 6: The performance of the feedback linearizers with 4.8 kHz sinusoidal ripple. (a) RF modulation signal of DSCS input; (b) Combiner output RF; (c),(d) RF modulation signals of the DSCS inputs r_0, r_1; (e),(f) RF modulation signals of the feedback linearizer outputs u_0, u_1; (g),(h) Amplifier Input RF modulation signals of the amplifier inputs u_{G0}, u_{G1}.

REFERENCES

[1] J. Lyles *et al.*, "New concepts for a high power 805 MHz RF amplifier for LANSCE using Gallium Nitride semiconductors", in *Proc. LINAC'24*, Chicago, IL, USA, Aug. 2024, pp. 238–240. doi:10.18429/JACoW-LINAC2024-MOPB088

[2] T. W. Barton and D. J. Perreault, "Theory and Implementation of RF-Input Outphasing Power Amplification", *IEEE Trans. Microwave Theory Tech.*, vol. 63, no. 12, pp. 4273–4283, Dec. 2015. doi:10.1109/tmtt.2015.2495358

[3] Y. Tian, Q. Hammi, S. Boumaiza, and F. M.Ghannouchi, "Design and Optimization of Digital Signal Components Separator of LINAC Transmitters Using FPGA Processors", in *Proc. ICSPC'2007*, Dubai, UAE, Nov. 2007, pp. 836-839.

[4] S. Kwon *et al.*, "FPGA Implementation of a Control System for the LANSCE Accelerator", in *Proc. IPAC'16*, Busan, Korea, May 2016, pp. 2771–2773. doi:10.18429/JACoW-IPAC2016-WEPOR044