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DESIGN OF A LOW-POWER PROOF-OF-CONCEPT MULTI-STAGE AMPLIFIER TEST STAND TO MODEL AND IMPLEMENT OUTPHASING CONTROL FOR THE LANSCE 805 MHZ SOLID-STATE HIGH-POWER RF AMPLIFIER*

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Abstract

Los Alamos Neutron Science Center (LANSCE) has a project to investigate the feasibility for a replacement radio-frequency (RF) amplifier that is not reliant on vacuum electron tubes, has a similar footprint, and equivalent RF functionality. Gallium Nitride (GaN) on Silicon Carbide (SiC) high electron mobility transistors (HEMT) will be used in combined configuration. To maintain existing operational capabilities with these GaN amplifiers, the low-level control system needs to be modified for maximum transistor lifetime. The HEMT operates in a saturated condition, with a constant amplitude drive signal to avoid the high-power dissipation of linear operation with reduced drive. This leaves the phase of the RF inputs as a control mechanism, utilizing outphasing for amplitude modulation of the multistage amplifier. The GaN amplifiers also require a bias sequencing/protection board that is being designed and tested separately. To test and verify the control system, a low power test rack using commercial wideband RF components was built. This model system includes drive control, four 10 W amplifier stages, a final combination chassis, and accelerator timing system. The information from this test rack will be used to learn how to efficiently control a multistage high-power GaN amplifier to fit the requirements of the LANSCE linear accelerator.

INTRODUCTION

The LANSCE linear accelerator (linac) currently uses klystrons at the core of its high-power radio-frequency (HPRF) system. These tube amplifiers can provide over a megawatt of RF power to it's coupled-cavity linac (CCL), which is able to accelerate a 100 MeV H– proton beam up to 800 MeV. This beam is crucial for supporting four of LANSCE's user facilities. LANSCE aims to run 24/7 during the annual run cycle, which demands high service hours out of the klystrons. When one fails, a replacement from a new batch is installed in its place while troubleshooting to maximize beam uptime. The newer klystrons have been failing at a faster rate and experiencing higher infant mortality [1]. This places a significant strain on the replacement inventory and spares have struggled to be satisfactorily replenished.

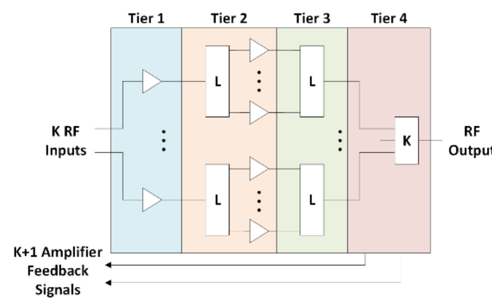

Figure 1: Multistage GaN Power Amplifier Architecture.

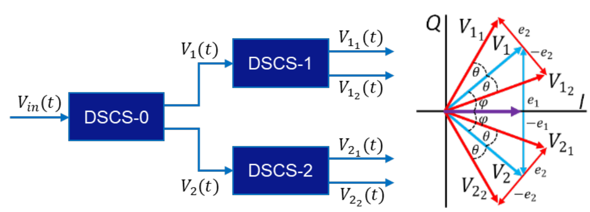

Figure 2: 4-way DSCS Expansion and Vector Diagram.

To address the mortality issues facing the LANSCE HPRF systems, alternative amplifier technology is being investigated. Solid-state power amplifiers (SSPA) show the most promise and are widely used across accelerator facilities [2, 3]. The technology that has emerged as having high power density, operating frequency, and long lifetimes necessary for LANSCE operations is newly developed Gallium Nitride (GaN) high electron mobility transistors (HEMT) on Silicon Carbide (SiC) that are capable of output 5 kW of RF power on a single chip [4]. This power density allows for a manageable multistage amplifier (Fig. 1) that can output the necessary 1.25 MW power to match the current capabilities of the LANSCE klystrons. To drive these HEMTs efficiently and get the longest lifetime out of them, constant RF drive power and bias voltage are needed. This leaves few options for the necessary RF amplitude control that LANSCE demands. Outphasing power amplifiers have demonstrated a viable approach for introducing amplitude and phase control [5, 6]. A four-way outphasing control system that uses multiple digital signal component separators (DSCS), shown in Fig. 2, is the leading solution to match the low amplitude and phase errors as well as the required control

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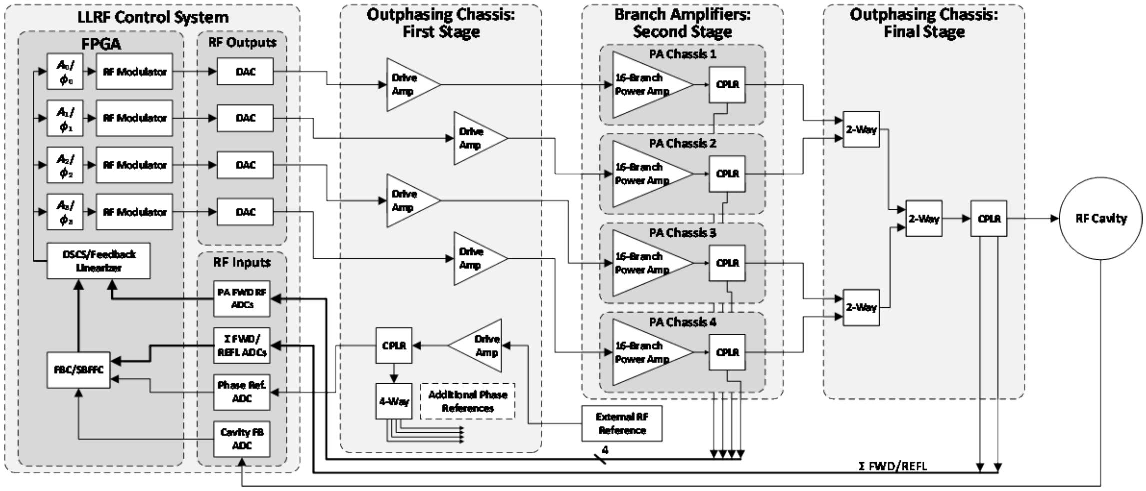

Figure 3: Proof-of-concept test stand block diagram.

margins at LANSCE [7, 8]. The outphasing control system is being developed on both current and future low-level RF (LLRF) systems. To support the development of the high-power control system, a low-power proof-of-concept test stand was designed using a multistage linear amplifier.

OUTPHASING PROOF-OF-CONCEPT TEST STAND

To ensure a GaN-based RF system can meet current LANSCE requirements while preserving the lifetime and power density benefits of the HEMTs, the SSPA is broken up into four three-stage amplifiers that each output 400 kW of RF power by utilizing a branch architecture. This multistage branched approach allows for power overhead, internal branch failures while maintaining high power output, and independently controlled amplifier systems that are combined at the final CCL drive stage [9]. By adjusting the phases of each of the four branches, the last combination has both phase and amplitude control through vector summations of the inputs. This outphasing method addresses the fine control required for accelerator tuning, but is not ideal for large power adjustments, i.e. running at much lower power during linac conditioning. Instead, a method of cutting power to a portion of the 40-amplifier section will be used for large power control margins.

To protect the GaN HEMTs and support outphasing control development, these modes of operation are to be demonstrated in a low-power branched linear amplifier that will drive an RF cavity. The block diagram for this test system is shown in Fig. 3. Various failure modes will be investigated, including module failures that result in RF opens, shorts, or line loading. Additional features of the LANSCE linac, such as feed-forward timing and beam loading compensation, will also be tested. Once developed, the outphasing control system in the test stand can be transitioned to high-power testing.

Branch Amplifier Chassis

A key component that is needed for this proof-of-concept test system is a multi-stage amplifier that emulates the proposed SSPA. To this end, the first RF drive stage is branched out to the second stage's 16 linear amplifiers and recombined to generate a 10 W output. The core amplifier chosen for the branches is the ZX60-83MP-S+ wideband medium power amplifier from Mini-Circuits, which has a measured OP1dB of around 27.5 dBm and can output more power in saturation. To get to the 10 W target output power with 16 of these amplifies, they will be overdriven into this saturation region. The amplification branches from the 16-way splitter to the 16-way combiner need to be phase-matched to achieve the best power combination. The full GaN system that this amplifier architecture is looking to mimic will use radial combiners rather than the corporate feed combiner/splitter used in this amplifier chassis. The corporate network is not radially symmetrical but is a better fit for a rack-mounted chassis than radial combiner/ splitter. The result is there may be phase mismatches introduced, resulting in combination loss for this proof-of-concept power amplifier. Tuning approaches will be investigated as needed to improve the GaN high power design.

The total phase shift introduced by the amplifier chassis can be broken down as

$$\Delta\phi_{\mathrm{Amp}} = \Delta\phi_{RFin_{split}} + \Delta angle\left(\sum_{m=1}^{16} V_{amp_m}\right) + \Delta\phi_{comb\_coup} + \Delta\phi_{coup\_RFout} \tag{1}$$

where $\Delta\phi_{RFin\_split}$ is the phase shift from the input of the chassis to the 16-way splitter, $\Delta angle\left(\sum_{m=1}^{16} V_{amp_m}\right)$ is the phase shift introduced by the vector sum of the 16 power amplifiers at the output of the 16-way combiner, $\Delta\phi_{comb\_coup}$ is the phase shift between the combiner and the directional coupler, and $\Delta\phi_{coup\_RFout}$ is the phase shift between the coupler and the output of the chassis. While the shifts introduced by cables and single input/output components can be compensated for with phase calibration offsets, the key to achieving the maximum output power while minimizing reflected power is to phase match each of the signal paths of the 16 amplifiers.

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Various challenges exist with the approach described. The main obstacle is that this 16-way amplifier needs to fit within a rack-mounted chassis without the chassis taking up too much space in the rack. There needs to be enough space for the 16 sets of phase-matched cables, DC power cables, and amplifiers. The amplifier footprint also poses a challenge, since there is enough space to put each in line with their respective combiner and splitter ports, but doing so would prevent mounting to the heatsink. Instead, the amplifiers have been split into two banks of eight, which opens up space needed for mounting them to heatsinks. A feedback directional coupler, bandpass filter, and the two 16-way combiner/splitters also need to fit with space to make necessary adjustments for any component replacements or failure mode testing. The result of the above requirements is to use a 4U chassis to have enough working space to both effectively cool the amplifiers while still providing access for maintenance.

Outphasing Chassis

The outphasing chassis serves multiple roles in this system to save rack space. Internally it provides the first stage of RF drive amplification, phase references for the control system, and the final 4-to-1 power combination with forward and reflected feedback before outputting power to the RF cavity. With the reduced input drive amplifiers and no parallel output power boosting network like those found in the 4U branch amplifier chassis, all the described internal systems fit within a 3U chassis.

To be flexible to possible control systems that will be driving the test stand, the first stage of drive amplifiers, will support an input power down to -3 dBm. Utilizing the performance of ZX60-83MP-S+ Mini-Circuits amplifiers in this chassis as well as the branch amplifier chassis minimizes part variance. Some control systems will need a phase reference for each of the four input chains, while other development options would only need one reference. Therefore, a fifth drive signal for the phase reference out of this chassis is coupled to a monitor output before being split four ways. By adding a monitor output, the chassis is more flexible for prototyping and control system testing.

The second half of the chassis used for combining the four independently controlled amplifier chains is completely passive. To achieve the highest peak power from combining the branch amplifier outputs, the phases of the RF signals entering the final combiner in this chassis need to be the same. For outphasing control of the cavity drive signal, the vector sum of the input signals needs to only vary with the input signal phase. By locking the drive amplitudes to emulate the needs of the high power GaN system, the phase of the input signals to the outphasing chassis will control the phase and amplitude of final output signal. The phases of each input n can be expressed as

$$\Delta\phi_n = \Delta\phi_{Drive\_Amp_n} + \Delta\phi_{Amp_n} + \Delta\phi_{Amp\_Outphs_n} \quad (2)$$

where $\Delta\phi_{Drive\_Amp_n}$ is the phase shift from the RF drive to the input of the amplifier chassis, $\Delta\phi_{Amp_n}$ is the phase shift inside the amplifier chassis, and $\Delta\phi_{Amp\_Outphs_n}$ is the phase shift from the output of the amplifier chassis to the input of the outphasing chassis. Again, all the cable phase shifts can be compensated for with phase calibration coefficients in the RF drive signal, ensuring each 10 W input to this chassis has the same phase.

Low Level and Outphasing Control Verification

Various diagnostics are available with these chassis' designs. For the 10 W branch amplifier chassis, this includes current measurements for each amplifier with a current probe, thermal measurements to observe any drift in gain or phase with temperature, and RF analysis of the system through forward and reflected output RF coupling. This chassis also provides both forward and reflected RF signals. For outphasing control, the phase and amplitude at the output of these amplifiers will be measured for the digital signal component separator (DSCS) in the control loop algorithm. Data on the impact of the reflected power from the final combinations in the Outphasing chassis will also be measured.

Failure analysis can be conducted in the 10 W amplifier chassis in a variety of ways. Removing DC power to one of the 16 amplifiers, replacing an amplifier with RF opens, shorts, or loads, adjusting the input power to the chassis, and modifying the RF input drive power will all be useful for observing how each failure type affects the overall system. The outphasing control system will need to be able to compensate for the varying performances in each amplifier chain, including power droop from removing portions of the branch amplifier.

The main takeaway from this test stand will be verifying the performance of the outphasing control algorithm. The LANSCE linac also utilizes a feedforward control system to support its various experimental facilities and compensate for beam loading transients [7]. To emulate this necessary feature, timing equipment is to be installed in the test stand and will be used to ensure the response of the outphasing control can support core features of the current LANSCE LLRF control systems.

FUTURE WORK

Once assembled, each branch amplifier chassis will be characterized to verify performance levels for both saturation and linear mode operation. Various failure mode analysis will be conducted to measure their impact on the amplifier. The outphasing chassis will be tested to verify drive power both to the branch amplifiers and the RF cavity. Phase offset calibrations will be conducted and feedback loops will be established to the outphasing control system to experimentally verify the DSCS performance. Reflected power measurements, both with and without simulated failure modes, will be used to better estimate the necessary protection levels needed for the GaN-based SSPA that this test stand is simulating. Finally, the test stand will be retrofitted to control the various GaN high power test systems that are being assembled.

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REFERENCES

[1] A. Waghmare and J. Valladares, "LANSCE 805 MHz klystron reliability analysis", in *Proc. IPAC'24*, Nashville, TN, USA, May 2024, pp. 1486-1488. doi:10.18429/JACoW-IPAC2024-TUPR28

[2] L. Felsberger, A. Apollonio, T. Cartier-Michaud, E. Montesinos, J. C. Oliveira, and J. A. Uythoven, "Availability Modeling of the Solid-State Power Amplifiers for the CERN SPS RF Upgrade", in *Proc. IPAC'21*, Campinas, Brazil, May 2021, pp. 2308-2311. doi:10.18429/JACoW-IPAC2021-TUPAB345

[3] P. Marchand, "Review and Prospects of RF Solid State Amplifiers for Particle Accelerators", in *Proc. IPAC'17*, Copenhagen, Denmark, May 2017, pp. 2537-2542. doi:10.18429/JACoW-IPAC2017-WEZB1

[4] J. Lyles *et al.*, "New concepts for a high power 805 MHz RF amplifier for LANSCE using Gallium Nitride semiconductors", in *Proc. LINAC'24*, Chicago, IL, USA, Aug. 2024, pp. 238-240. doi:10.18429/JACoW-LINAC2024-MOPB088

[5] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-Way Lossless Outphasing System Based on an All-Transmission-Line Combiner", *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1313–1326, Apr. 2016. doi:10.1109/tmtt.2016.2531691

[6] T. Barton, "Not Just a Phase: Outphasing Power Amplifiers", *IEEE Microwave Magazine*, vol. 17, no. 2, pp. 18-31, Feb. 2016. doi:10.1109/MMM.2015.2498078

[7] S. Kwon *et al.*, "FPGA Implementation of a Control System for the LANSCE Accelerator", in *Proc. IPAC'16*, Busan, Korea, May 2016, pp. 2771-2773. doi:10.18429/JACoW-IPAC2016-WEPOR044

[8] S. Kwon *et al.*, "FPGA Implementation of a Digital Signal Component Separator and a Disturbance Compensator for the LANSCE 805MHz Solid-State High Power RF Amplifier", presented at NAPAC'25, Sacramento, CA, USA, Aug. 2025, paper MOP043, this conference.

[9] T. W. Hall *et al.*, "Radio-Frequency Hardware Considerations for a High-Power Solid-State Amplifier", presented at NAPAC'25, Sacramento, CA, USA, Aug. 2025, paper WEP075, this conference.