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HIGH POWER 805 MHz SOLID STATE AMPLIFIERS USING GaN ON SiC HEMT FOR LANSCE CCL*

J. T. M. Lyles†, M. S. Barrueta, J. T. Bradley III, M. C. Brown, T. W. Hall,
S. I. Kwon, S. J. Russell, J. A. Valladares, P. J. Van Rooy, J. A. Vega
Los Alamos National Laboratory, Los Alamos, NM, USA

Abstract

The Los Alamos Neutron Science Center uses a coupled-cavity linac (CCL) to accelerate H- ions from 100 to 800 MeV. It is powered by forty-four 1.25 MW 805 MHz klystrons of older design. Continued supplies of identical klystrons for the linac operation beyond 2050 are uncertain. We have embarked on a feasibility study for a replacement RF amplifier without vacuum electron tubes, that fits in the space of one klystron. Commercial silicon LDMOS transistors have reduced power above 600 MHz and are limited by the maximum drain to source breakdown voltage. We selected high voltage Gallium Nitride (GaN) on Silicon Carbide (SiC) high electron mobility transistors (HEMT) to reduce the number of active devices and the complexity of power combining smaller amplifiers. They are able to operate at higher channel temperature and voltage ratings compared to silicon transistors. We have tested devices with 3.6 kW of saturated power at 100 volts, and are planning for 5 kW HEMTs for the final design. Outphasing modulation allows higher efficiency and lower thermal dissipation than class AB linear amplifiers. Power supplies and combining technology are also under study for this system.

INTRODUCTION

LANSCE uses an 800 MeV combined proton/H- linac. Protons of 100 MeV from the drift tube linac are used for isotope production while a subsequent CCL accelerates H- beam from 100 to 800 MeV. This normal conducting structure is powered by forty-four 1.25 MW 805 MHz klystrons, which all together provide approximately 44 MW of peak RF power and 5.3 MW of average power. These klystrons have been manufactured essentially unchanged since their introduction in 1968. Mean time to failure (MTTF) for more recent klystrons is shorter than it was for the original production tubes [1]. The linac must provide beams beyond 2050. There are concerns about relying solely on this vacuum electron tube technology for over 25 more years.

The LANSCE klystrons require 86 kV beam voltage from conventional mains power supplies and capacitor banks, which present their own set of difficulties. The HV transformer/rectifier units are no longer available from the original source, and rebuilding them has had mixed success. Transformer companies are principally committed to supporting utility infrastructure for increasing demands for electrical power. Scientific customers for one-off orders represent a small portion of their market. The 60 Hz AC regulators at LANSCE are similarly difficult to obtain or repair. Seven capacitor banks, each feeding 6-7 klystrons, rely on a large number of oil-paper insulated series/parallel capacitor strings. It is common for component failures to result in collateral damage in the bank due to the 230 kJ of stored energy. As engineering courses have phased out teaching vacuum tube technology and are now concentrating on solid-state devices, a longer period of on-the-job training is required for new personnel working with this equipment. These HV equipment challenges are exacerbated by having a younger engineering team less familiar with HV engineering than the designers who built the systems 53 years ago.

A new initiative is underway to develop a replacement RF power amplifier that can fit in the space of one klystron and its modulator tank [2]. This will use many solid-state amplifier (SSA) pallets combined to produce equivalent or better performance than that of a klystron. This eliminates most obsolescence concerns of the 50+ year-old technology at LANSCE, replacing them with low voltage technology. Interestingly, this work attracts new hires with skills in modern radar, scientific and broadcast high power RF.

SSA DESIGN CONSIDERATIONS

Transistor Technologies

Peak power capability has been a hallmark for vacuum tubes, where the thermal mass is large and the peak to average power ratio can be as high as ten. For a SSA, the most reliable approach is operating in continuous mode, and this has enabled them to replace klystrons or inductive output tubes at dozens of synchrotrons and storage rings worldwide [3]. Pulsed operation, such as for the LANSCE CCL, requires considering the intrinsic peak capability of the individual junctions or channels inside the devices, the packaging for thermal design, and having energy storage with capacitors, not unlike klystrons except at one thousandth of the voltage. Lessons learned from published SSA developments at other accelerators using silicon laterally-diffused metal-oxide semiconductor (LDMOS) have been reviewed for this project. The largest and most challenging pulsed RF SSA is a 1.6 MW long pulse amplifier at CERN for the SPS, where ground breaking performance first required a number of modifications to solve initial problems [4].

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†jtml@lanl.gov

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LDMOS is a mature technology from multiple manufacturers and has powered wireless communication for decades. They can be made from large wafers in conventional silicon foundries so the price per watt is attractive. Rated at a maximum operating V_{ds} (drain to source) voltage of 60-75 Volts these field effect transistors can generate up to 1.9 kW of saturated peak power below 500 MHz but at 805 MHz the gain and peak power diminishes. The drain to source capacitance of these device limits their ultimate frequency-times-power product. Conventional linear amplification (class AB) requires back off of the peak power from the saturated datasheet value, P_{sat}, which is measured with a specific amount of gain compression. This reduces the desired power capability even more, below 1 kW. LDMOS is being replaced with wide bandgap semiconductors, notably GaN. The GaN bandgap is 3.4 eV compared to 1.1 eV for LDMOS. As a result, the breakdown field in the device is 2 MV/cm whereas in LDMOS it is 300 kV/cm. Output shunt capacitance (C_{ds}) is ~1/4 that of LDMOS and input capacitance (C_{gs}) is 50% less. Power density is 5-20 W/mm of gate periphery for HV GaN and ~2 W/mm for LDMOS at 50 Volts. High power HEMT devices are now available from multiple sources [5-7]. By adjusting the doping and gate field plate design, GaN on SiC HEMT have been developed for 150-volt drain to source voltage (V_{ds}) at UHF and L band frequencies [8, 9].

High power low voltage transistors are difficult to impedance match as the conjugate output impedance needed for efficient matching to 50-Ohm circuits is related to the voltage and inversely to the power Eq. (1):

$$Rl = \frac{V_{DD}^2}{P_{out}}. \quad (1)$$

Thus, for a typical drain voltage of 50 Volts, with 1500 Watts produced, the optimal drain load impedance is 1.67 Ohms. Matching this up to fifty Ohms is difficult as the copper traces on the circuit board must carry about 30 Amps at the transistor end of matching network. This low impedance requires multiple stages of impedance transformation with additional power losses. LDMOS transistors for this power level have large dies with more shunt capacitance, complicating their output matching and further limiting their maximum operating frequency. High voltage GaN on SiC HEMTs, on the other hand, allow for simple matching. Figure 1 shows the input and output matching with our prototype 3.6 kW HEMT pallet.

The functional block of push-pull HEMT plus passive matching circuits make a pallet. A pair of pallets is combined to make a blade, which has a local protection board, gate bias sequencer with drain overcurrent sensors, and puck circulator on the output. In our preferred design, forty blades are summed together in a radial combiner to reach ¼ of the total power of the entire SSA.

Using GaN on SiC devices allow us to design a SSA that will not become obsolete within a decade. We are evaluating prototype 3.6 kW devices from a transistor fab with HV GaN on SiC capability with pulsed RF power. The device shown in Fig. 2 uses conventional Ag-Sn die attach and is designed for 805 MHz with 1 mS pulses for 12% duty factor. Operating with V_{ds} at 100 Volts, the power gain is > 18.5 dB with 72% efficiency at P_{sat} of 3.6 kW peak. RF test fixtures are mounted on water-cooled plates in our SSA laboratory, equipped with RF source, driver amplifier and loads, plus a high pulsed current power supply. We are testing 16 pallets for repeatability of power, gain, efficiency, phase response, all with varying duty factor and temperature [10]. 5 kW HEMT are in development now, and the next milestone will be to combine two sets of 8 pallets using them with radial combiners in a scaled-up bench top prototype.

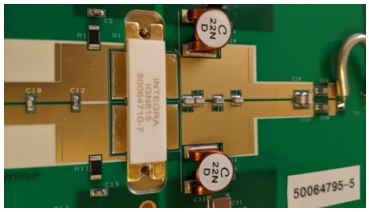

Figure 1: HEMT and push-pull matching on pallet.

Combining Power Amplifiers

For a large SSA with over 300 active devices, multistage combining networks create accumulated losses that reduce the overall efficiency. Combining schemes must also consider protection of the individual pallets from reflected power or overdrive if one or more devices fails in the network and closed loop control is operational. In addition to a power circulator in the WR975 waveguide to the CCL, individual circulators will be provided in critical points in the SSA. The limiting power level of a blade appears to be the coaxial RF connectors. We are presently charactering various commercial circulators and combiners [11]. Once the power has reached one quarter (342 kW) of the total required power then full height or half height WR975 waveguide will be used.

Thermal Considerations

Similar to klystrons it can replace, the SSA will require water cooling through the active device cooling plates along with many flow and temperature interlocks. This is a design space that heavily impacts the piping layout as well as the instrumentation and control design. Practitioners of SSA design include the mounting of the transistor to the pallet and the cooling plate, which is critical to minimize the thermal resistance from GaN die to the cooling plate. The material has nonlinear thermal conductivity with temperature [12], so it has been important to work with the manufacturer for thermal parameters measured using their advanced techniques [13]. In silicon LDMOS it is typical to operate the semiconductor junction at 150-170 deg. C. GaN on SiC semiconductor channel can operate at temperatures higher than 200 deg. C. Arrhenius plots suggest a million hours is achievable at 225 deg. C [14]. The balance of circuitry of the overall system may even set the limit on SSA MTTF.

As mentioned earlier, linear amplification requires peak power operation below P_{sat}. Operating at reduced power with high drain voltage to get a relatively flat Pout/Pin

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curve raises the drain power dissipation as the efficiency is lower with this poorly matched loadline. A different HEMT's performance in Fig. 2 shows how backed-off power operation can cause excessive heating which can damage a transistor.

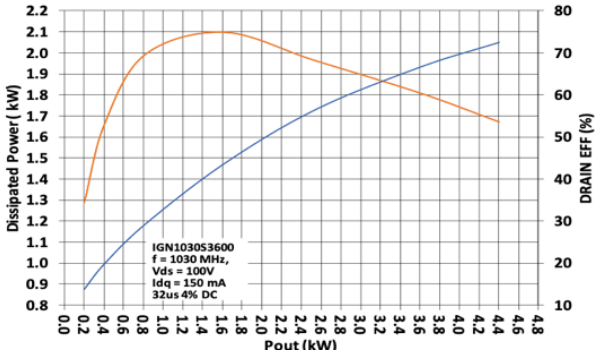

Figure 2: Drain P_{diss} vs. power reduction at a fixed V_{dss}.

In the selected HEMT, higher peak power and duty factor results in 233 Watts of average power that will be dissipated at P_{sat} operating point. This will increase as drive power is reduced. Unlike a klystron, that dumps constant beam power into the collector, rated for full beam regardless of RF power level, transistors will operate sub-optimally in certain situations:

- When conditioning a CCL cavity;
- Ramping up power slowly to minimize sparking;
- During accelerator beam tuning;
- Normal uneven RF power distribution along linac;
- Fast power fluctuation for beam loading.

Novel Amplitude Modulation Method

The outphasing modulation technique developed by Chireix has been resurrected from historic tube use [15, 16]. This method was used by LANL and Westinghouse for a 120 kW bipolar transistor SSA that powered the RFQ in the Beam Experiment Aboard Rocket (BEAR) project [17]. It uses a pair of identical amplifiers to operate at maximum (saturated) efficiency. Linear amplitude modulation is obtained when using pairs of nonlinear amplifiers in phase-opposition. Figure 3 [from Ref. 18] demonstrates the general concept.

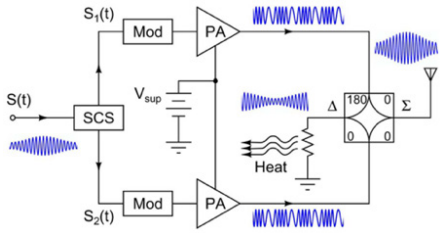

Figure 3: Pair of saturated PAs driven in phase opposition

Outphasing modulation for amplitude control is developed in the digital low level RF controller [19]. Phase modulation for the overall SSA is developed with conventional PI feedback loop outside of the outphasing system. 14 dB (50-1250 kW) of controlled dynamic range is required, where faster outphasing will be used for amplitude feedback for beam loading compensation and pulse flattening while slower power reduction by switching off designated pallets will handle any larger power adjustments needed for the previously listed conditions. A mock up low power RF system is being used to study the implementation of outphasing modulation with the digital IQ system [20].

AC/DC Power

As the SSA is a pulsed load, DC power must have sufficient stored energy for pulse flatness/regulation and to avoid significant flicker on the AC power network. We are studying the optimal location of this storage, likely to be a combination of bulk capacitance at the converters as well as distributed capacitance closer to the pallets. The exiting AC grid supplies 4.16 kV AC to the mains power supply for klystrons. This will be reconfigured to accommodate switch-mode power converters with 480 V supply voltage. The footprint of the existing capacitor bank in each sector building can provide the space for the low voltage high current power supplies for each SSA, seven for some sections of the CCL. Efficient use of electrolytic capacitors is found when they are operated close to their recommended working voltage. Most commercial parts are rated at fixed voltage intervals, the closest being 160 Volts DC. For 100-Volt HEMT this is inefficient use of these components from a energy density standpoint. For longest MTTF aluminium electrolytic capacitors are not recommended, unless there is a regular replacement interval. Other technologies such as ceramic and polymer film capacitors are being evaluated but they have much lower capacities than electrolytic capacitors. Work is ongoing to define these components.

CONCLUSION

A new SSA is being developed to supplement or replace 805 MHz high power klystrons at LANSCE. Various trade studies are underway for the engineering details of the amplifier. Prototype GaN on SiC HEMT are being tested, and plans for the coming year include testing higher power combinations to determine best combining architecture and the effectiveness of outphasing modulation. Two leading-edge technologies are being used to overcome shortcomings that would otherwise make a 1.25 MW pulsed SSA at 805 MHz very complex, physically large and inefficient.

- HV GaN on SiC HEMT for highest RF power density.
- Operation of HEMT near saturation, with outphasing modulation for linear amplitude control.

REFERENCES

[1] A. Waghmare and J. Valladares, "LANSCE 805 MHz klystron reliability and analysis" in *Proc. IPAC'24*, Nashville, TN, USA, May 2024, pp. 1486–1488. doi:10.18429/JACoW-IPAC2024-TUPR28

[2] J. Lyles *et al.*, "New concepts for a high power 805 MHz RF amplifier for LANSCE using Gallium Nitride semiconductors" in *Proc. Linac'24*, Chicago, IL USA, Aug. 2024, pp. 238–240. doi:10.18429/JACoW-LINAC2024-MOPB088

ISBN: 978-3-95450-261-5 ISSN: 2673-7000 doi: 10.18429/JACoW-NAPAC2025-WEP032

[3] M. Di Giacomo, "Solid state RF amplifiers for accelerator applications", in *Proc. PAC'09,* Vancouver, Canada, May 2009, paper TU4RA101, pp. 757–761.

[4] S. Pitman on behalf of the SY-RF-AC section, "Status update and operational experience of the 200 MHz SSPA system for the CERN SPS", presented at the 13th CW and High Average Power RF Workshop, Knoxville, TN, USA, Sep. 2024.

[5] P. Hindle, "Extremely high-power GaN devices", *Microw. J.,* Sep. 12, 2019.

[6] MACOM MAPC-A1511 GaN amplifier 100 V, 3000 W. https://www.macom.com/products/product-detail/MAPC-A1511

[7] Integra Technologies IGN1214M3200 GaN device. https://www.integratech.com/100vrf-gan/ign1214m3200

[8] G. Formicone and J. Custer, "A highly manufacturable 75-150 VDC GaN-SiC RF technology for radars and particle accelerators", *IEEE Trans. On Semiconductor Manufacturing,* vol. 31, no. 4, pp. 440–446, 2018. doi:10.1109/TSM.2018.2866209

[9] G. Formicone and J. Custer, "An emerging solid-state UHF technology based on 100 VDC GaN for powering particle Accelerators" in *Proc. CAARI'24*, Denton, TX, USA, Oct. 2024, pp. 1-9. doi:10.1063/1.5127690

[10] J. Vega *et al.*, "New development and testing facility for HPRF SSA system at LANSCE CCL", presented at NAPAC'25, Sacramento, CA, USA, Aug. 2025, paper WEP060, this conference.

[11] T. Hall *et al.*, "Radio frequency hardware considerations for a high power solid-state amplifier", presented at NAPAC'25, Sacramento, CA, Aug. 2025, paper WEP0075, this conference.

[12] A. Darwish *et al.*, "Channel temperature analysis of GaN HEMTs with nonlinear thermal conductivity", *IEEE Trans. Electron Dev.*, vol.62, no. 3, pp. 840-846, 2015.

[13] Thermal Analysis of Integra's GaN on SiC Transistors, App. Note 015, Integra Technologies Inc.

[14] Reliability of Integra Technologies 100V GaN on SiC RF Power Transistors, App. Note 011, Integra Technologies Inc.

[15] H. Chireix, "High Power Outphasing Modulation", in *Proc. Inst. Radio. Eng.*, vol. 23, no. 11, pp. 1370–1392, 1935. doi:10.1109/JRPROC.1935.227299

[16] T. Barton, "Not just a phase: outphasing power amplifiers", *IEEE Microwave Mag.*, vol. 17, pp. 18–31, 2016. 10.1109/MMM.2015.2498078

[17] C. Davis *et al.*, "60 kW UHF solid state RF power supply", in *Proc. PAC'89*, Chicago, IL, USA, Mar. 1989, pp. 162–164.

[18] D. Perreault, "A new power combining and outphasing modulation system for high-efficiency power amplification", *IEEE Trans. Circuits Syst.*, vol. 58, no. 8, 2011, pp. 1713–1726. doi:10.1109/TCSI.2011.2106230

[19] S. Kwon *et al.*, "FPGA implementation of a digital signal component separator and a disturbance compensator for the LANSCE 805 MHz solid-state high power RF amplifier", presented at NAPAC'25, Sacramento, CA, USA, Aug. 2025, paper MOP043, this conference.

[20] M. Brown *et al.*, "Design of a low-power proof-of-concept multi-stage amplifier test stand to model and implement outphasing control for the LANSCE 805 MHz solid state high-power RF amplifier", presented at NAPAC'25, Sacramento, CA, USA, Aug. 2025, paper WEP020, this conference.