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# RADIO-FREQUENCY HARDWARE CONSIDERATIONS FOR A HIGH-POWER SOLID-STATE AMPLIFIER*

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*Abstract*

A feasibility study is developing a prototype solid state power amplifier to supplant or replace 805 MHz klystrons powering the coupled-cavity linac at the Los Alamos Neutron Science Center (LANSCE). We are considering the RF passive hardware used for such an amplifier. The power from individual transistor pallets that provide 5 kW each must be power-combined to the requisite 1.25 MW needed to replace a klystron. Various approaches are being considered for combining Additionally, the protection of the various components from reflected power is essential to avoiding damage to the pallets and all of the passive RF components such as combiners and connectors. The use of magic tees as both combiners and isolators is discussed, and circulators are another critical component for this design. Finally, as power is combined, another concern is the power handling of connectors, and the balance between performance and the practicality of the large number of connectors becomes crucial.

## INTRODUCTION

LANSCE provides an 800 MeV beam of $H^-$ to four user facilities, and klystrons have been used as the RF power sources to the coupled-cavity linac (CCL). Recently, there has been a high mortality rate for these klystrons [1,2]. Solid state power amplifiers (SSPA) could potentially supplement these diminishing RF sources due to the new development of Gallium-Nitride (GaN) transistors that are capable of outputting up to 5 kW on a single chip [2, 3]. This high power density reduces the footprint of a 1.25 MW SSPA to a size that can be matched to our present RF galleries. The use of SSPA would also eliminate the high voltage power supplies and the oil tanks that house the present modulators.

This paper will address some of the challenges with the RF that are present with building such an amplifier. First, the possible combining methods will be discussed to address their how they could be used either on their own or together with other techniques to achieve 1.25 MW from individual 5 kW transistors. Next, circulators will be discussed as a method of protection for the transistors from reflections internal and external to the SSPA. Finally, the power handling of RF connectors internal to the SSPA is discussed.

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## POWER COMBINATION

A significant obstacle to the design of the SSPA is the power combining of the 5 kW transistors. Any combination scheme will have to combine power from hundreds transistors to reach 1.25 MW, and the total SSPA footprint should be small enough to fit within the present footprint of the klystrons. The SSPA will be driven by multiple inputs of differing phase (out-phasing) as the means of amplitude and phase control [4, 5], so those variations must avoid deleterious effects like reflected power in the combination scheme. Other unintentional variations such as transistor gain should also be well managed in the combination scheme.

### *Impedance Matched Combiners*

A large class of combiners matches sections of impedances to combine two or more inputs. A simple case of such a combiner is the Wilkinson topology [6], which isolates the inputs from each other and minimizes reflections via quarter wave transformers between input and output and resistors between inputs. Gysel proposed a solution to the common problem of the overheating of isolated resistors by instead dedicating a grounded load to each input to better dissipate that heat [7]. Another combiner of this type is the hybrid combiner, whose two inputs must be offset by 90° to get a single combined power.

Any of these could be used in a corporate combining structure where two transistors are combined, then the output of those is combined with two others and so on. This method would require too much space in the form of combiners and also has greater additive losses than other combination schemes so this is not a viable option. Practically, the number of 5 kW transistors that can be combined with these options is four or less due to the limitations on the voltage hold-off of connectors and the thermal management of the matching loads.

Radial combiners are an interesting case of impedance matched combiners. The physical structure of this results in $N$ inputs evenly spaced at some distance along a circular layout with the output perpendicular to their plane. The S-matrix for an N-way combiner is

$$S = \begin{bmatrix} 0 & \frac{1}{\sqrt{N}} & \frac{1}{\sqrt{N}} & & \frac{1}{\sqrt{N}} \\ \frac{1}{\sqrt{N}} & -\frac{N-1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} \\ \frac{1}{\sqrt{N}} & \frac{1}{N} & -\frac{N-1}{N} & & \frac{1}{N} \\ & \vdots & & \ddots & \\ \frac{1}{\sqrt{N}} & \frac{1}{N} & \frac{1}{N} & \cdots & -\frac{N-1}{N} \end{bmatrix} \quad (1)$$

where port 1 is the output port and ports 2 through $N + 1$ are the input ports. This does not have the isolation of other

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combiners discussed, but instead the power reflected to any input port is zero only if all the other inputs are of equal magnitude and phase.

The radial combiner can be used to combine power from a few dozen but not all of the transistors in the SSA. First, the out-phased signals cannot be combined in radial combiners as they will generate significant reflections to the transistors. Second, the output of the radial combiner is limited by its coaxial structure as discussed later. Finally, the footprint can become quite large in order to have room for N number of input connections.

### *Resonant Cavity Combiners*

A simple cylindrical resonator operating in the $TM_{010}$ is often used as a combiner [8, 9]. These combine any number of inputs coupled via loops located around the perimeter of the cavity, and the output is capacitively coupled at the center. The loaded quality factor (Q) should be minimized by maximizing the external Q with highly coupled inputs and outputs [8]. This minimizes reflections to the transistor at the beginning and end of pulses, eliminates the need for active resonance control [10], and minimizes field and thus potential arcs in the cavity. Phase changes in resonant cavities do cause high reflections, so a single combiner with an out-phasing scheme could not be used for our SSPA. They will also experience some reflected power to the inputs with magnitude and phase variations, although the exact amount would depend on the combiner design. Additionally, all the input coupling loops must be empirically adjusted to optimize performance. Because of these complications, cavity combiners are not being actively pursued.

### *Waveguide Combiners*

Waveguide combiners are a particular case of the N-way combiners that can be used at high peak power. A simple 2-way waveguide combiner has two input arms and an output arm that either branches out of the narrow dimension (electric plane) or the broad dimension (magnetic plane), and a magic tee combines the two simple tees into one device with two co-linear input arms and two output arms. If we vary the phase between two input sources using outphase modulation, power is shifted between these two ports, with one connected to the CCL and the other to a load. Well designed tuning elements will also isolate the co-linear arms from each other, providing protection to the driving stages.

### *Combiner Testing*

A prototype is being developed with 8-way radial combiners. The measurement of one of these combiners in vector form is shown along with the ideal values in Fig. 1. The measured values have been rotated to allow better visual comparison there is an arbitrary phase shift in the measurement. While the reflected power from the input ports ($S_{nn}$) and the power between input ports and the output ($S_{1n}$ & $S_{n1}$) match very well, there is significant deviation in angle and magnitude for the S-parameters between input ports. Those values still sum to a small reflected signal, but this deviation could impact the prototype as irregularities such as transistor gain or shifts in circulator performance change the different inputs. The effect on a full power SSPA will be diminished due to the large number of inputs of the full scale 40-way combiner.

Table 1: Results for the Testing a Radial Splitter and Combiner Back to Back with Varying Connections (J2 through J9) Disconnected and Loaded

| **Ports disconnected** | $S_{21}$ **dB** | $S_{11}$ **dB** |
|---|---|---|
| None | -0.020 | -31.57 |
| J2 | -1.38 | -21.29 |
| J2, J3 | -3.05 | -15.97 |
| J2, J4 | -2.97 | -16.13 |
| J2, J6 | -2.96 | -16.35 |
| J2, J6, J8 | -4.94 | -14.62 |
| J2, J4, J6, J8 | -7.32 | -14.47 |

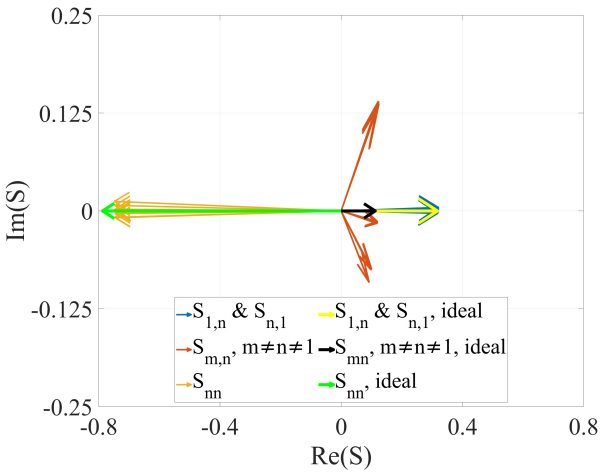


Figure 1: Measured vs. ideal S-parameters displayed as vectors for an 8-way combiner. The measured values have been phase shifted to account for the adapters used for measurement.

Another test of the radial combiners is to measure the S-parameters of two radial combiners connected together via their input ports. The prototype development is using this type of test with the transistors amplifying the signals between the two. This test gives a baseline for what should be expected from that test. Some of the connections between the radial combiner and splitter were removed and terminated with loads to provide a conservative estimate how much gain would be lost for different scenarios where transistors could fail as shown in Table 1. These results are instructive for prototype testing, and the effect in a full power SSA would be diminished due to the higher number of inputs.

Out-phasing into a waveguide magic tee network with two intermediate combinations combined in a final combiner was simulated in CST. The magic tees had -16 dB of reflection and -21 dB of isolation between inputs as a conservative

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example. The highest power reflected to the inputs was -12.0 dB, but this could be reduced to -13.0 dB by keeping the same phase offsets (82° and −103°) but changing which ports they are applied to. This is higher reflected power than desired, but manageable with circulators as discussed in the next section. Additionally, the actual magic tees produced by industry are to have optimal reflected power and isolation, further reducing the power reflected to transistors.

## CIRCULATORS

Circulators are non-reciprocal devices that isolate RF devices from their loads and will be crucial for the protection of transistors from reflected power. Circulators can be designed to operate at a more narrow band in order to reduce the insertion losses, but an adjustable bias current may be needed to maintain low loss and good isolation over varying temperatures and power levels. This is prohibitive at the transistor level where about 300 circulators and a control circuit would be needed per SSPA.

The number of high power circulators within the amplifier should be minimized to reduce the size of the SSPA. The resonant accelerator cavities present a high reflected power at the beginning and end of a pulse, and arcs also reflect power to the SSPA, which necessitates a circulator at the output. Because the magic tee offers good isolation between co-linear arms, circulators are not required at these locations. This leaves a vulnerability to arcs in the waveguide or an aberrant loss of power from a single arm. Placing circulators at the transistor output is the best option within the SSPA to protect from issues leading to reflections within any combiner, and their small power can integrate the load and cooling into a single package with the transistor amplifier pallets.

A candidate circulator rated for 5 kW is pictured in Fig. 2 with the top of the case opened. Its insertion loss was measured to vary between -0.4 dB to -0.25 dB for the two units. That is equivalent to reducing the output of each transistor by 300-400 W, or by nearly 100 kW for the few hundred transistors needed for the whole SSPA. Other circulators will be tested to see if these have better performance. The large range of measured loss is also a concern as this could result in unequal power levels going into a radial combiner. The range of the output phase variation was only 2°, however, and the isolation from the load to the input was $< -30$ dB.

## RF CONNECTORS

RF transmission line and connectors must be capable of both handling the high peak power and not impede the scalability of the design. The most susceptible component to failure is the transistor pallet, so connections at this level must be accessible and rated for its peak voltage and average power. The 7/8" EIA and 7/16 DIN standards are good sizes at this level, with the 7/16 DIN being preferred because of the ease of connection. Both have a peak voltage limit of about 2000V [11–13], which limits the power to about 80 kW, or 20 kW if we are assuming full reflected power

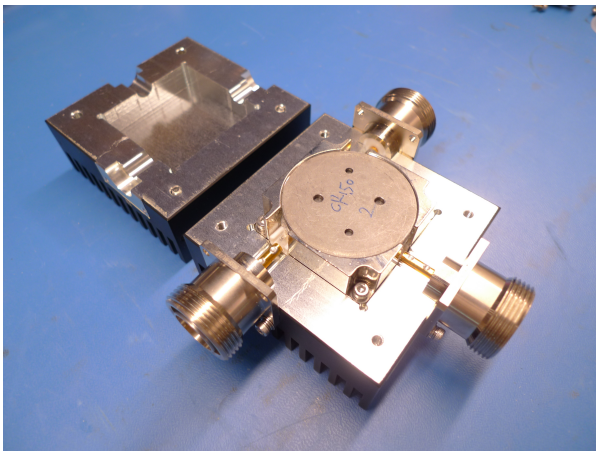

Figure 2: 5 kW circulator used for testing with casing opened.

can be observed. This allows two transistors to be combined into either connector with some margin of error for various de-rating considerations like our 7000 ft elevation. A quick connecting piece that would allow for the pallet to slide on without a collar to twist on has also been discussed, but such an item would require more testing and consideration of mechanical failure.

Combiners that have a high number of inputs such as radial combiners have coaxial transmission line outputs, so the limits at higher power are also important. The largest nominal size that can be used is 4-1/16" because this is the largest standard coaxial size that has a cut-off frequency above 805 MHz. The peak voltage limit of this size coax is about 4700 $V_{rms}$ after de-rating for our altitude, so this the limit of power that can be output in those combiners is 440 kW.

## CONCLUSIONS

A combination scheme has been determined that will allow for out-phase control, a small footprint, and reasonable reflected power. Two transistor pallets with circulators can be combined with a Gysel onto a cooling plate to have a 10 kW unit, and 40 of these can be combined via a radial combiner to produce 400 kW. Four of these can be combined via magic tees to get to reach 1.25 MW with headroom for the various losses. A scale prototype will be built to test the individual components and to identify issues in their use as a system. The individual transistor chips are currently being tested as presented in [14], and these will be prototyped into a pallet with cooling and a circulator. Next, we will power test using our 8 way combiner to ensure we can understand how well the process matches with our predictions, and we have two of these combiners that can be combined into a magic tee, allowing for a higher power test of out-phasing. Finally, the magic tee and 40-way radial combiner can be tested to power levels of a final SSA by backfeeding them with a klystron.

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