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LIFETIME EXTENSION OF LEGACY CEBAF LLRF HARDWARE

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Abstract

A significant portion of the Low-Level Radio Frequency (LLRF) hardware in Jefferson Lab's CEBAF is from the original construction of the facility using 1980's CAMAC technology. Of the fifty-three zones in CEBAF, thirty-six of them are legacy hardware. The age of the legacy system has led to difficulties in maintaining the hardware due to parts going obsolete without suitable drop-in replacements. Continued operation of the legacy system is required as the installation of LLRF 3.0 systems is costly and cannot be completed in a short period of time with the available resources. The most pressing failure in the legacy system was a failing buffer card, which is responsible for communication between the EPICs network and individual RF control modules. A new buffer card was designed as a transparent, drop in, replacement so that upgrades are simply a matter of swapping the existing legacy hardware. This buffer card upgrades a single point failure component and promises to extend the operable lifetime of CEBAF's legacy systems.

LLRF 1.0

As it currently stands, over two thirds of the LLRF system in JLab's CEBAF is original hardware. Communication between the RF Control Modules (RFCM) and the Experimental Physics and Industrial Control System (EPICS) is facilitated through the Computer Aided Measurement And Control (CAMAC) system [1]. Each RFCM is connected to its own Buffer Card inside the CAMAC crate, for a total of eight Buffer Cards per zone [1]. With thirty-six zones still using legacy hardware, this brings the total number of buffer cards in the machine to 288. These buffer cards use a now obsolete PEEL173 complex programmable logic device (CPLD), to decode read/write instructions from the CAMAC backplane. Due to the age of the PEEL's, the memory is failing, rendering the buffer cards non-functional. These failures cause intermittent issues in the operation of the zones. Whilst some LLRF 1.0 systems are being upgraded to LLRF 3.0, the upgrade process is multi-year and the current plan is not to replace all the 1.0 zones with 3.0 due to numerous constraints. The memory failures, the inability to obtain replacement components and the need to keep the LLRF 1.0 systems operational, necessitated the development of a drop-in replacement for the Buffer Card using new hardware.

LLRF 2.0/3.0

JLab's CEBAF currently contains seventeen zones equipped with either LLRF 2.0 or 3.0 systems. These new systems eliminate the need for buffer cards in the zones they are installed in as each field control chassis (FCC) communicates directly over the network [2]. These systems bring improved control of the superconducting cavities and reduce trip recovery time [2]. Upgrading all of the zones in CEBAF would be ideal, however due to resource constraints this path is not currently feasible.

CONCEPTUAL DESIGN

Multiple options were explored for the replacement controller during the development process. Current CPLDs, FPGAs and microcontrollers were all considered for use. We decided to use a microcontroller for the new revision of the buffer card due to a combination of the ease of use, availability and cost as compared to the other options. The selected microcontroller is part of the PIC18 family of devices. The PIC18F57Q43 was selected for its 8 Configurable Logic Cells (CLC), 5V operation and pin count. Updated buffer chips were selected, reducing the risk of components going obsolete in the near future and reducing the overall part count. The CLCs are programmed with the requisite logic functions to decode the read/write instructions from the CAMAC backplane, this allows the commands to be interpreted and executed in hardware leaving the microprocessor available for other operations (Fig. 1). A RS232 interface was added to the board to enable the display of additional diagnostic information.

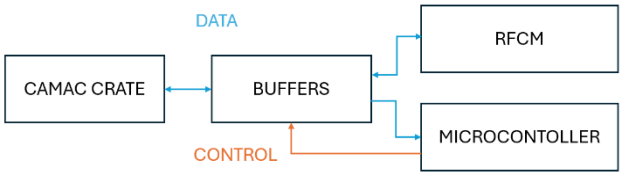

Figure 1: Operational Diagram.

CODE SIMPLIFICATION

The original code is made up of multiple independent sub-functions which make up the read, write and acknowledge functions (Fig. 2). These functions are larger than necessary, as such they were simplified using Boolean algebra, allowing the logic to fit on the available CLCs (Fig. 3).

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```
@COMMON PRODUCT TERM
FUN0 = N * /F1 * /F2 * /F4 * /F8 * /F16 ;
FUN1 = N * F1 * /F2 * /F4 * /F8 * /F16 ;
FUN2 = N * /F1 * F2 * /F4 * /F8 * /F16 ;
FUN5 = N * F1 * /F2 * F4 * /F8 * /F16 ;
FUN9 = N * F1 * /F2 * /F4 * F8 * F16 ;
FUN16 = N * /F1 * /F2 * /F4 * /F8 * F16 ;
FUN17 = N * F1 * /F2 * /F4 * /F8 * F16 ;
FUN18 = N * /F1 * F2 * /F4 * /F8 * F16 ;

@I/O DIRECTION

@LOGIC EQUATION
RE = / ( FUN0 + FUN1 + FUN2 + FUN5 ) ;
WR = / ( FUN9 + FUN16 + FUN17 + FUN18 ) ;
QX = / ( FUN0 + FUN1 + FUN5 + FUN9 + FUN16 + FUN17 +
         (FUN18 * RDY) + (FUN2 * RDY)) ;
```

Figure 2: Original PEEL Code.

RE:

- !((! F1 + ! F2) * (F1 + ! F4) * ! F8 * ! F16 * N)

WR:

- !((! F1 + ! F2) * (F1 + ! F8) * ! F4 * (! F8 + ! F16) * (F8 + F16) * N)

QX:

- !((! F1 + ! F2) * (F1 + ! F4) * (F1 + ! F8) * (! F2 + RDY) * (! F4 + ! F8) * (! F4 + ! F16) * (! F8 + ! F16) * N)

Figure 3: Simplified Code.

BOARD DESIGN

After finalizing the conceptual design, work on the board began. The original board design (Fig. 4) did not run the full length of the card slot, requiring additional labour to install the operational indicators on each card, this decision was made due to the cost of PCBs at the time of the original design process. Because of the decrease in PCB cost the decision was made to expand the board so that it would be full length, (Fig. 5) so that the assembly process is simplified by eliminating the need for any wiring work. The elimination of wiring in the design helps reduce the number of failure points in the design. Additionally, the simplification of the assembly process reduces the time and labour required to build the cards, further reducing the cost.

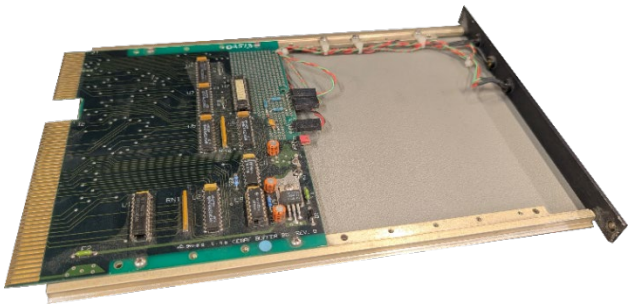

Figure 4: Original Buffer Card Design.

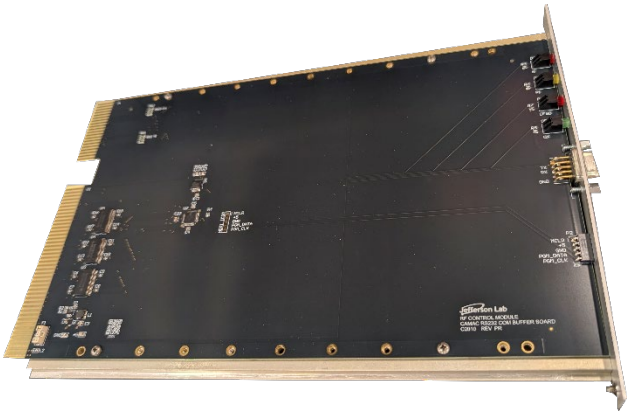

Figure 5: Updated Buffer Card Design.

TESTING

Once the bord design had been finalized, a prototype run of boards was ordered. Upon receipt of the prototype boards initial testing was run in the test lab to ensure the design functioned as intended. The testing involved ensuring the board is the proper size for the CAMAC crate, it powers up when the operating voltage is applied, the microcontroller functions as intended, the commands are received and interpreted correctly, and that the data is transferred from the CAMAC bus to the RFCM. Once the prior testing was completed the new buffer cards were left running in the test stand for a burn-in period to ensure there were no latent issues with the design. After completing the burn-in period one zone in the machine had its legacy cards swapped out for the new revision, this final test definitively proved that the design is a fully functional drop-in replacement for the legacy buffer cards.

CONCLUSION

This update to components in the Legacy RF system has mitigated a potential system failure that would prevent proper operation of CEBAF. The updated design replaces obsolete and aging hardware with new hardware, extending the serviceable life of this particular system. Modifications to the design introduced greater debugging capabilities and simplified the assembly process. This upgrade to the buffer card eliminates a single point of failure component and shows promise in the extension of the operable lifetime of CEBAF's legacy systems.

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