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DESIGN AND DEVELOPMENT OF AN UPGRADED FAST ORBIT FEEDBACK SYSTEM FOR NSLS-IIU

S. Kongtawong[*,1,2], K. Ha[1], Y. Hidaka[1], G. Wang[1], Y. Tian[1], T. Shaftan[1]
[1]National Synchrotron Light Source II, Upton, NY, USA
[2]Synchrotron Light Research Institute, Nakhon Ratchasima, Thailand

Abstract

As light source facilities evolve, upgrading fast orbit feedback systems is essential for improving beam stability. NSLS-II is planning an upgrade to NSLS-IIU, which introduces stricter stability requirements for advanced experiments. To address this, we developed a next-generation fast orbit feedback prototype system to enhance noise suppression and extend control bandwidth beyond 1 kHz. A system-wide evaluation was conducted, covering beam position monitors, cell controllers, power supply controllers, power supplies, and vacuum chamber effects. Latency and bandwidth bottlenecks were identified in the cell and power supply controllers. A new cell controller was designed to increase the sampling rate from 10 kHz to 31.5 kHz and reduce system latency to under 70 µs. The transfer function and gain measurements of a single-input-single-output system show a 10-dB improvement in noise suppression and an extension of bandwidth into the kHz range. We present the development and performance results of the upgraded system, offering a path toward higher beam stability at NSLS-IIU.

INTRODUCTION

Recent upgrades and new synchrotron light source facilities around the world are pushing toward significantly lower emittance. NSLS-II is planning an upgrade to NSLS-IIU, which will reduce the horizontal emittance to as low as 23 pm·rad at 3 GeV or 42 pm·rad at 4 GeV [1,2]. With the resulting beam size reduction, maintaining high electron beam orbit stability becomes increasingly critical for operational performance.

In addition to minimizing sources of mechanical and environmental vibrations, NSLS-II aims to enhance the performance of its fast orbit feedback (FOFB) system by increasing both suppression gain and feedback bandwidth. The current FOFB system operates with a unity-gain bandwidth of approximately 300–350 Hz [3]. The upgrade targets extending this bandwidth into the kilohertz range, in line with trends at other advanced facilities [4–6].

This paper presents the design and development of new digital processing components, along with experimental results. We demonstrate that, even with the existing power supplies and vacuum chambers, a unity-gain bandwidth exceeding 1 kHz can be achieved.

* skongtawong@bnl.gov

SYSTEM CHARACTERIZATION AND DESIGN SPECIFICATIONS

We began by re-evaluating the latency and transfer function of the existing FOFB system to validate a dynamic model developed for NSLS-II. The FOFB system architecture, shown in Fig. 1, consists of several components, with performance primarily limited by the digital processing latency of the cell controller (CC) and the bandwidth of the corrector power supplies. The system currently supports 240 beam position monitors (BPMs) and controls up to 90 power supplies per plane.

At the core of the system, the CC receives BPM data and computes corrections using a 480×180 response matrix [7]. However, due to resource constraints in the Xilinx Virtex-6 FPGA in the CC, matrix operations are implemented sequentially rather than fully in parallel, introducing a processing delay of approximately 110 µs, making this stage the dominant latency source in the system.

In addition to processing latency, the power supply (PS) bandwidth further constrains the system. The current correctors have bandwidths of approximately 4 kHz in the horizontal plane and 1.5 kHz in the vertical plane. In 2019, upgraded power supplies with bandwidths of 6.3 kHz (horizontal) and 3.3 kHz (vertical) were developed and installed in Cells 23–28, covering one-fifth of the storage ring for testing.

To model the system behavior, we use the following transfer function:

$$G(s) = \frac{\text{Const.}}{(s + p_{\text{ps}})(s + p_{\text{chamber}})} \times \left(\frac{1 - e^{-sT_{\text{avg}}}}{s}\right)\left(\frac{1 - e^{-sT_{\text{zoh}}}}{s}\right)\exp(-sT_{\text{latency}})H_{\text{PID}} \tag{1}$$

where

- p_{ps} is the power supply pole ($2\pi \times$ bandwidth),
- p_{chamber} is the vacuum chamber pole (bandwidth 13 kHz),
- T_{avg} is the FA (Fast Acquisition) averaging time (at 10 kHz),
- T_{zoh} is the zero-order hold delay from the DAC (at 10 kHz),
- T_{latency} is the total system latency,
- H_{PID} is the digital PID controller.

To verify the model parameters, we conducted bench measurements of delay and filtering at each stage, followed by

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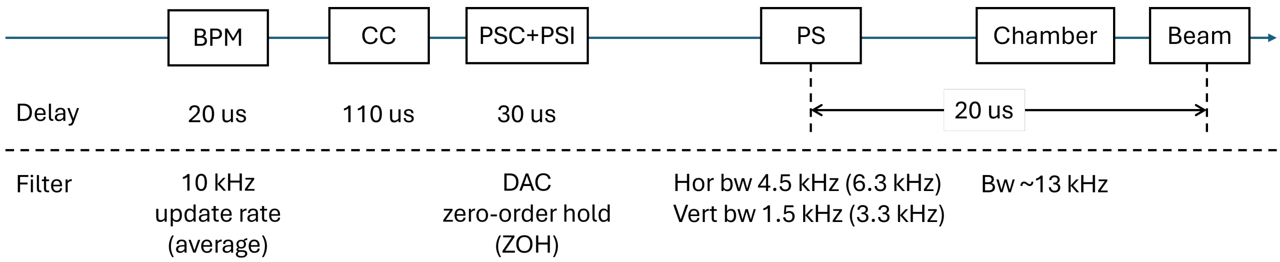

Figure 1: Layout of the FOFB system at NSLS-II, showing delays and filters at each stage.

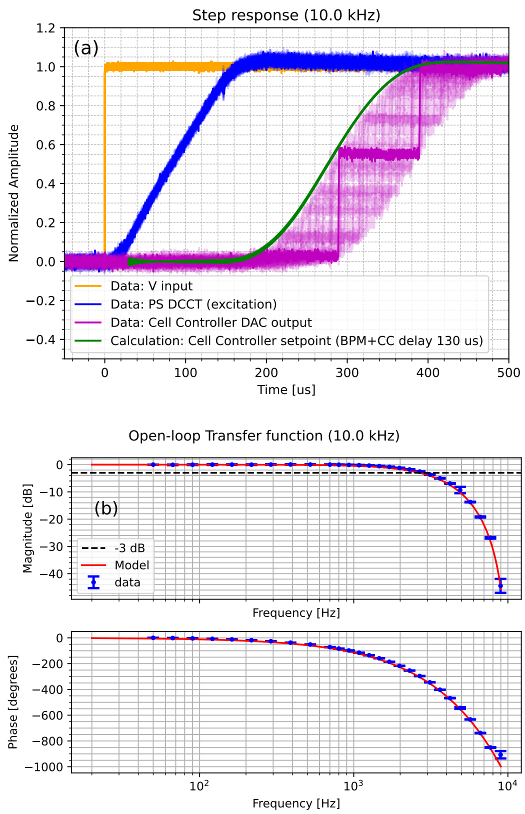

Figure 2: Comparison between model and experimental data using the electron beam in the ring: (a) step response of the Cell Controller output, and (b) transfer function of the whole system.

step and frequency response measurements using the electron beam in the ring. The results, shown in Fig. 2, exhibit strong agreement with the model predictions. Although the model employs a simplified single-pole approximation for both the power supply and vacuum chamber, it still matches the experimental data reasonably well.

With a validated model of the existing system, we explored upgrade scenarios to achieve a unity-gain bandwidth of >1 kHz. The model indicates that reaching this target requires reducing total latency and increasing both the sampling rate and power supply bandwidth. Figure 3 compares the predicted noise attenuation for different parameters. The blue and orange curves represent the current system, showing a bandwidth of approximately 300–350 Hz. The other lines represent system responses under upgraded conditions

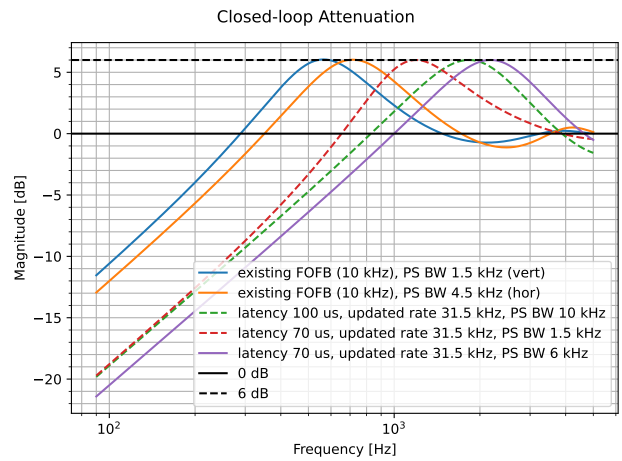

Figure 3: Comparison of noise attenuation from calculations using varying system parameters.

at an update rate of 31.5 kHz. With a total latency of 70 µs and a power supply bandwidth of 6 kHz, the system achieves a unity-gain bandwidth of 1 kHz. Additionally, the gain improves by 10 dB at low frequencies compared to the existing system.

These results suggest that a practical upgrade, focused on reducing latency and improving digital throughput, could enable a 1-kHz feedback bandwidth using the existing power supplies installed on the ring.

DEVELOPMENT OF THE UPGRADED SYSTEM

We began the upgrade by developing a new cell controller. As previously discussed, the total latency of the existing system is approximately 180 µs. Our goal was to reduce it to below 70 µs. For this development, we used a Xilinx Zynq ZCU216 UltraScale+ FPGA board [8], which provides significantly greater computational resources. This enabled more operations to be performed in parallel, reducing overall processing time. Figure 4 shows the updated timing diagram for the cell controller. The processing time of the new controller is approximately 28.5 µs, a substantial improvement over the 110 µs of the existing controller. The diagram also includes the updated timing for the new power supply controller (PSC), which has reduced its delay from 30 µs to 2 µs.

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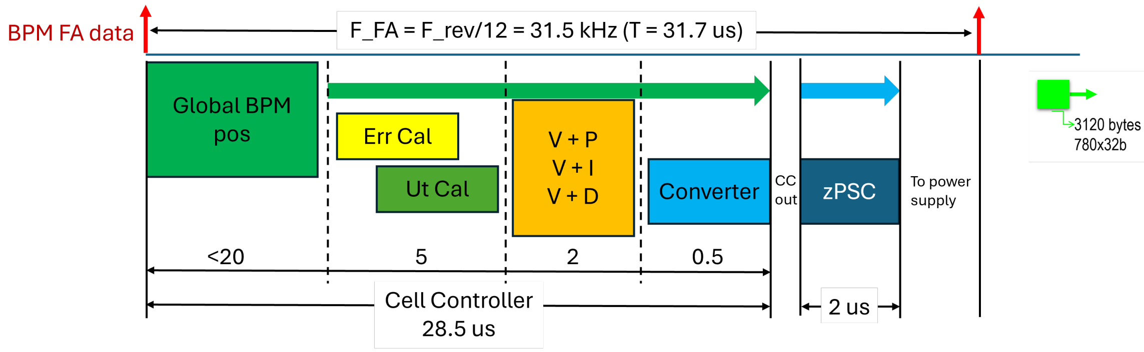

Figure 4: Timing diagram of the new Cell Controller and Power Supply Controller processing.

Another major improvement was the increase in BPM sampling rate to 31.5 kHz. This was achieved using the same Virtex-6 FPGA board as in the existing system. By reducing the decimation factor for fast acquisition data from 38 turns to 12 turns, the sampling rate was increased from 9.96 kHz to 31.5 kHz.

With these reductions in CC and PSC delays, and the assumption that other components maintain the same latency as in the existing system, the total system latency is now approximately 70 µs, meeting our design specification.

After verifying all functionalities in the laboratory, we installed the new cell controller in the storage ring for beam testing. A single BPM and a fast corrector magnet were used to demonstrate a single-input single-output (SISO) feedback control loop using the beam.

EXPERIMENTAL DEMONSTRATION AND SYSTEM VALIDATION

We conducted a SISO experiment using Cell 23 in the storage ring. This cell was selected because its power supply was upgraded in 2019, increasing the horizontal bandwidth to 6.3 kHz, which should be sufficient to achieve a unity-gain feedback bandwidth above 1 kHz. The BPM used in this test, C23P10, was modified to update at 31.5 kHz and transmit data to the cell controller.

For this experiment, global BPM data communication was not implemented. Instead, we intentionally added a 20-µs delay in the cell controller to simulate the expected delay from future global data transfers. A separate FPGA board, originally from an electrometer system, was repurposed to function as the power supply controller. It received data from the cell controller, performed digital-to-analog conversion, and drove the power supply. Additionally, a function generator was used to inject excitation signals alongside the feedback signal.

We first measured the open-loop transfer function and confirmed it matched the model. Then, we closed the feedback loop and measured the attenuation of beam motion with the feedback on and off under various excitation frequencies. The results are shown in Fig. 5, which plots the attenuation for different PI controller parameters. For an appropriately tuned PI controller, the unity-gain bandwidth

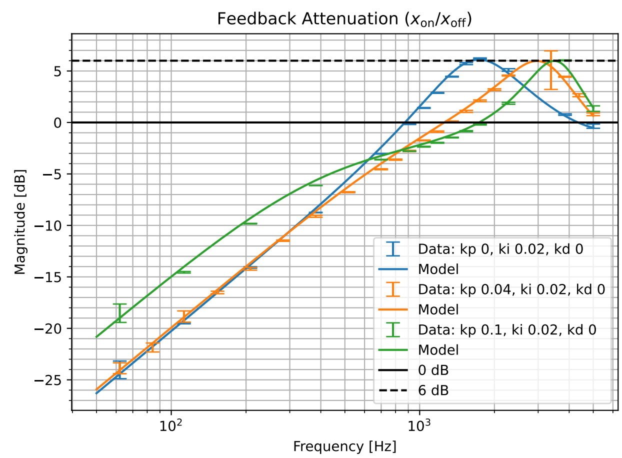

Figure 5: Measured noise attenuation with feedback on for various PI controller parameters. The plot demonstrates a unity-gain bandwidth exceeding 1 kHz with proper PI tuning.

reached approximately 1.2 kHz. Using the integral term alone, the bandwidth reached around 900 Hz. Increasing the proportional gain further increased the bandwidth but reduced overall gain. The measured results closely matched the model predictions.

These results demonstrate that the newly developed cell controller, with a reduced total latency below 70 µs and a 31.5-kHz sampling rate, is capable of achieving >1 kHz unity-gain bandwidth, even using the existing vacuum chamber, magnet, and power supply.

Future work includes improving the power supply bandwidth to exceed 6 kHz in both planes. We plan to adopt a power supply design similar to the one developed for ALS-U, which should meet this requirement. Additional efforts focus on redesigning the vacuum chamber and magnet to support bandwidths beyond 13 kHz. This involves investigating parameters such as chamber size, wall thickness, and material properties.

Global BPM data communication is also under active development. Potential topologies include a daisy-chain configuration or a star network to minimize transmission delay. We are still evaluating whether to adopt MTCA.4 or to develop a custom communication system.

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SUMMARY

This paper presents the design, implementation, and validation of an upgraded FOFB prototype system, developed to meet the tighter beam stability requirements of the upcoming NSLS-IIU light source. Latency, data update rate, and power supply bandwidth were identified as key limitations through a system-wide evaluation. A validated dynamic model indicates that achieving a unity-gain bandwidth above 1 kHz requires increasing the BPM sampling rate beyond 30 kHz and reducing total system latency below 70 µs.

To meet these targets, a new cell controller was built using a Zynq UltraScale+ FPGA board, reducing processing latency from 110 µs (for the existing Virtex-6 design) to 28.5 µs. The power supply controller delay was also reduced from 30 µs to 2 µs, while the BPM sampling rate was increased from 9.96 kHz to 31.5 kHz by adjusting the decimation factor. These upgrades lowered the total system latency to approximately 70 µs.

The upgraded system was tested in a SISO configuration in Cell 23 at the NSLS-II storage ring, which features a 6.3-kHz power supply for the horizontal plane. Feedback experiments confirmed a unity-gain bandwidth exceeding 1 kHz, with results in close agreement with model predictions.

Future work will focus on extending the power supply bandwidth beyond 6 kHz in both planes, exploring low-latency global BPM communication, and improving vacuum chamber and magnet design.

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