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OPTIMIZATION OF BEAM INTENSITY MEASUREMENT SYSTEM OF HIPA AT PSI

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Abstract

Beam intensity measurement of High Intensity Proton Accelerator (HIPA) at PSI mainly consists of several passive cavity type monitors and corresponding electronics. New VME electronics were designed to replace the old CAMAC ones. The VME system is suffering significant temperature-dependent drift, leading to an inaccurate measurement. Many compensation schemes were considered to address this issue and eventually achieving a temperature coefficient 166 ppm/degree for RF test signal. Furthermore, the new electronics incorporate a phase measurement of the 50.6 MHz proton bunches for beam energy monitoring, which greatly facilitates the commissioning and status monitoring of the accelerator.

INTRODUCTION

The HIPA can generate up to 1.4 MW continuous proton beam. The proton beam is accelerated from a Cockcroft-Walton source followed by two cyclotrons: the so-called Injector 2 cyclotron accelerating the beam from 870 keV to 72 MeV and the so-called Ring cyclotron further accelerating to 590 MeV [1].

The beam intensity measurement system of HIPA consists of many beam current monitors mounted on the different beam transport line for beam current measurement and transmission calculation, the overall layout can be found in Fig. 1.

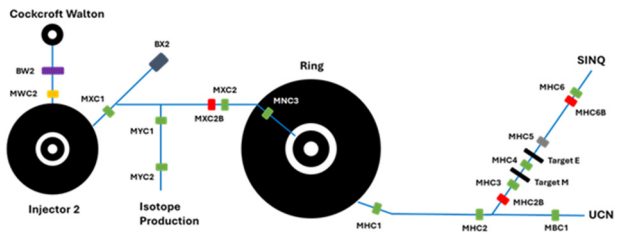

Figure 1: Layout of the beam current monitors of HIPA.

MWC2 located in front of Injector2 is measuring the DC 870 keV proton beam coming from the Cockcroft Walton ion source. MXC1/2 and MNC3 are located in the beam line from Injector2 to Ring and MYC1/2 in the Isotope Production line for the 72 MeV/50.63 MHz CW beam current measurement. MHC1-6 and MBC1 are mounted after the Ring for high energy (590 MeV) beam current measurement.

There are also 3 Bergoz current monitors, which measure the current in absolute way, running as a reference for the other beam current monitors. Beside the Bergoz monitor, beam dump e.g., BX2 can also provide the absolute beam intensity value for calibration.

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For most beam intensity monitors of HIPA (Green icon). The measurement principle is based on the use of a coaxial resonator (reentrant cavity) [2], which can be tuned to a specific resonance frequency by modifying the dimension of the capacitance gap and the inductance wall, see Fig. 2 (left). A wall current with the same time structure as the beam will be induced when the proton beam passing through the cavity. The amplitude of the magnetic field, shown in Fig. 2 (right), in the resonator is directly proportional to the beam current, a measurement of this field provides a measure of the proton beam current.

The resonator is tuned to the 2nd harmonic (101.26 MHz) of the proton beam pulse frequency. This frequency is used because of the better signal-to-noise ratio, the RF disturbance components being mainly at the odd harmonics.

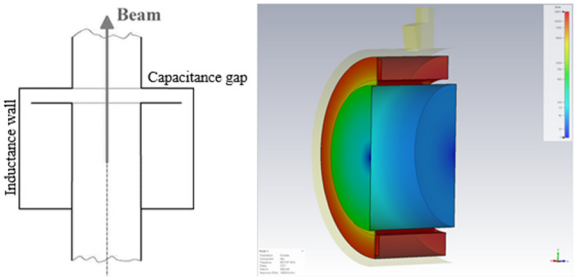

Figure 2: Measurement principle of the cavity type monitor (left); Magnetic field distribution in the cavity (right).

The signal from the monitor is brought to the electronics by using low-loss 50 Ohm cables, with lengths between 50 and 250 m. The output is further used for the transmission calculation and interlock generation when the current value is above a given limit.

DIGITAL SYSTEM DESIGN

The old CAMAC based electronics have been served for decades. A new VME based version has been developed to replace the CAMAC. The core of the new system is digital electronics based on a VME card IFC1210 from Ioxos company as presented in Fig. 3.

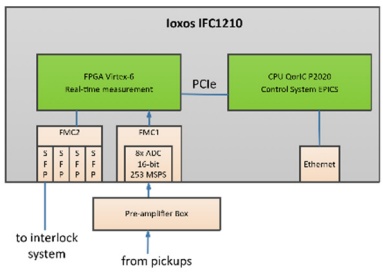

Figure 3: Block diagram of the digital electronics.

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The card has two FMC slots and both are in use. One FMC ADC3110, also from Ioxos, contains eight 16-bit ADC channels sampling at 253 MHz. The sampling clock is synthesized from the machine reference clock of 50.6 MHz. The second FMC slot is occupied by a quad SFP card FM-S14 from Faster Technology. This card provides optical interface to multi-gigabit transceivers (MGT) used in FPGA for communication with an interlock system. The real-time signal processing is performed in a large FPGA chip Virtex-6 from AMD/Xilinx. In addition, the base board is equipped with a CPU running Linux and control system EPICS. The control software communicates with the FPGA over PCIe from one side and with client applications over Ethernet on the other side.

The digital signal processing of the analog signals is implemented in the FPGA because of the hard real-time requirement for generation of interlock signals. The block diagram of the FPGA firmware is presented in Fig. 4.

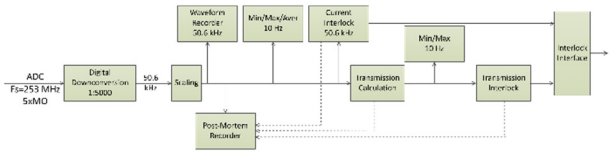

Figure 4: Block diagram of the signal processing in FPGA.

The pickup signal of 101.26 MHz is sampled with 253 MHz and mixed digitally down to base band and further filtered in multiple stages composed of CIC and FIR filters and decimated by factor of 5000 down to rate of 50.6 kHz. This frequency is used for further processing and generation of the interlock signals. After down conversion the signal is scaled to physical units of microamps, which reflects the current of the beam. The whole computation path described so far is repeated for every of twelve current measurements.

One of the crucial purposes of the system is to protect the machine against too much current or too many losses based on the transmission calculation. The FPGA firmware compares the current and transmission measurements with pre-defined thresholds and generates interlock signals, which are sent over MGT links to the interlock system. In reaction to the interlock signals, the interlock system activates the beam shutter. In addition, the interlock system monitors if the MGT link is active and in case of transmission interruption, the beam shutter is activated as well.

FPGA firmware also offers several functions which provide interface to the control system and for debugging purpose. The current and transmission signals are continuously recorded as waveforms with an update rate of 50 kHz and transferred periodically to EPICS at 10 Hz. With this feature, one can analyse the quality of the down converted signals. In addition, the firmware computes statistical values of each signal such as min, max and average also with 10 Hz update rate. These values are presented to the system users. For catching of special events there is implemented a so-called post-mortem recorder. The post-mortem recorder has several options, which allow triggering on signal level or interlocks. In case of a trigger, the recorder collects data over more than 1 second of all current and transmission signals. It also collects samples before the trigger, which is a very useful feature to analyse how the signals develop until an exception occurred. The complementary control system EPICS runs on the same board in the CPU. EPICS provides to the user graphical interfaces, which allow to set and read every register and memory from the firmware.

TEMPERATURE STABILIZATION

A modular approach is applied for signal amplification before the analog-to-digital conversion. The pre-amplifiers are mounted into a 19-inch rack unit with 20 channels, as depicted in Fig. 5 (top). External low-pass filters, used to prevent aliasing, are mounted on the installed boxes. The Amplifier ZX60-P103LN+ from Mini Circuit, with gain of 25 dB, is used. It has an excellent noise figure, and good linearity. However, as for other RF gain blocks, its gain is susceptible to temperature. Therefore, temperature stabilization measures are taken within the unit to reduce the temperature drift caused by the preamplifier. Figure 5 (bottom) shows the temperature control chain. The amplifiers are mounted on a solid aluminum block. The temperature of this Aluminum block is controlled by two power resistors on its rear side. The control is done by a Meerstetter TEC controller with a PI feedback loop. The controller has a maximal power delivery of 80 W. A PT100 mounted on the Aluminum block provides the temperature feedback. The controller is connected to the network through a custom ethernet to serial PCB and can therefore be configured and supervised by EPICS.

Figure 5: Pre-amplifier (top) and its temperature control unit (bottom).

The temperature stabilization of the amplifiers was tested in a climatic chamber. The beam signal is emulated with a signal generator at 101.26 MHz. The temperature of the Aluminium block is regulated to 50 °C. The signal is carried into the climatic chamber, where it is amplified by the pre-amplifier rack unit. The amplitude of the output signal is then measured by the VME System out of the climatic chamber. Figure 6 shows the resulting beam current drift when the temperature is cycled from 25 °C to 45 °C, with roughly 2 hours step size. The same range of temperature are to be expected in the racks where the modules are

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installed. The output values are normalized to the nominal HIPA beam current of 2000 µA. One channel of the temperature-controlled 19-inch rack unit was measured, simultaneously to a channel in a different rack unit without temperature control.

The resulting readings of the measurement shown in Fig. 6 is summarized in Table 1. The temperature stabilization reduces the drift from -1.4 µA/°C to only -0.3 µA/°C, which is a factor larger than 4. The remaining drift is partly coming from the cabling and the connectors inside the climatic chamber that are not temperature stabilized.

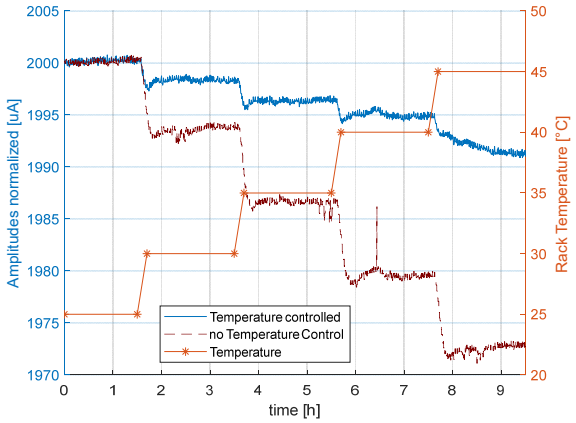

Figure 6: Gain drift of pre-amplifiers with/without temperature stabilization.

Table 1: Beam Current Drift Caused by Pre-amplifier with and without Temperature Stabilization

	25°C [µA]	40°C [µA]	Drift [µA /°C]
With T.S.	2000	1995	-0.3
Without T.S.	2000	1979	-1.4

The interior of the pre-amplifier unit is depicted in Fig. 7. It is based on a 2-height unit Elma standard enclosure, with customized front panel, rear panel and mounting tray. The temperature-controlled aluminum block is held by two FR4 plates to ensure thermal insulation to the housing.

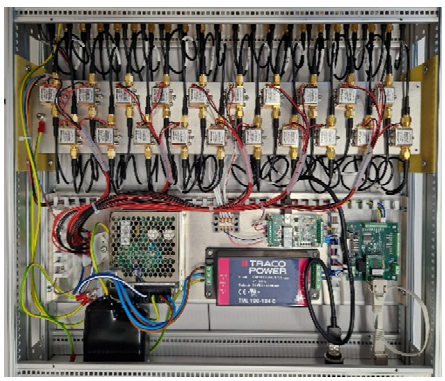

Figure 7: Inside of the pre-amplifier box, the low-noise amplifiers are mounted on an aluminum block.

NEW FEATURE

The VME system provides not only beam intensity but also phase information. This enables the extraction of the proton beam energy from Injector 2 using the time-of-flight (TOF) method, by employing a pair of current monitors along the IW2 line, such as MXC1 and MXC2. The same approach can also be applied to the high-energy beam transport line downstream of the Ring.

There are two phase delays to be considered during the calculation, cable delay and electronic delay. The cable phase delay can be easily calculated out by measuring the cable length. The phase delay of each electronics channel can not be determined, but the phase difference between two channels can be approached by swapping the input signals at the input ports of the electronics.

Assuming φ1 and φ2 are the measured phase value from two current monitors,

$$\varphi_1 = \varphi_{I1} + \varphi_{D1},$$

$$\text{and } \varphi_2 = \varphi_{I2} + \varphi_{D2},$$

where φ_{I1} and φ_{I2} are the phase at the input ports of each electronic channels, φ_{D1} and φ_{D2} are the phase delay caused by the electronics. The phase difference between these two current monitors shows as follows:

$$\varphi_2 - \varphi_1 = \varphi_{I2} - \varphi_{I1} + \Delta_\varphi,$$

where $\Delta_\varphi = \varphi_{D2} - \varphi_{D1}$ is the phase difference between electronic channels. After swapping the cables at the input ports of the electronics, one can have:

$$\varphi_2 - \varphi_1 = \varphi_{I1} - \varphi_{I2} + \Delta_\varphi.$$

Then the phase difference between electronic channels can be calculated out:

$$\Delta_\varphi = \frac{(1) + (2)}{2}.$$

The measured beam energy after Injector2 with respect to the beam intensity can be found in Fig. 8, the accuracy of the measurement is better than 1 %.

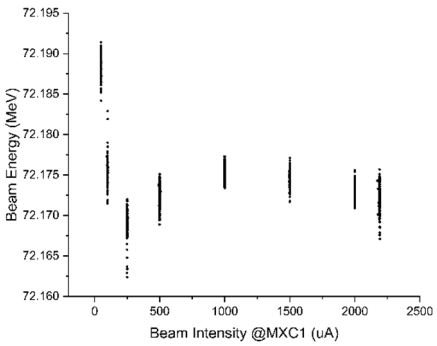

Figure 8: Injector 2 beam energy measured under different beam intensity.

CONCLUSION

After a successful commissioning and beam testing of the whole system. The VME electronics have been deployed in August 2025, it shows a stable performance on beam intensity and energy measurement.

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