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UPGRADE OF THE BPM PROCESSOR FOR SXFEL*

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Abstract

The Shanghai Soft X-ray Free Electron Laser (SXFEL) is scheduled for a digital and intelligent upgrade over the next two years, aiming to achieve fully autonomous operation. This upgrade requires timestamping the BPM measurement results in the beam diagnostics system to enable synchronous acquisition of all measurement data at SXFEL. A new prototype of the digital BPM signal processor (DBPM) has been developed based on a Zynq UltraScale+ MPSoC FPGA. In addition to high-speed data connectors for the ADC board, the design features an FMC slot to accommodate a White Rabbit timing board for receiving bunch ID and trigger signals as timestamps. It also includes 10 GB SFP ports to support high-speed data transmission between processors. In this paper, the design of the hardware, firmware, and software of the upgraded BPM signal processor is presented.

INTRODUCTION

SXFEL, located on the campus of the Shanghai Synchrotron Radiation Facility, has an overall length of 532 m, comprising a linear accelerator tunnel of approximately 250 m, a 40 m beam distribution hall, a 160 m undulator hall, and an 80 m section housing the beamlines and experimental stations [1]. The electron beam energy reaches up to 1.5 GeV, with a maximum bunch charge of 0.5 nC. The photon energy can reach 620 eV, and the beam repetition rate is adjustable between 10 and 50 Hz [2].

At SXFEL, more than one hundred beam position monitors (BPMs) are distributed along the facility, including stripline BPMs and cavity BPMs. The stripline BPMs achieve a resolution better than 10 μm, while the cavity BPMs reach a resolution of 1 μm [3]. The processors and racks currently in operation are shown in Fig. 1 and Fig. 2, respectively.

In the currently operating BPM processors, the absence of timestamps for individual bunches prevents synchronous data acquisition, making machine-learning-related studies impossible. In the processors at SHINE, White Rabbit timing signals have been integrated, enabling synchronized acquisition of measurement results [4] and supporting high-repetition-rate hard X-ray free-electron laser output [5]. The White Rabbit card is shown in Fig. 3. The WR system provides sub-nanosecond time synchronization while simultaneously distributing trigger signals and bunch identification (Bunch ID) information required for accelerator operation. Using these timing references, multiple BPM processors can acquire data under a unified time base and accurately associate measurements with the corresponding bunches, thereby enabling high-precision alignment among different processors.

SXFEL is undergoing a digital and intelligent upgrade. According to project requirements, the SXFEL processors are to be upgraded, with completion targeted within two years. The proposed solution employs the same system-on-chip FPGA while maintaining compatibility with the existing ADCs and front-end boards. It also supports the integration of a White Rabbit timing mezzanine card and provides high-speed SFP interfaces for data transmission. Furthermore, associated FPGA logic, signal processing algorithms, and EPICS IOC control software will be developed. The prototype hardware has been successfully constructed, incorporating both the stripline BPM signal processing algorithm and the EPICS IOC. In addition, White Rabbit timing data can now be acquired.

Figure 1: Current BPM processor.

Figure 2: BPM processor rack.

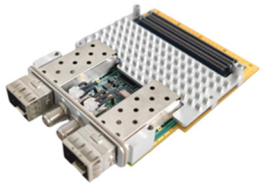

Figure 3: White Rabbit card.

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NEW PROCESSOR DEVELOPMENT

Hardware Design

The current BPM processor employs Virtex-5 as the core chip, using an FPGA+ARM architecture as the main platform. Furthermore, the overall hardware resources are limited, which does not support the integration of a White Rabbit timing module or high-speed SFP interfaces. Its hardware architecture is shown in Fig. 4.

The new BPM processor developed for SXFEL adopts the Zynq UltraScale+ MPSoC as its core platform, integrating four ARM Cortex-A cores and high-performance programmable logic (FPGA). The processor board provides abundant hardware resources: 8 GB of DDR memory is configured on the programmable logic (PL) side, and 4 GB of DDR memory is available on the processing system (PS) side for buffering raw ADC data and processed results. In addition, the board supports multiple interfaces, including two FMC connectors for attaching ADC mezzanine boards and the White Rabbit timing module, an RJ45 connector for Ethernet communication, a 10 GB SFP+ port for high-speed data transfer, as well as JTAG and SD card interfaces. The updated processor and digital baseboard structure are shown in Fig. 5, and its performance comparison is presented in Table 1.

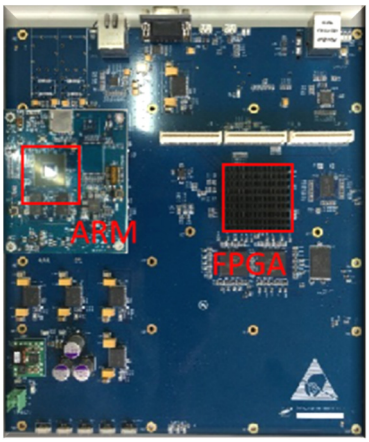

Figure 4: FPGA carrier board at SXFEL.

Figure 5: New carrier board and new processor.

Table 1: Performance Comparison

Indicator	Virtex5 (Old)	XCZU15EG (New)
Hardcore ARM	0	4xCortex-A53
LUT	28800	341280
FF	28800	682560
DRAM	480 kB	11.3 MB
BRAM	2160 kB	26.2 MB
DSP	48	3528
UBRAM	0	31.5 MB

The processor mezzanine cards are of two types. One includes only ADC acquisition, while the other integrates ADCs along with a front-end composed of band-pass filters, amplifiers, attenuators, etc. The board features four independent analog input channels with 16-bit resolution, supporting sampling rates up to 125 MHz and an analog bandwidth of up to 650 MHz. Data communication between the mezzanine board and the FPGA is implemented via the FMC HPC connector, with high-speed transmission achieved through LVDS signaling. Table 2 summarizes the overall specifications of the processor.

Table 2: Processor Specifications

Parameter	Value
Channels	4
Bandwidth	650 MHz
ADC bits	16
Max ADC rate	125 MHz
FPGA	Xilinx ZU15EG
Clock	Ext./Int.
Trigger	Ext./Self/Period
PL DDR	8 GB
PS DDR	4 GB
SFP	2 UDP, 2 Aurora
Interlock	Lemo
Software	Arm-Linux/EPICS

Firmware Design

The overall architecture of the SoC FPGA is shown in Fig. 6. The ADC samples four analog input channels, and the acquired signals are processed to determine the beam position information. To achieve high-throughput data processing, the signal processing is performed on the FPGA side. The signal processing flow of the stripline BPM is illustrated in Fig. 7. After compensation of the four-channel input data, the signals are squared, summed, and square-rooted, and the beam position information in the x and y directions is finally obtained using the difference-over-sum algorithm.

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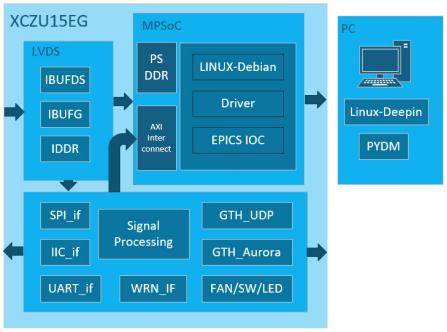

Figure 6: Software architecture of the processor.

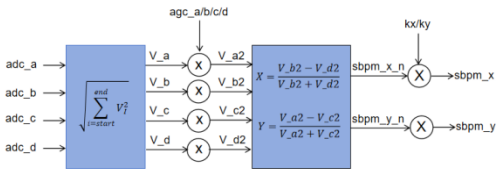

Figure 7: Signal processing flow of the stripline BPM.

Software Design

On the ARM side, a Linux-Debian operating system is deployed to facilitate file management and data communication. In addition, a PyDM user interface was developed based on the EPICS Base 7.0.7 framework. On the PS side, an IOC process is implemented using the Asyn support package and managed with procServ. Interaction between the user interface and the underlying hardware is achieved through PV variables. The system supports automatic startup at boot, time synchronization via Chrony, parameter delivery, status monitoring, and dynamic visualization of signals and result waveforms.

LAB TESTS

Laboratory tests were carried out on the upgraded BPM processor prototype. First, the EPICS-based user interface integrated in the processor is shown in Fig. 8. This interface enables parameter configuration, waveform display of ADC data, and visualization of the calculated beam position results.

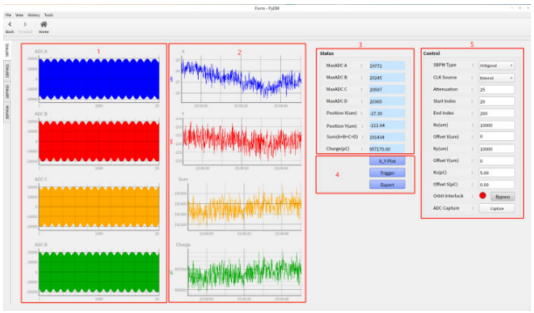

Figure 8: EPICS user interface.

Subsequently, a 500 MHz sine wave was used as the input, with a 119 MHz external clock and a 10 Hz external trigger signal for testing. A total of 100 data sets were acquired, each consisting of 4096 points. The grouped plotting results in MATLAB are shown in Fig. 9, where all data sets exhibit identical phases, indicating that the signal source, clock, and trigger were phase-locked. Furthermore, histograms of the calculated x and y position results were obtained, as shown in Fig. 10. On the FPGA side, the functionality of timestamp data acquisition from the White Rabbit timing module was also verified using an online logic analyzer, along with data communication via the SFP interface using the UDP protocol. Finally, the position resolution was determined to meet the required specifications: 10 µm for the stripline BPM and 1 µm for the cavity BPM.

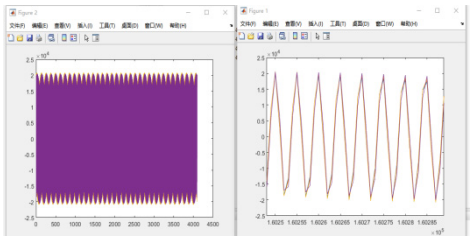

Figure 9: Phase-locked sampling.

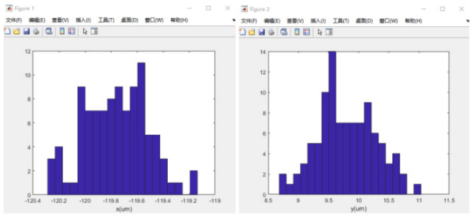

Figure 10: Position distribution histogram.

CONCLUSION

At present, the upgraded BPM prototype has completed basic testing of stripline BPM signal processing, software development, and White Rabbit timing integration. The next steps include developing signal processing algorithms for the cavity BPM, applying timestamps to the processed results, and ultimately replacing the processor without affecting facility operation.

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