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DEVELOPMENT OF ANALOG FRONT-END MODULE FOR THE BPM SIGNAL PROCESSOR AT SSRF*

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Abstract

A new BPM processor is being developed to address the ageing of BPM signal processors and the new demand for synchronised data acquisition at the storage ring of Shanghai Synchrotron Radiation Facility (SSRF). The BPM processor consists primarily of a digital carrier board and an analog front-end (AFE) module. The AFE is responsible for the conditioning of the BPM output RF signal and for the compensation of long-term drift. This paper presents the design of the AFE module and gives an evaluation of its performance. The experimental results show that the AFE module under development fully satisfies the high resolution and high stability requirements of the upgraded SSRF BPM processor.

INTRODUCTION

The Shanghai Synchrotron Radiation Facility (SSRF) is a third-generation synchrotron radiation sources that has been open to users since 2009. The main parameters of SSRF storage ring are given in Table 1.

Table 1: Parameters of SSRF Storage Ring

Parameter	Value
Energy	3.5 GeV
RF frequency	499.654 MHz
Harmonic number	720
Revolution frequency	693.964 kHz
Current (single bunch)	5 mA
Current (multi bunch)	200-300 mA

The storage ring of the SSRF consists of 20 cells and 140 BPM probes. Currently, SSRF employs the Libera Electron and Brilliance series processors for beam position measurements. However, these devices are facing ageing-related issues. To address this, an intelligent upgrade of the storage ring is planned within the next two years, requiring high-speed synchronized acquisition of beam position data across the entire ring. Consequently, the BPM processors must be upgraded to support synchronized timing information from White Rabbit timing system.

In the early stage, we developed an in-house prototype processor using which can no longer meet the present requirements[1-2]. Therefore, a new processor development has been initiated. The new processor will be based on a system-on-chip FPGA, not only reproducing the functionalities of the existing BPM processors, but also integrating White Rabbit timing information.

The RF front end plays a critical role in determining the performance of the BPM processor. By filtering, amplifying, and applying gain control to the four electrode signals from the BPM pickup, the RF front end converts them into RF signals compatible with various beam intensities, facilitating subsequent digitization and processing. In the clock subsystem, phase locking to the accelerator's 694 kHz revolution clock is achieved, followed by generation of a synchronous clock with a 169× frequency multiplication, thereby producing the pilot signal.

ELECTRONICS DESIGN

Table 2 lists the specification requirements for the AFE module at SSRF.

Table 2: Goals of AFE Module

Parameter	Value
Dynamic range	60 dB
Noise figure	<10 dB
Input power	-50 to 0 dBm
Center frequency	499.654 MHz
Crosstalk	< -50 dB
3 dB bandwidth	< 30 MHz
1 dB compression point	> 20 dBm
RMS Phase Jitter(12K-20M)	< 300 fs

Analog Module

To meet these requirements, the analog module has been carefully designed. Figure 1 presents the block diagram of the RF chain, while Fig. 2 shows a photograph of the implemented hardware.

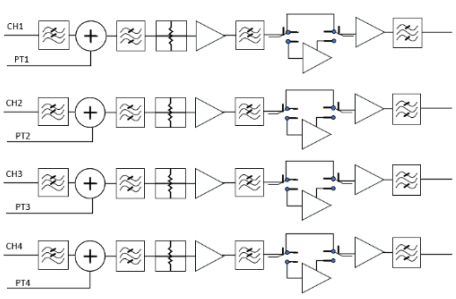

Figure 1: Analog front end block diagram.

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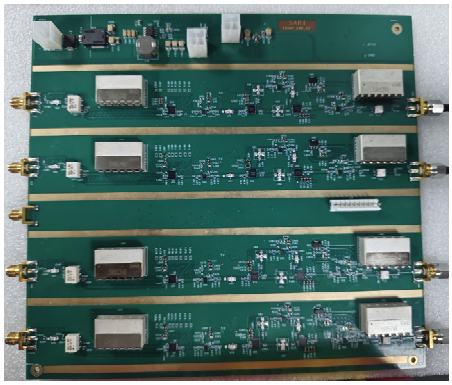

Figure2: Photograph of the implemented hardware.

The front-end circuit is similar to the one presented at IBIC 2024 [3], but has been enhanced and re-engineered by adopting a different type of bandpass filter, replacing all functional devices, and completing impedance matching. In the current version of the front end, both the pilot-tone coupling module and the conditioning module are integrated. The pilot-tone module processes the signal generated by the discrete clock module through a 1-to-2 splitter, followed by a 2-to-4 splitter, before coupling it with the beam signal. The beam signal chain mainly consists of two bandpass filters (center frequency 499.8 MHz, 20 MHz bandwidth, flatness of ±0.1 dB within ±2 MHz, and a minimum stopband attenuation of 55 dB within ±80 MHz), three amplifier stages (the third stage can be bypassed via an RF switch), and a digitally controlled step attenuator. The amplifiers are designed with low-noise and high-linearity characteristics, with specifications of: gain G = 22 dB, noise figure F = 0.5 dB, third-order output intercept point OIP3 = +37 dBm, and 1 dB compression point P1dB = +22 dBm. The attenuator provides a tuning range of 0–31.75 dB with a step size of 0.25 dB. Figure 3 shows the amplitude–frequency response of the RF chain. And the simulated overall noise figure of 6.975 dB.

Figure 3: Frequency response of analog module.

Clock Module

The AFE module also includes a clock module. The reference clock of this module is derived from the accelerator revolution frequency of 693.964 kHz. After clock debouncing and fan-out, it generates 117.284 MHz synchronized clocks for the FPGA and ADC, as well as the reference clock for the pilot-tone generator LMX2541, which produces a 501.4 MHz pilot tone. Its block diagram shown in Fig. 4, and a photograph of the implemented hardware in Fig. 5.

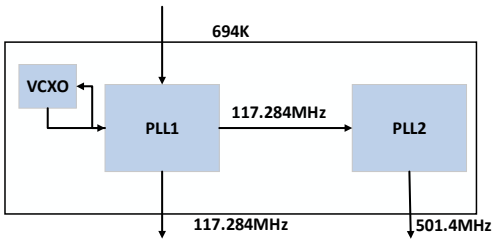

Figure 4: Clock block diagram.

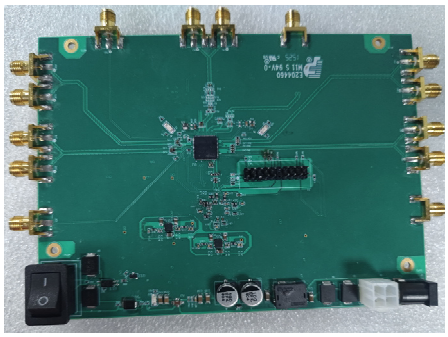

Figure 5: Photograph of the clock module.

The integrated jitter of the generated clocks and the jitter of the pilot tone was measured by using an R&S FSWP. The test results indicate that within an integration bandwidth of 12 kHz to 20 MHz, the jitter remains below 300 fs, satisfying the SSRF requirements.

PERFORMANCE TEST

Building on previous work, the digital baseboard and high-precision ADC module were developed. Based on these two modules, the AFE was subjected to resolution tests. All experiments—including TBT, FA, and SA—used a Rohde & Schwarz SMB100B signal generator to emulate the beam signal. TBT measurements allowed observation of beam dynamics on very short timescales, FA measurements provided insight into beam stability over intermediate timescales, and SA measurements reflected long-term trends, serving as a reference for evaluating overall system stability and reliability. By combining these data streams, the performance of the BPM signal processor could be comprehensively characterized, providing critical guidance for further optimization of the analog front-end, digital processing algorithms, and overall system architecture. Figure 6 illustrates the overall experimental setup.

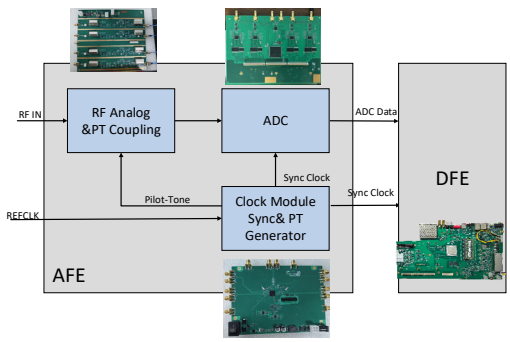

Figure 6: The overall experimental setup.

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Turn by Turn (TBT) Data

In this experiment, a −10 dBm signal at 499.67 MHz was injected into the AFE input channel to evaluate the turn-by-turn (TBT) resolution. The TBT frequency of SSRF is approximately 694 kHz, and a total of 2000 TBT data points were acquired. The measured standard deviation of the TBT data is 200.0 nm in the horizontal plane and 197.7 nm in the vertical plane, indicating that the performance meets SSRF specifications (Fig. 7).

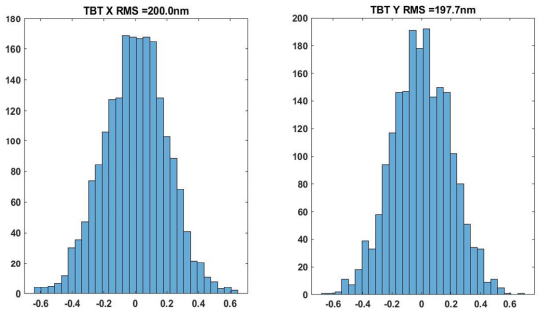

Figure 7: Position resolution for TBT.

Fast Acquisition (FA) Data

A −10 dBm signal at 499.67 MHz was injected into the four AFE input channels to evaluate the Fast Acquire (FA) resolution. The FA frequency of SSRF is approximately 10 kHz, and a total of 2000 FA data points were collected. The measured horizontal and vertical resolutions are 103.3 nm and 92.9 nm, respectively, meeting SSRF design specifications (Fig. 8).

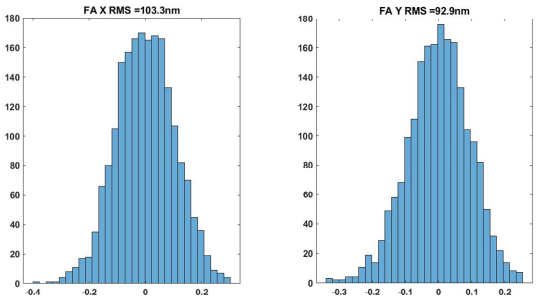

Figure 8: Position resolution for FA.

Slow Acquisition (SA) Data

During the experiment, a −10 dBm signal at 499.67 MHz was injected into each of the four channels. The position resolution was evaluated both prior to compensation (blue curve) and after compensation (orange curve). The slow acquisition (SA) frequency of SSRF is 10 Hz, and a total of 2000 data points were collected. The measured horizontal and vertical resolutions are 11 nm and 11.5 nm, respectively. During the 2.5-hour test, the measured resolutions were 25.8 nm and 72.1 nm in the X and Y directions, respectively. These results demonstrate that enabling the pilot tone improves the resolution, and the standard deviations of the horizontal and vertical positions satisfy the SSRF design specifications. We also conducted two-and-a-half-hour tests, as shown in Fig. 9. It can be observed that temperature has a decisive effect on the long-term stability of the X-axis SA measurements.

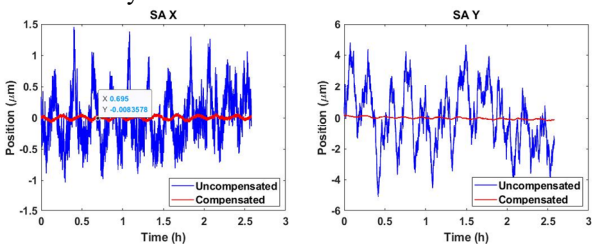

Figure 9: Position resolution for SA X.

CONCLUSION

In this work, an analog front-end (AFE) module for the BPM signal processor at SSRF was developed, integrating analog conditioning ,and clock/pilot-tone generation functionalities.Laboratory tests, including Turn-by-Turn (TBT), Fast Acquire (FA), and Slow Acquire (SA) measurements, demonstrated that the AFE module meets SSRF's high-resolution and high-stability requirements, achieving position resolutions of 200.0 nm (horizontal) and 197.7 nm (vertical) for TBT, 103.3 nm and 92.9 nm for FA, and 11 nm and 11.5 nm for SA(2000 data points), 25.8 nm and 72.1 nm (2.5 hours)respectively. The SA results indicate that although the pilot tone provides effective compensation, small residual drifts persist under laboratory temperature cycles. Future work will focus on further optimizing the front-end design to mitigate the impact of temperature on long-term stability. The developed system is scheduled for deployment at the SSRF storage ring to replace aging Libera processors, and ongoing efforts focus on optimizing digital processing algorithms and system integration to maintain performance under varying beam conditions.

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