ISBN: 978-3-95450-262-2 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2025-MOPCO12

FIRST BEAM COMMISSIONING EXPERIENCE WITH RF SYSTEM-ON-CHIP-BASED BUNCH-BY-BUNCH SIGNAL PROCESSING SYSTEM AT SLS 2.0

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Abstract

After a dark time of 15 months, the new diffraction limited storage ring SLS 2.0 had first beam in January 2025. In April 2025, the nominal beam current of 400 mA was reached. In this contribution, we present the status and first beam commissioning experience with the RF System-on-Chip (RFSoC) based signal processing systems of the new SLS 2.0 ring. RFSoCs integrate several fast multi-GSample/s ADCs and DACs, FPGA (programmable logic) fabric and multi-core CPUs all on the same chip. During SLS 2.0 commissioning, the integrated EPICS IOC of the RFSoCs provided bunch-by-bunch diagnostics of dedicated BPM position and charge readings. Integrated DACs are driving newly developed transverse and longitudinal kicker magnets, enabling bunch-by-bunch excitation and damping. Bidirectional multi-Gigabit fiber optic links connect the RFSoC to the event system master, thus enabling both synchronisation of the RFSoC to the event system, as well as real-time control of the event system master by the RFSoCs, e.g. for control of beam injection timing and filling pattern.

INTRODUCTION

The Swiss Light Source (SLS), the 3rd generation light source at Paul Scherrer Institut (PSI), began user operation in 2001. After more than two decades of successful operation, SLS was decommissioned in September 2023. Between September 2023 and December 2024 (the "dark time"), the storage ring was replaced by the new diffraction-limited storage ring of the SLS 2.0 upgrade project. The new ring features a lower emittance and an increased beam energy of 2.7 GeV, providing up to 60-fold higher brightness for hard X-ray users to ensure competitiveness with other state-of-the-art facilities. Commissioning of SLS 2.0 started in January 2025. By mid-2025, the main performance goals of the storage ring had been achieved [1], paving the way for the first pilot user experiments in July 2025. As part of the SLS 2.0 upgrade, RFSoC-based signal processing systems were introduced, replacing ageing VME-based electronics and providing feedback systems: The multi-bunch feedback (MBFB), the filling pattern feedback (FPFB), as well as diagnostics tools such as coupled-bunch mode (CBM) instability monitoring, bunch-by-bunch beam arrival-time measurement, and charge monitoring. The feasibility and development of these systems with the RFSoC were previously demonstrated in [2, 3] and they have now been deployed in the upgraded storage ring. This contribution reports on the status of the RFSoC-based systems in the upgraded machine and presents results from the first six months of commissioning.

RFSOC-BASED SYSTEMS

The hardware set-up of the RFSoC-based processing systems at the SLS 2.0 storage ring is built around the AMD ZCU111 evaluation board, which we packaged in a 19″ enclosure together with two in-house developed add-on cards and referred to as the RFSoC-box. One add-on card provides control of a separate RF front-end (RFFE) and a fast beam-dump controller (BDC), while the other breaks out the 8 ADC and 8 DAC channels of the RFSoC via SMA connectors. The ZCU111 incorporates a first-generation Xilinx Zynq UltraScale+ RFSoC, integrating multi-GS/s ADCs and DACs, FPGA programmable logic, and two multi-core ARM CPUs: A quad-core 64-bit application processing unit (APU) and a dual-core real-time 32-bit processing unit (RPU). In this configuration the device offers eight 12-bit ADCs at 4.096 GS/s and eight 14-bit DACs at 6.5 GS/s. In the present setup, three RFSoC-boxes are deployed: one dedicated to the FPFB (including bunch arrival-time and bunch charge measurement), one to the transverse MBFB, and one to CBM diagnostics. This modular approach was chosen for initial operation to simplify development, where integration of MBFB and advanced diagnostics on a single RFSoC is planned [2]. Signals from four capacitive BPM buttons are conditioned in an RF hybrid network, generating a sum signal (S), proportional to bunch charge, and a difference signals (X, Y), proportional to horizontal and vertical bunch offsets times bunch charge. These signals are connected to an external RFSoC RFFE box that provides digital step attenuators (DSAs) and RF amplifiers. With ~1 GHz bandwidth, three analogue conditioning paths enables on-line user-controllable gain/attenuation adjustments, providing overvoltage protection for the RFSoC data converters, and allowing independent channel on/off switching. For the FPFB, the sum signal S is directly sampled at approximately 4 GS/s and processed in real-time by the RFSoC's RPU, enabling bunch-charge and arrival-time diagnostics as well as execution of the feedback algorithm. A dedicated bidirectional 2.5 Gbit/s optical fiber link between the FPFB and the event system master (EVM) closes the FPFB loop, with the RFSoC transmitting and receiving information to control beam injection timing and thus the filling pattern. In addition, the FPFB is connected to a second optical link from the EVM carrying event codes. These are decoded by an embedded event receiver (EEVR) in the programable logic (PL), synchronizing both the FPFB and the MBFB system with the SLS 2.0 event system. In contrast to the FPFB, which directly samples the BPM sum signal, the MBFB still relies on analogue down-conversion at the current stage of commissioning, while direct sampling is foreseen for future operation**.** Before digitization in the RFSoC, the

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X, Y, and S signals are downconverted from 1.5 GHz to baseband using a commercial RFFE originally employed in SLS 1.0. The RFFE output signals are processed at 500 MS/s in the RFSoC PL to realize the low-latency three-plane MBFB algorithm [2], and the RFSoC DACs generate correction signals that close the feedback loops. In the transverse planes, the correction signals are amplified to drive the new kicker magnets already in operation at SLS 2.0. In the longitudinal plane, the feedback is not yet active. A new 1.875 GHz MBFB longitudinal kicker cavity, designed for the smaller SLS 2.0 beam pipe, together with the direct-driving approach presented in [3] using I and Q outputs from two DAC channels at 3.75 GS/s to feed longitudinal amplifiers, has been tested and validated and is planned to be implemented in the near future. The communication between the RFSoC systems and the SLS 2.0 control system is provided via Ethernet. EPICS IOC runs on the RFSoC APU, supporting feedback parameter configuration and data retrieval for high level applications such as CBM monitoring and arrival time measurement, both using 4 GS/s data.

Multi-Bunch Feedback (MBFB)

The SLS 2.0 booster and storage ring main RF operates at ~500 MHz and ~2 ns bunch spacing, with harmonic numbers of 450 for booster and 480 for the ring. At a sampling rate of ~4 GS/s (8 times the RF frequency), a single RFSoC ADC provides eight samples per bunch. The present MBFB firmware uses one ADC per plane, streaming eight parallel samples into the PL. By selecting the sample closest to the bunch-pulse peak, the processing rate is reduced to 500 MS/s, analogous to the previous SLS 1.0 system. We realized the MBFB algorithm entirely in VHDL, including the low-latency digital filters with reconfigurable taps, adjustable gain, and tuneable latency (2 ns steps with 250 ps fine adjustment), as well as DDS-based multi-bunch excitation, allowing controlled excitation of selected bunches for diagnostics.

Filling-Pattern Feedback (FPFB)

The FPFB firmware acquires the BPM sum signal (S) from a single RFSoC ADC at ~4 GS/s, using fractional-frequency sampling with 16-turn interleaving for an effective ~64 GS/s rate. ADC acquisition is handled in the PL, while interleaving, charge and arrival-time evaluation, and feedback calculation run in C on the RPU. Bunch charge is calculated from the negative pulse area and arrival time from the area midpoint, generating an injection list that prioritizes injection into bunches with the largest negative deviation from a user-defined filling pattern. Bunch-charge data is simultaneously available from two redundant sources: From the BPM-based RFSoC system itself, and from an external cPCI-Serial photon-based Filling Pattern Monitor (FPM) connected via a Gigabit fiber link. The injection bunch number list is transmitted over another bidirectional multi-gigabit fiber link to the EVM for injection control. Besides the feedback-driven mode, an alternative feedforward mode allows applying a user-defined injection list directly. Individual bunch charges are continuously monitored, and if a threshold for the maximum allowed single-bunch charge is exceeded, a beam-dump request is sent to the BDC within 10 µs to protect the accelerator. The feedback routine executes in ~180 ms, thus meeting FPFB requirements for the 320 ms top-up cycle.

STATUS AND RESULTS

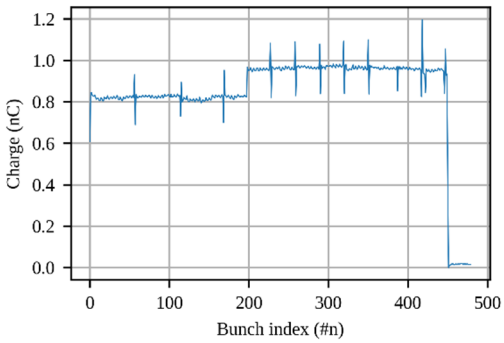

Figure 1: RFSoC-based BPM bunch charge at 400 mA, with 450 bunches filled and a 30-bunch gap.

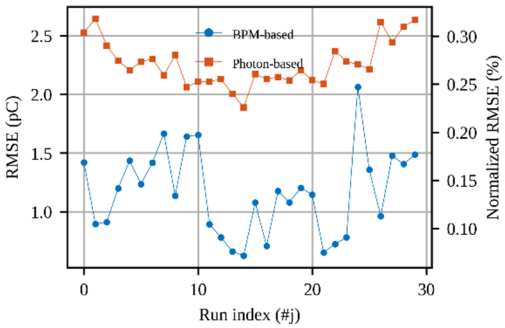

Figure 2: Comparison of bunch charge measurement resolution: RFSoC BPM-based (blue, no averaging) versus photon-based FPM (red, average over 32 acquisitions).

From the first commissioning stages up to the nominal 400 mA, the RFSoC-based system reliably measured bunch charge and arrival time, while also providing a safety function by monitoring individual bunch-charge and triggering the BDC when thresholds were exceeded. Figure 1 shows a typical filling pattern with 450 bunches and a 30-bunch gap. The charge step in the bunch train results from accumulation in feedforward mode, where injection stops at the target current of 400 mA and resumes once it falls below. Although the FPFB loop was successfully closed during recent beam tests, EVM IOC issues in interpreting the injection list and handling the gun trigger delay still prevent achieving a perfectly flat filling pattern. The bunch-charge spikes in the plot illustrate the problem, where the first bunch of the list is skipped, and the next one is injected twice. Figure 2 compares the RFSoC-based system with the complementary photon-based FPM, which was introduced at a later stage of commissioning, weeks after first beam. The photon-based FPM uses a fixed average over 32 acquisitions, while the RFSoC provides a configurable moving average. The RFSoC results shown are without averaging, yet the RFSoC already outperforms the

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FPM, with RMSE deviations below 1.5 pC versus ~2.5 pC, and averaging is expected to further improve resolution.

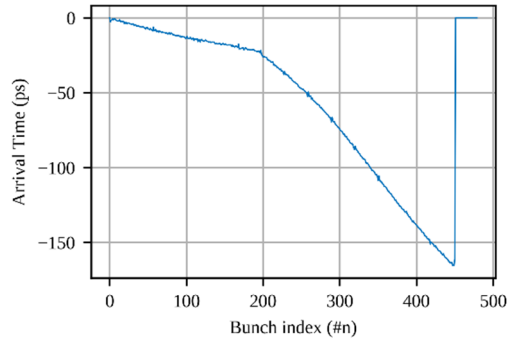

Figure 3: RFSoC-based BPM bunch arrival-time measurement for pattern in Fig. 1.

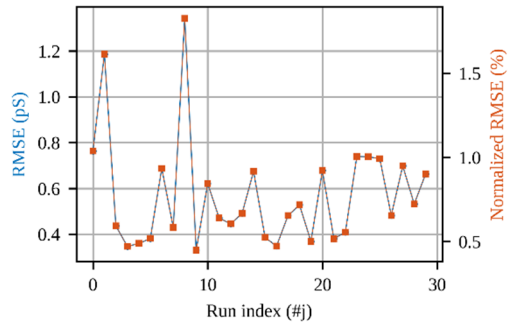

Figure 4: RMSE of the RFSoC-based BPM bunch arrival-time measurement for multiple measurement runs of pattern in Fig. 1.

Figure 3 shows the bunch arrival-time corresponding to the charge pattern of Fig. 1. At 400 mA, transient beam loading of the passive 3rd harmonic cavity (3HC) causes ~150 ps variation between head and tail of the train. The RMSE values per run are summarized in Fig. 4, remaining well below the 2 ns bunch spacing, significantly exceeding the accuracy required for longitudinal MBFB implementation using direct sampling. The transverse MBFB was successfully tested by exciting oscillations with beam pinger kicker in the horizontal and vertical planes. Figure 5 presents turn-by-turn BPM data with and without feedback at 74 mA. The fitted decay curves show damping times reduced from ~0.33 ms to ~0.20 ms in the X-plane and from ~0.28 ms to ~0.13 ms in the Y-plane, confirming the correct operation of the RFSoC-based MBFB system.

SUMMARY AND OUTLOOK

The RFSoC-based systems have been commissioned at SLS 2.0, providing important functionality during the first phases of commissioning. The FPFB measured bunch-charge and arrival-time diagnostics from day one. Recently, the FPFB feedback loop has been closed successfully. Minor issues with the EVM IOC, occasionally leading to a double bucket fill, were temporarily corrected with a workaround where the FPFB modifies the bucket list, accordingly, compensating the imperfections of the event master. The transverse MBFB is also operational, currently using the SLS 1.0 RFFE with analogue down-conversion, with the next step being migration to the RFSoC RFFE for direct sampling of BPM position signals. Building on this, we will exploit all ADC samples at 4 GS/s of the BPM position signals, taking into account the arrival time variation from first to last bunch caused by transient beam loading. The longitudinal MBFB with the new 1.875 GHz kicker cavity will be put into operation soon, including hardware acceleration of the current C-based bunch-phase calculation in VHDL and replacing the analogue up-converter with a digital one to directly drive the kicker amplifiers. The CBM diagnostics, now implemented at high level, is being ported to low-level software running in the RFSoC RPU. Monitoring of return signals from the transverse and longitudinal kicker cavities is foreseen with the AMD ZCU208 evaluation board and its 3rd generation RFSoC, providing additional diagnostics as well as automatic delay calibration.

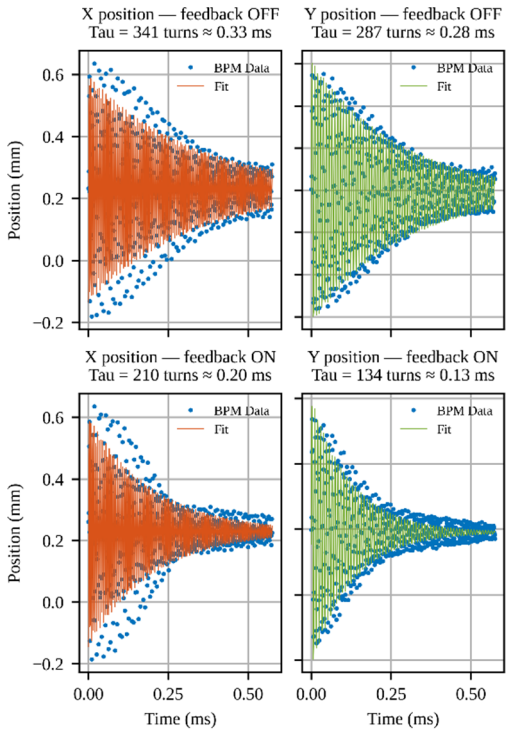

Figure 5: Turn-by-turn BPM X (red) and Y (green) position data at 74 mA with feedback OFF (top) and ON (bottom).

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[1] M. Böge, "SLS 2.0 storage ring commissioning", presented at IPAC'25, Taipei, Taiwan, Jun. 2025, paper WECN1, unpublished.

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