OPTIMIZATION AND UPGRADE OF THE BPM ELECTRONICS SYSTEM FOR CSNS-II RCS

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Abstract

The China Spallation Neutron Source (CSNS) Phase II project aims to increase the Rapid Cycling Synchrotron (RCS) beam power to 500 kW, resulting in a tenfold increase in Beam Position Monitor (BPM) signal amplitude from 10-20 V to 100 V, necessitating an electronics upgrade for precise position measurements. Inspired by the J-PARC Main Ring 1.3 MW upgrade, we propose a preliminary design featuring a MicroTCA.4-based Rear Transition Module (RTM) equipped with high-power attenuators for stable signal attenuation and impedance matching tailored to CSNS RCS cables (52.88 Ω, 80.6 m). Digital processing utilizes a domestically developed MicroTCA.4 AMC board based on the Xilinx Zynq-7045 SoC, supporting 8-channel 16-bit ADC at 125 MSPS and EPICS integration. Position calculations adopt the GSI least-squares fit algorithm to reduce offset-induced errors and enhance robustness. Using CSNS Phase I BPM offline data, Python simulations based on windowed least-squares fitting compared traditional Δ/Σ methods with the least-squares approach, indicating support for a target resolution of <1 mm and providing a foundation for the BPM electronics upgrade.

INTRODUCTION

The China Spallation Neutron Source (CSNS) Phase I has successfully operated its Rapid Cycling Synchrotron (RCS) at beam powers of 100 to 140 kW. The Beam Position Monitor (BPM) electronics system, validated through preliminary upgrades, handles dual-bunch frequencies between 1 and 2.44 MHz, with bunch lengths compressed from 500 ns to 100 ns, using a 250 MSPS 14-bit ADC with a dynamic range of 10^4. However, as CSNS Phase II targets an RCS beam power of 500 kW, the BPM signal amplitude is expected to increase tenfold from 10-20 V to 100 V, posing challenges for the existing electronics. The primary attenuation through resistive dividers is prone to temperature-induced drift and impedance mismatch, compromising position accuracy.

To address these challenges, our preliminary design draws inspiration from the J-PARC Main Ring 1.3 MW upgrade, which utilized high-power attenuators (e.g., RF2033 power divider) and nitrogen-sealed reed relays to achieve attenuation from -12 dB to -30 dB [1]. For CSNS II, we optimize the analog front-end while leveraging a domestically developed MicroTCA.4 AMC board based on the Xilinx Zynq-7045 SoC, supporting EPICS IOC integration [2]. Figure 1 shows the BPM electronics architecture based on the MicroTCA architecture, including RTM cards and AMC cards, connected via Zone 3.Algorithmically, we adopt the GSI time-domain least-squares fit method for Δ/Σ tuples to mitigate baseline offsets, enhancing position accuracy [3].

This study outlines the preliminary design, focusing on hardware architecture, algorithmic innovations, and simulation results.

SYSTEM DESIGN

Analog Front-End Design

The analog front-end is designed around a MicroTCA.4-based Rear Transition Module (RTM) board, adapting the attenuator unit architecture from the J-PARC Main Ring (MR) system, as illustrated in its block diagram

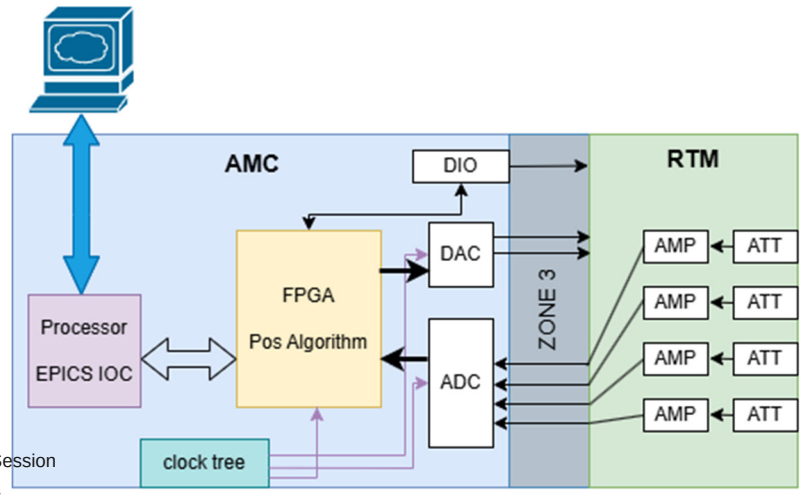

Figure 1: RCS-BPM system architecture diagram.

showing the attenuator configuration. This upgrade replaces the original four-stage passive resistive divider (attenuation ratios of 1, 0.25, 0.1, and 0.025) with a robust switchable attenuator combined with a proportional divider circuit. High-power components, such as the RF2033 power divider providing -12 dB attenuation, are integrated with nitrogen-sealed reed relays (e.g., HFS-1C-05W), maintaining contact resistance below 10 mΩ [1].

As shown in Fig. 2, the cable length and impedance deviate from the standard 50 Ω, with a measured characteristic impedance of approximately 52.88 Ω and a length of 80.6 m. This deviation validates the need for tailored impedance matching in the CSNS-II RCS BPM electronics design. Key optimizations focus on custom impedance matching networks adapted to the specific cable characteristics.

For high-power handling, the design attenuates input peaks of 100 Vpp to the ADC's 2 Vpp range with an overall -30 dB ratio. A 25 MHz low-pass filter (LPF) covers the primary harmonics from 1 to 2.44 MHz, filtering noise [4].

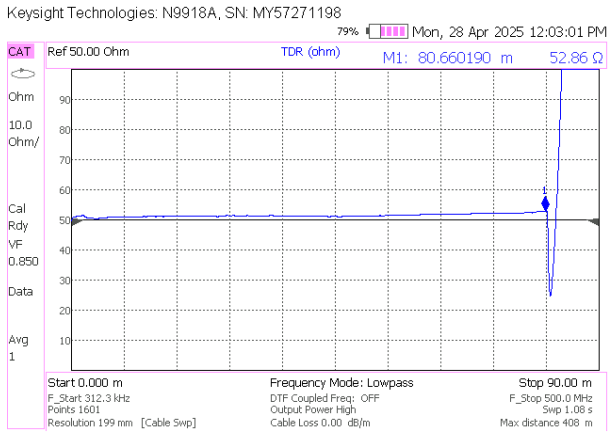

Figure 2: Illustrates the BPM cable impedance measured using a Network Analyzer Time Domain Reflectometry (TDR) technique.

Temperature and distortion control are enhanced through nitrogen-sealed relays, minimizing atmospheric contamination and maintaining a temperature coefficient below 0.1 dB/°C, with signal distortion under 1 % [1]. Compared to the CSNS I system [4], which exhibited good linearity but suffered from high reflections, this upgrade improves impedance matching and reduces reflections, ensuring compatibility with existing diagonal-cut BPM sensors featuring four electrodes while supporting the elevated voltages of CSNS II.

Digital Processing Design

Digital processing leverages a domestically developed MicroTCA.4 Advanced Mezzanine Card (AMC) board, centered on the Xilinx Zynq-7045 System-on-Chip (SoC). This board provides 8 channels of 16-bit ADC sampling at 125 MSPS, with a dynamic range exceeding 9.5 effective number of bits (ENOB) [2]. Figure 3 shows the block diagram of the RTM board module for MicroTCA.

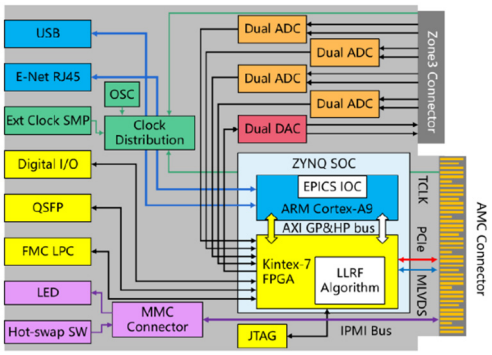

Figure 3: The block diagram of the AMC module [2].

System integration organizes each RCS quadrant with 8 front-end RTM boards and 8 AMC board. The EPICS Input/Output Controller (IOC) runs on the Zynq's ARM core, facilitating real-time position calculations and process variable (PV) publishing, ensuring scalability for CSNS II operations.

BPM POSITION ALGORITHM

Conventional Algorithm

Traditional BPM position calculations rely on the difference-over-sum (Δ/Σ) method, encompassing techniques such as integral (INT), root-sum-square (RSS), and standard deviation (STD). In the CSNS I system, a dual-threshold window integration is employed, defined by formulas $\Delta = \int(R-L)\,dt$, $\Sigma = \int(R+L)\,dt$, and $Pos = K * \Delta/\Sigma$, where K is a calibration constant. While effective for basic operations, this approach is highly sensitive to baseline offsets and low-frequency distortions [4].

Fitting Algorithm

To overcome these limitations, we adopt the GSI least-squares fit algorithm applied to Δ/Σ tuples, as outlined in. The core formula is $m = cov(\Delta, \Sigma)/var(\Sigma)$, with position $Pos = (1/s) * m$, where s represents the BPM sensitivity. This method offers significant advantages: it eliminates the need for baseline restoration and tolerates random offsets and AC coupling distortions [3]. Figure 4 illustrates an example of the least squares fitting method.

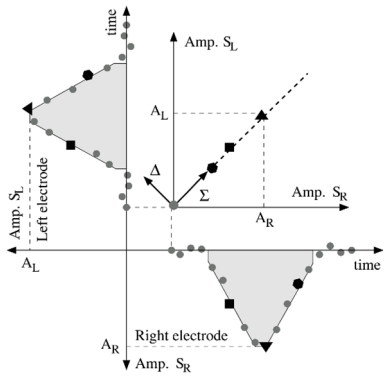

Figure 4: Illustration of fit method of left against right electrode signal [3].

Python Simulation and Algorithm Comparison

During the beam operation period, 20 ms offline data from the four BPM electrode waveforms were collected using an oscilloscope, while simultaneously recording the RF window signal. Python was used to process the signals within the window, applying both the conventional difference-over-sum algorithm with integration and the least-squares fit algorithm to calculate positions, generating turn-by-turn (TBT) data. Additionally, averaging over 1024 points was performed to obtain closed-orbit distortion (COD) data for comparison. Figure 5 shows a comparison of the COD data obtained from the differences over sum algorithm, the least squares fitting algorithm, and electronics output. In the figure, the blue line represents the COD data fitted by the differences over sum algorithm, the orange line represents the COD data fitted by the least squares fitting algorithm, and the green line represents the COD position data output by electronics.

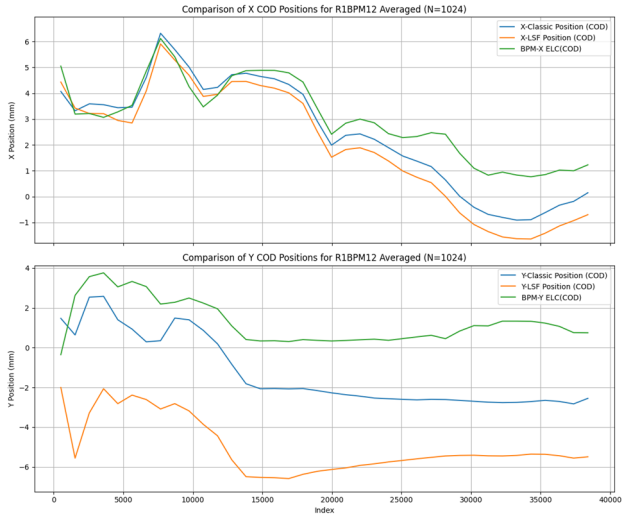

Figure 5: Comparison of COD data for different algorithms.

From the figure, it can be observed that the position trends calculated by different algorithms at the same moment are consistent, but the position offsets vary, indicating that the algorithm has a significant impact on position calculation bias. In subsequent work, various conditions will be introduced on the calibration platform to validate the effects of different algorithms on the offset.

CONCLUSIONS

With the power upgrade in CSNS Phase II, the RCS BPM detector signals are significantly larger, placing higher demands on the dynamic range of the new electronics, while the algorithm's impact on position calculation accuracy is also critical. The preliminary design for CSNS II RCS BPM electronics integrates J-PARC MR attenuator concepts and domestic MTCA hardware, combined with GSI algorithms to enhance accuracy. Future work includes hardware prototyping and beam tests.

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