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DESIGN OF DIGITAL ACQUISITION FOR BEAM CURRENT MONITOR*

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Abstract

As a part of the Proton Improvement Plan – II (PIP-II) at Fermilab, instrumentation systems are being modernized to take advantage of the higher speeds and ease of use offered by standardized embedded systems like MicroTCA. A rear-transition module (RTM) is being designed to interface with said embedded systems. In each of the four identical channels on the RTM, the differential signal from an alternating-current current transformer (ACCT) transimpedance amplifier will again be amplified by a differential operation-amplifier, then filtered by a low-pass topology. The conditioned signal is then digitized at a maximum of 10 MS/s by an analog to digital converter (ADC) integrated circuit. After digitization, the ADC passes the data to an off the shelf AdvancedMC (AMC) Xilinx FPGA module using low voltage differential signals. This paper will describe the simulation of analog circuitry for signal conditioning, simulation of digital signal integrity based on physical design as well as verification of design characteristics critical to signal integrity. This work aims to create a methodology that can be applied to future RTMs requiring application of high-speed digital design principles.

INTRODUCTION

Historically, instrumentation infrastructure at Fermilab utilized VME architecture to achieve modularity [1]. Over time, there became an increasing need for higher bandwidth signal processing and data transfer to facilitate research and development. MicroTCA was selected as the replacement to meet these needs and others, including flexibility in processing power through the selection of the AMC and better maintainability via the integrated management systems and hot-swappable RTMs (see Fig. 1).

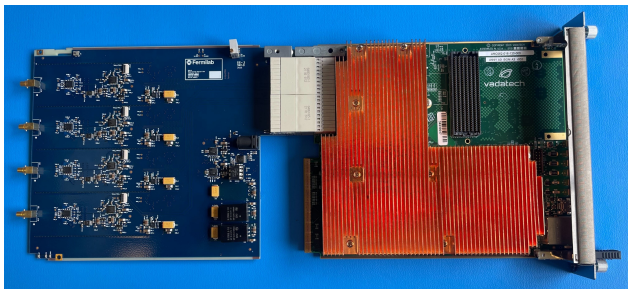

Figure 1: RTM and AMC outside of MicroTCA chassis.

In order to incorporate beam current monitor measurements into the MicroTCA update effort, a prototype ACCT RTM was designed. The raw signal is created by a Bergoz ACCT with a maximum cutoff frequency of 5.0121 MHz. The raw signal then passes through a shielded twisted pair to interface with the Bergoz ACCT-E-RM-3R transimpedance amplifier. To reduce the risk of failure due to radiation degradation, the transimpedance amplifier will be placed just outside the enclosure, necessitating a cable length longer than the Bergoz specified 20 m. Three outputs exist on the ACCT-E-RM-3R, a 50 Ω single ended BNC, 1 MΩ BNC, and a 100 Ω differential BNO output. The 1 MΩ output was not used because the high impedance increases the risk of coupled electro-magnetic interference generating electrical noise. The 50 Ω single ended connection was already in use, leaving the differential output. The generated differential output voltage can vary depending on the termination of the signal at the ACCT RTM. Again, the low impedance termination was selected for the ACCT RTM and, per specification, the differential output voltage has a range of ±2 V.

HARDWARE DESIGN

To ensure compatibility with the AMC562 and MicroTCA system, the ACCT RTM was designed with the intention to meet specifications laid out in conjunction with Vadatech. The specifications defined requirements such as: the dimensional envelope the ACCT RTM printed circuit board (PCB) must fit in, the location and functional pinout of the high-speed backplane connectors, and a required set of circuitry referred to as Zone 3 circuitry (Fig. 2). Several RTMs are being designed concurrently at the laboratory, so the Zone 3 components and topology were selected to be common.

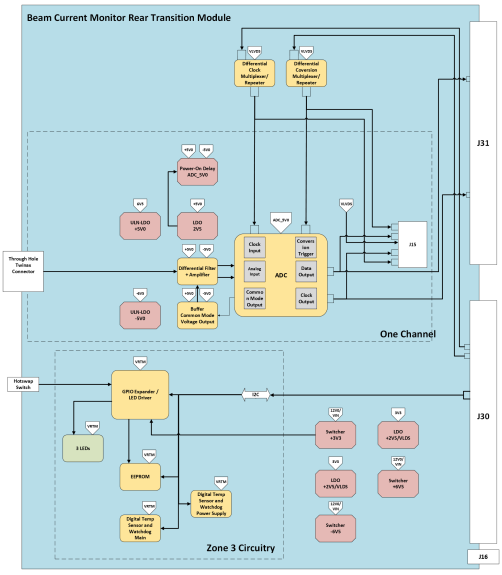

Figure 2: ACCT RTM block diagram.

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Digitizer

The ACCT RTM was chosen to have four identical digitizer channels to reduce the number of unused channels while still meeting the needs of the PIP-II beam layout. The AD7626 differential ADC was selected as the digitizer integrated circuit (IC) due to its 10 MS/s throughput to allow for the digitization of the 1 MHz signal without amplitude and phase distortion along with its ability to communicate through LVDS protocol with the AMC562. To achieve full throughput the AD7626 required a 250 MHz LVDS clock signal and 250 MHz LVDS conversion trigger. Each differential pair originates from the FPGA on the AMC562 and is fed into a 2:8 SY89838 clock buffer/multiplexer IC, one buffer per pair, on the ACCT RTM to support the four onboard channels. The internal reference voltage of 4.096 V on the AD7626 was used for simplicity purposes, and the required common mode voltage of 2.048 V is an output of the IC. The digital output of the AD7626 consists of two sets of LVDS pairs: the digitized signal and a clone of the input clock to account for time delay in routing, also operating at 250 MHz.

Analog

The differential op-amp THS413IDR in anti-alias filtering configuration conditions the input from the transimpedance amplifier. The common mode voltage from the AD7626 is buffered then taken as an input to the THS4131DR. The maximum output voltage swing of the THS413IDR over the full temperature range of the IC was specified in the datasheet as ±3.6 V. It was ambiguous as to whether maximum output voltage swing was a differential or single-ended specification. A nominal voltage gain of 1.5 was selected to satisfy the output voltage swing specification for both cases. The low pass filter was designed to have a cutoff frequency of at least 5 MHz. Nominal component values were derived from example equations given in the THS413IDR datasheet, then refined in LTSpice simulations. A Monte-Carlo simulation was also performed to evaluate the effect of passive component tolerances on the gain and filter performance (Fig. 3).

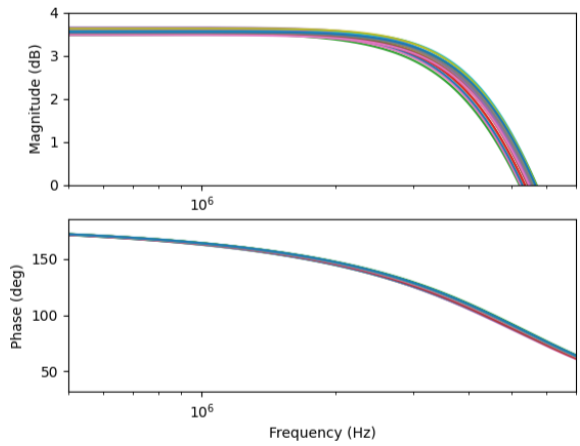

Figure 3: Passive component tolerance Monte-Carlo.

Board Stack-Up

The layer stack-up of the ACCT RTM PCB was custom designed to appropriately apply high speed digital design techniques needed for sub 0.5 ns signal rise times. Isola FR408HR was selected as the dielectric material due to its general availability in the market and controlled dielectric properties. The top and bottom of layers of the PCB were selected to be the signal layers with ground planes as the inner adjacent layers. Early floor planning showed that no analog signals would run parallel to digital traces for any considerable length allowing for analog and digital signals to be on the same layer. The Layer Stack Manager tool in Altium was used to define the six layer stack-up and calculate the desired trace width and spacing for differential pairs. The nominal distance between the signal layers and adjacent ground plane was selected to be approximately 3.5 mils which ensured that the LVDS trace width and spacing was equal to or greater than 6 mils. The 6 mils trace and spacing was desired to allow for bare PCB manufacturers to use standard processes which controls cost and facilitates quality. The innermost layers, of each set of three, are voltage planes and have a distance of approximately 4 mils to their respective adjacent ground planes. A ground layer to voltage layer spacing of 4 mils or less increases the capacitance between the planes creating a desired parasitic bypass capacitance able to filter at high frequencies. The thickness of dielectric materials between the two sets of three layers were selected to increase the nominal overall board thickness, including solder mask, to within 1 mil of the required 62.3 mils board thickness.

Signal Integrity Investigation

Signal integrity simulations were performed on LVDS routing using Altium's signal integrity tool. The intent of the simulations were to evaluate intentional impedance discontinuities from debugging components, fanout, and termination of the traces. A simulation was performed on the clock differential pair from the SY8983 multiplexer to the AD7626. The IBIS model of the SY89838 was derived from the ibis model for the SY89543 multiplexer in a similar family. The IBIS model for the AD7626 was available from the manufacturer. The LVDS clock signal was terminated with a 100 Ω resistor between the signals in the differential pair. Another simulation was performed on the data output of the AD7626 to the ACCT RTM and AMC562 interface. It was assumed that the differential pair routing and termination on the AMC562 board was done correctly, so only the traces on the ACCT RTM were of concern. The connector interface was treated as an IC in simulation and artificially terminated with each signal in the pair terminated to the common mode voltage of 1.2 V with 50 Ω .

The single ended impedance of the traces was validated through the use of MOHR CT100HF TDR, a trimming potentiometer and an in-house assembled 50 Ω probe utilizing the test features included in the design (see Fig. 4).

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Figure 4: TDR test setup.

RESULTS

The bode plot of the Monte-Carlo analysis of component tolerance on frequency response of the anti-alias filter is shown in Fig. 3. The initial amplification shows that component tolerance to be responsible for 50 mV of variation in the output of the filter. A comparison of the frequency response at 1 MHz to the initial amplification value showed a variation of less than 10 mV, indicating good margin from the cutoff frequency. All simulated cutoff frequencies, −3 dB from the initial amplification, were greater than 5 MHz with the smallest value being 5.012 MHz.

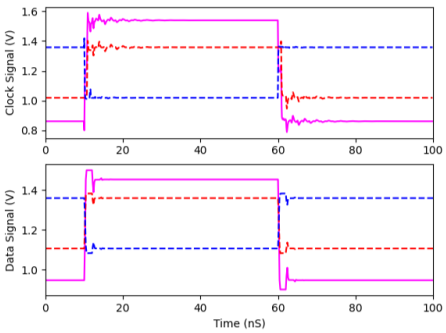

Figure 5: Signal integrity simulation.

Figure 5 shows the differential clock signal, offset by the common mode voltage, overlaid the positive and negative portions of the differential pair. The simulated distortion due to reflection in the differential signal is far away from the logic level transitions, indicating good signal integrity. The differential signal shows the simulated reflections cause an overshoot of approximately 60 mV on the rising edge. The overshoot is present in the single ended traces but is much less than the max pin voltage of 2.5 V.

The data signal to the ACCT RTM interface is also shown in Fig. 5. The simulated distortion in the differential data signal shows less overall ringing but a larger undershoot. There is still a significant amount of margin from the logic level transitions. However, any additional discontinuities on the AMC562 may cause signal integrity issues in the actual design.

Figure 6 shows the impedance measurement of the test structure on ACCT RTM. The red highlighted region is

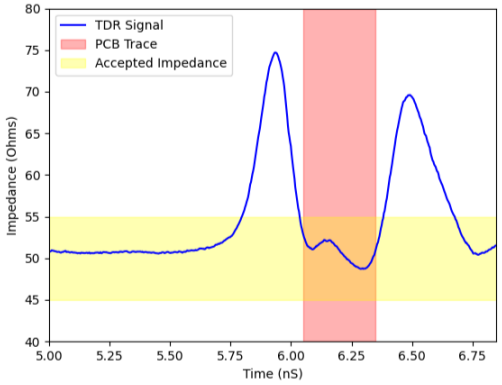

Figure 6: Trace impedance measurement.

actual trace on the PCB and is in a valley between two peaks with maximum magnitudes greater than 70 Ω. The first peak represents the probe connection to the test structures. It is believed that the increase in impedance is due to the design of the in-house probe. The length of the contacts where the polymer dielectric was replaced with air, and no shielding exists, is likely too long. The second peak is likely due to an increase in impedance from the lead length and internals of the trimming potentiometer. The yellow highlighted region shows the accepted range of impedances for the PCB trace on board. Even with the discontinuities due to the two peaks, the PCB trace impedance does appear to be within the acceptable range for this design.

CONCLUSION

Simulation results and results of early acceptance testing are promising. The Monte-Carlo analysis shows the need for calibration to account for the initial offset error due to component tolerances. A 50 mV offset from the nominal is analogous to a 17 µA offset from the Bergoz output, which is an error of 1.7 % of the maximum 1mA range. The signal integrity simulations of the LVDS differential pair show that the intended termination scheme should be adequate for the final design. The simulated signal distortion due to reflections shows more than 100 mV of margin from logic level transitions and very little risk of part damage due to undervoltage or overvoltage. The signal integrity simulations were supported by the TDR measurements, showing that the measured trace impedance matched the intended design.

Some of the parts that are necessary for the board to function were populated incorrectly, which limited the possible analysis and validation of the design. Future work will remedy the incorrect part population allowing the assessment of filter performance, digitizer performance, and FPGA algorithms.

REFERENCES

[1] R. R. Santucci, J. S. Diamond, N. Eddy, A. Semenov, and D. C. Voy, “A Modern Ethernet Data Acquisition Architecture for Fermilab Beam Instrumentation”, in *Proc. IBIC’22*, Kraków, Poland, pp. 500–503, 2022. doi:10.18429/JACoW-IBIC2022-WEP40