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DESIGN AND DEVELOPMENT OF A FOC ALGORITHM BASED ON MACHINE LEARNING FOR THE HEPS

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Abstract

The High Energy Photon Source (HEPS) is a fourth-generation synchrotron light source with 6 GeV beam energy developed by the Institute of High Energy Physics. The Fast Orbit Feedback (FOFB) system maintains beam orbit stability for optimal performance. This work presents a neural network-based algorithm to replace traditional PID control in FOFB systems. A Multi-Layer Perceptron (MLP) neural network was designed and trained using simulated data from HEPS, with hyperparameter optimization to enhance performance. The trained model was quantized for FPGA deployment and validated in a laboratory test environment. The system achieved mean error at the 1 mA level, demonstrating the feasibility of neural networks as an effective alternative to PID control in FOFB applications.

INTRODUCTION

The High Energy Photon Source (HEPS) is a fourth-generation synchrotron radiation facility under construction by IHEP, operating at 6 GeV with brightness of $1 \times 10^{22}\,\mathrm{phs \cdot s^{-1} \cdot mm^{-2} \cdot mrad^{-2} \cdot (0.1\,\%\,bw)^{-1}}$ and emittance <60 pm·rad [1].

Fast Orbit Feedback (FOFB) systems are critical for maintaining beam stability. Traditional PID-based FOFB relies on response matrices requiring online measurement, consuming commissioning time. Neural network approaches offer data-driven alternatives with implicit physical encoding, eliminating explicit matrix calculations during operation [2–5].

This work presents an MLP-based FOFB implementation using FPGA technology. The model correlates beam orbit with corrector mappings using HEPS simulation data, with systematic evaluation of latency optimization and BPM malfunction robustness [5, 6].

SYSTEM ARCHITECTURE

FOFB System Overview

The FOFB system involves coordinated operation of multiple subsystems, including accelerator physics, control systems, power supplies, magnets, and timing. It comprises three main subsystems: the beam position monitor (BPM) system, the FOFB controller system, and the fast corrector subsystem including fast corrector power supplies, magnets, and vacuum boxes.

In each control cycle, the Orbit Feedback Controller (FOC) receives beam position data from all BPMs in the storage ring, applies the orbit feedback algorithm to determine appropriate setpoints for fast corrector power supplies, and transmits results to backend fast corrector power supply controllers (PSC) which convert the data into corresponding currents applied to fast correctors, ultimately adjusting the beam position.

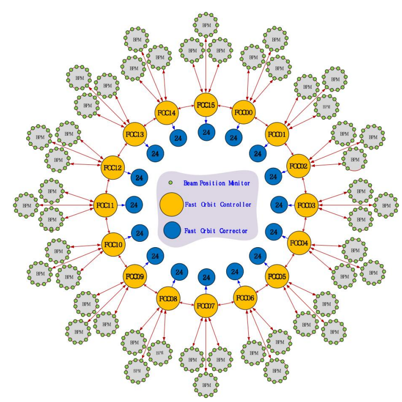

Figure 1: FOFB system topology.

The FOFB system topology, shown in Fig. 1, adopts a 7BA (Seven-Bend Achromat) lattice structure with 48 units. The storage ring is equipped with 576 BPMs, 384 fast correctors, 48 BPM sub-stations, and 16 FOFB sub-stations. Each BPM sub-station contains 12 sets of BPM electronics, while each FOFB sub-station is equipped with one FOC directly controlling 24 correctors across three 7BA cells [4, 7].

MLP Neural Network Architecture

Multi-Layer Perceptron (MLP), also known as a fully connected neural network (FCNN), consists of neurons connected in parallel with multiple hidden layers between input and output layers. The model structure is shown in Fig. 2. MLP is capable of modeling interaction responses and is primarily used for solving classification and regression problems [8].

The designed neural network comprises two hidden layers with 16 and 64 neurons respectively. The input consists of 576 sets totaling 1,152 position data points, while the output yields 384 correction values. These correction values are represented as signed fixed-point numbers with 21-bit data width in amperes, including a 4-bit integer part, a 16-bit fractional part, and a sign bit as the most significant bit.

FPGA Implementation Strategy

FPGA-based implementations provide low-latency, deterministic execution for real-time mapping from 576 BPM

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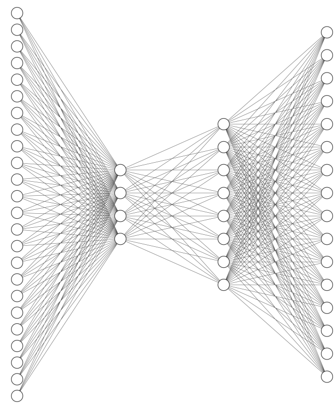

Figure 2: MLP neural network structure.

inputs to 384 corrector outputs. Hardware-level determinism and low power consumption enhance long-term stability [9].

The MLP uses fixed-point arithmetic with pipelined reuse of DSP resources. The architecture consists of three layers: 1,152 ×16, 16 × 64, and 64 × 384, with 32-stage pipelined matrix multiplication. ReLU activation is applied after each layer, with truncation only during zero-crossing comparison to maintain precision [10].

IMPLEMENTATION DETAILS

Data Collection and Model Training

Simulated data from HEPS was collected using the Experimental Physics and Industrial Control System (EPICS) platform, including beam orbit distortions and fast corrector strengths. The dataset characteristics are summarized in Table 1. The storage ring's 576 BPMs measure orbit offset in both vertical and horizontal directions, providing 1,152 input features, while 384 fast corrector values serve as training targets. A total of 440,000 data points were collected with 80 % allocated for training and 20 % for testing.

Table 1: Dataset Characteristics

Parameter	Value
Number of BPMs	576
Number of Correctors	384
Input Features	1,152
Output Features	384
Total Data Volume	440,000
Training Proportion	80 %
Testing Proportion	20 %

Model Quantization for FPGA Deployment

Quantization analysis was performed for bit widths from 4 to 16 bits. Results in Fig. 3 show significant accuracy degradation at 4-6 bits, slight decrease at 8 bits, and stable performance at 10+ bits. Considering both model accuracy and hardware resource constraints, 8-bit quantization was selected as the optimal compromise between performance and FPGA resource utilization.

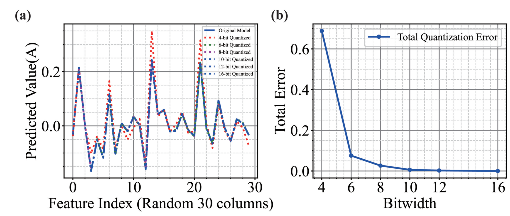

Figure 3: Precision analysis for different quantization bit widths: (a) accuracy loss for 30 random predictions, (b) accuracy loss under different bit widths.

RESULTS

MLP Model Performance

The trained MLP model demonstrates excellent prediction accuracy as shown in Fig. 4. Blue markers represent actual corrector values while red crosses indicate predicted values. The model achieves close agreement with an average absolute error of 1.04091 mA, validating the effectiveness of the neural network approach for FOFB control.

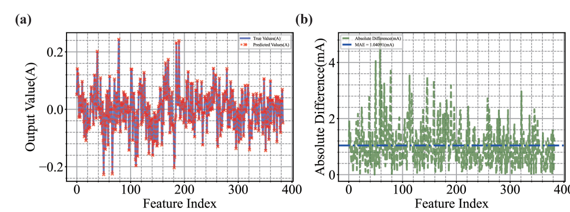

Figure 4: Model prediction performance: (a) actual vs. predicted values for 384 correctors, (b) prediction deviations with MAE indicated by blue line.

Robustness Under BPM Failures

Model robustness was evaluated by randomly injecting fault data into 1-50 BPMs in the test dataset. Figure 5 shows the impact of varying BPM failure numbers on model performance. Test loss increases linearly from 0.002 to 0.004 as failures grow from 0 to 50, while Mean Absolute Error (MAE) rises from 0.02 to 0.04. Importantly, even under high-failure scenarios (50 BPM failures), the MAE stabilizes at 0.04 level, demonstrating robust fault tolerance essential for practical engineering applications.

FPGA Implementation Validation

Comprehensive validation was conducted comparing MATLAB simulation inference results with actual deployed model outputs. Figure 6 presents excellent agreement between simulation and hardware implementation, with Mean Squared Error (MSE) of 0.000083 and R^2 coefficient of 0.999999. This demonstrates high fidelity of the FPGA hardware implementation and validates the quantization strategy effectiveness.

The FPGA-based MLP implementation achieves processing latency under 10 microseconds, meeting real-time requirements for FOFB systems while maintaining deterministic execution. The combination of hardware optimization

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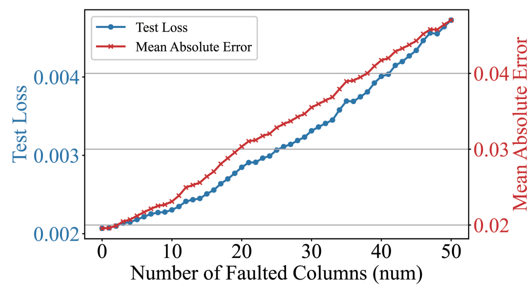

Figure 5: Model performance degradation under different numbers of faulty BPMs, showing robust fault tolerance.

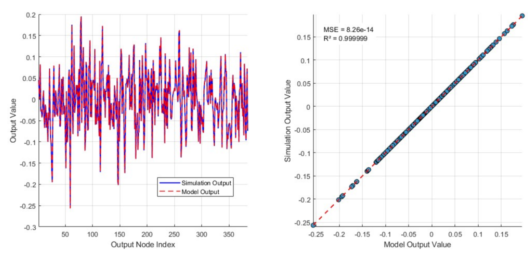

Figure 6: FPGA implementation validation: (left) overlaid waveforms of MATLAB simulation vs. deployed model, (right) consistency scatter plot showing MSE = 0.000083 and R^2 = 0.999999.

and model quantization provides an effective solution for high-performance accelerator control applications.

CONCLUSIONS

This work introduces a FOC algorithm for FOFB systems based on an MLP neural network. The algorithm constructs a data set from simulated data of the HEPS light source, building an MLP model that maps 576 BPMs to 384 fast correctors, which is deployed on FPGA. We optimize the MLP model through grid search of hyperparameters and validate its stability by incorporating random noise into the dataset to simulate BPM fault conditions. Experimental exploration of different bit-width configurations achieves an optimal balance between precision and FPGA resource utilization. The implementation accelerates inference time through a specially designed pipelined reuse architecture for adders and multipliers. Unlike traditional PID algorithms, our MLP-based FOFB system eliminates explicit dependence on response matrices. While the current MLP architecture demonstrates simplicity and excellent accuracy, there remains optimization potential through investigating alternative neural network structures like Transformers to achieve superior model performance.

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