ISBN: 978-3-95450-262-2 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2025-MOPMO21

BEAM DIAGNOSTIC SIGNAL PROCESSOR FOR SHINE*

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Abstract

SHINE has developed different signal processors for beam diagnostics, including processors for cold button beam position monitor (BPM), stripline BPM, chicane BPM, cavity BPM, cavity bunch arrival-time monitor (BAM), electro-optic BAM, CSR bunch length monitor (BLM), beam charge loss monitoring, and fast orbit feedback system (FOFB). The processors employ a common SoC-FPGA-based digital motherboard and accommodate diverse applications by hosting various daughterboards. This paper presents the design of these processors and the applications on SHINE.

INTRODUCTION

The Shanghai HIgh repetitioN rate XFEL and Extreme light facility (SHINE) is China's first hard X-ray FEL, scheduled for completion in 2027 [1]. The 3.1 km facility, located 30 m underground in Zhangjiang, comprises an injector, superconducting LINAC, three undulator lines, three photon beamlines, and ten experimental stations.

Beam diagnostics are essential for stable accelerator operation. Over 500 devices will be installed, including button BPMs, stripline BPMs, chicane BPMs, cavity BPMs, bunch arrival-time monitors (BAMs), electro-optic BAMs, CSR bunch length monitors, beam charge loss monitors, and the fast orbit feedback (FOFB) system [2].

To meet the requirements of high-performance diagnostics, SHINE has developed a series of signal processors supporting real-time operation at 1 MHz. All processors are based on a common SoC-FPGA motherboard, adapted to specific applications with dedicated daughterboards. Table 1 summarizes the processors, and the following sections present the platform design and implementations.

COMMON FPGA PLATFORM

A generic FPGA motherboard was developed as the core of the common platform (Fig. 1). It is based on a SoC FPGA integrating a quad-core ARM processor and programmable logic. An FMC LPC interface allows mounting a White Rabbit timing card to provide bunch ID and trigger signals, enabling synchronous data acquisition.

* Work supported by The National Science Foundation of China (Grant No.12175239). Youth Innovation Promotion Association, CAS (Grant No.2019290). Outstanding member of the Youth Innovation Promotion Association, CAS (Gant No.Y2023079).
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The motherboard connects to ADC daughterboards via the FMC HPC interface. Different ADC boards can be used to implement multiple processors, reducing cost and design effort. Table 1 summarizes the diagnostic monitors and requirements that define each processor specification. This flexible architecture makes the platform suitable for a wide range of diagnostics at SHINE.

Table 1: SHINE Beam Diagnostic Processors

Monitors	Number	Daughterboard specification
Cold button BPM	80	1 GSPS, 14-bit
SBPM	90	1 GSPS, 14-bit
Chicane BPM	3	8-channel 1 GSPS, 14-bit
CBAM	6	1 GSPS, 14-bit
LTU CBPM	80	1 GSPS, 14-bit
Undulator CBPM	100	2.6 GSPS, 14-bit
EO-BAM	4	250 MSPS, 16-bit
CSR-BLM	2	250 MSPS, 16-bit
FOFB	12	8 × SFP, 8 × FL
Charge interlock	11	8 × SFP, 5 × interlock

On the software side, all processors share a common IOC framework based on Debian and EPICS. The system supports automatic startup, remote access, time synchronization, and save / restore of IOC status. The IOC monitors ADC waveforms, beam position, bunch ID, and interlock signals. User interfaces, developed with PyDM, display process variables and system status on control room screens. Figure 2 shows the SHINE signal processor PyDM main interface.

Figure 1: FPGA motherboard.

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Figure 2: Main interface of the SHINE signal processor in PyDM.

4-CHANNEL 1GSPS PROCESSOR

To support 4-channel operation at up to 1 MHz, a dedicated processor was developed for SHINE. It provides better than 0.1 % resolution for SBPM, LTU CBPM, and cold button BPM, and more than 10-bit ENOB for CBAMs. The processor uses a 4-channel, 14-bit ADC board with up to 1 GSPS (Fig. 3). An external 216.67 MHz clock is multiplied by 4, resulting in a sampling rate of 866.68 MHz.

Figure 3: ADC board.

Figure 4: Generic signal processor.

For cold button BPMs (~1 GHz, 100 MHz bandwidth) and SBPMs (~500 MHz, 40 MHz bandwidth), standard processors (Fig. 4) are used. A dedicated SBPM processor was developed with dump-bucket scanning and interlock protection for a specific installation: under high-repetition-rate mode, it drives a circular beam scan, monitors the orbit in real time, evaluates the scan radius and trajectory, and outputs interlock signals (Fig. 5). Online injector tests with SBPMs [3] showed 1.8 µm resolution (combined RF front-end and processor) and 1.0 µm resolution (processor alone).

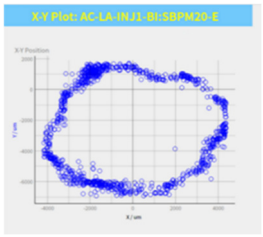

Figure 5: Beam scan experiment.

SHINE also employs two types of cavity BPM pickups: 35 mm unit in the LTU with 3.5 GHz signal down-converted to ~54 MHz by a 1 GSPS processor, and 8 mm unit in the undulator. For CBAMs, the processor achieved an relative amplitude resolution of 4.3×10^{-4} and arrival-time resolution of 4.9 fs (Fig. 6).

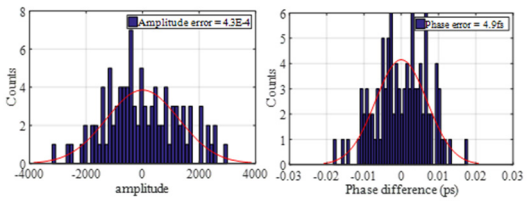

Figure 6: The relative amplitude resolution (left) and arrival-time resolution (right).

8-CHANNEL 1GSPS PROCESSOR

To meet the 0.1 % resolution requirement for chicane BPMs (Fig. 7), an 8-channel processor was built using a 14-bit, 1 GSPS ADC board mounted on the motherboard. It is applied to four pairs of button electrodes in the BC section, with beam position determined from the relative signal distribution.

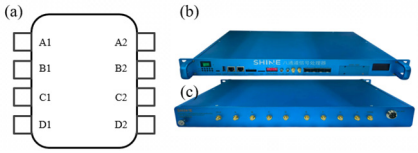

Figure 7: Chicane BPM layout (a), front view of the processor (b), and back view of the processor (c).

RF DIRECT SAMPLING PROCESSOR

For the undulator CBPMs (5.254 GHz), an RF direct-sampling processor was developed to avoid complex down-conversion. The system requires only a BPF, LNA, and attenuator (Fig. 8), reducing analog components and easing maintenance. It is based on the common FPGA motherboard with a direct-sampling ADC module (4-channel, 14-bit, 5.254 GHz bandwidth, 2.6 GSPS) (Fig. 9). A fixed-point Goertzel-DFT algorithm was implemented for high-repetition-rate processing.

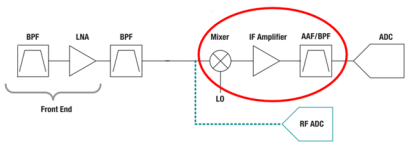

Figure 8: RF direct sampling processor block diagram.

Figure 9: RF direct sampling processor.

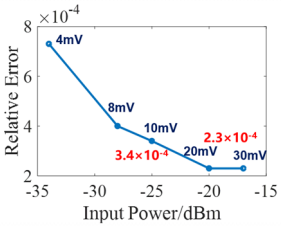

Figure 10: The relative position error in the lab.

ISBN: 978-3-95450-262-2 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2025-MOPMO21

Laboratory tests achieved relative errors of 3.4×10^{-4} (100 pC, 100 µm) and 2.3×10^{-4} (100 pC, 200 µm), surpassing the 1.0×10^{-4} requirement (Fig. 10). Beam tests at SXFEL confirmed resolutions of 3.2×10^{-4} with ~300 µm jitter. All hardware is completed and ready for deployment.

4-CHANNEL 250MSPS PROCESSOR

Both EOBAM and CSR-BLM require high amplitude resolution with relatively low bandwidth. A 4-channel, 250 MSPS processor with 16-bit ADCs was developed. For EOBAM, single-point sampling is sufficient, using two channels per signal: one for the peak and one for the baseline (Fig. 11). The arrival time is determined from the peak–baseline difference. For CSR-BLM, a 216 MSPS sampling rate is adequate, but high resolution is essential. A DC-coupled version of the same processor is used, with a down-converted CBPM reference cavity signal for normalization. This design meets the requirements of both systems (Fig. 12).

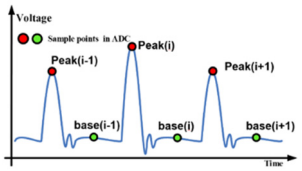

Figure 11: EOBAM signal sampling diagram.

Figure 12: EOBAM processor.

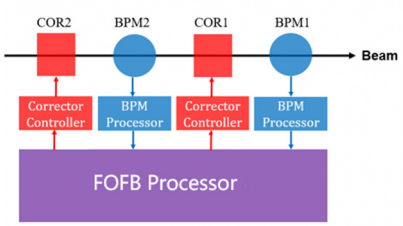

Figure 13: FOFB processor block diagram.

FAST ORBIT FEEDBACK (FOFB) PROCESSOR

The FOFB system requires high-speed BPM data reception and correction signal distribution. A dedicated processor was developed on the common FPGA motherboard. The processor architecture is shown in the processor block diagram (Fig. 13). It integrates an 8-channel SFP interface board for BPM data and an 8-channel FL interface board for corrector power supplies. The SFP board provides eight 10 Gbit optical links, while the power-control board supports eight 5 Mbaud (Manchester-encoded) links. The processor collects orbit data from BPMs, computes deviations, and generates correction signals based on SVD with PID algorithm. Hardware implementation is shown in Fig. 14, including the processor and SFP interface board. The system is under development.

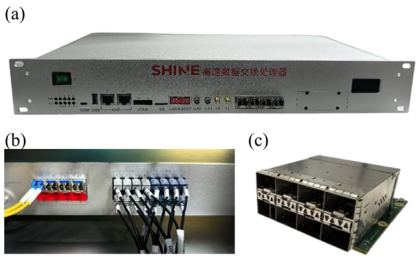

Figure 14: Front view of the FOFB processor (a), back view of the FOFB processor (b), and the SFP interface board (c).

BEAM CHARGE INTERLOCK PROCESSOR

The beam charge interlock requires BPM charge data reception and interlock signal generation. A dedicated processor was developed based the common FPGA motherboard. It integrates an 8-channel SFP interface board for BPM data reception and 5-channel interlock interface for system protection. The SFP board supports 10 Gbit links, allowing charge data to be collected from BPM processors. The processor compares the received data with predefined thresholds to detect beam loss and generates interlock signals accordingly. The processor architecture is shown in Fig. 15 and is under development.

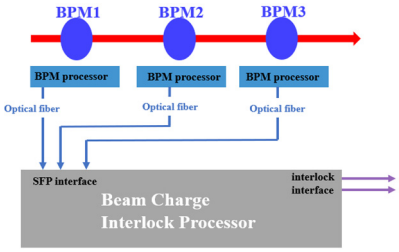

Figure 15: Block diagram of beam charge interlock processor.

Figure 16: Photograph of the processor cabinet (left) and electronics control page (right).

CONCLUSION

The processors have been installed and commissioned from the injector to the COL1 section of SHINE (Fig. 16). Several functions have been optimized, including phase-lock and trigger indicators, and processor fan status monitoring, enabling batch management. These improvements enhance system reliability and maintainability, providing a foundation for future deployment across the facility.

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