

ALS-U Instrumentation Overview*

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Abstract

The Advanced Light Source Upgrade (ALS-U) to a diffraction-limited storage ring with a small vacuum chamber diameter requires excellent orbit stability and a fast response orbit interlock for machine protection. The on-axis swap-out injection scheme and dual RF frequencies demand fast monitoring of pulsed injection magnets and a novel approach to timing. Recent development efforts at ALS and advances in PLLs, FPGAs, and RFSoCs that provide higher performance and mixed signal integration can be leveraged for instrumentation solutions to these accelerator challenges. An overview of preliminary ALS-U instrumentation system designs and status will be presented.

Introduction

The ALS-U upgrade project will deliver a world-leading light source that provides users with bright, high-coherent-flux soft x-rays. The scope of the upgrade includes a new 2-GeV, high-brightness storage ring (SR) fed by a new full-energy accumulator ring (AR) and transfer lines in the existing ALS storage-ring tunnel. The AR will be installed early, and the plan is to complete AR commissioning in 2025, with the remaining accelerator sections to be commissioned in 2026.

The ALS-U Instrumentation team is responsible for high speed, high performance electronic systems and fast data networks that interconnect devices. The systems are grouped into four categories: orbit stability (BPMS and fast orbit feedback (FOFB)), timing (event generation and distribution, injection triggering), fast machine protection (fast interlock and global mitigation), and fast data acquisition (fast monitoring of ICTs, BCMs, fast magnets).

Since the AR and SR requirements and interfaces for these systems are generally similar, the approach is to provide common designs with a superset of features to accommodate both rings. This paper will present a brief overview of each of the instrumentation systems.

Architecture

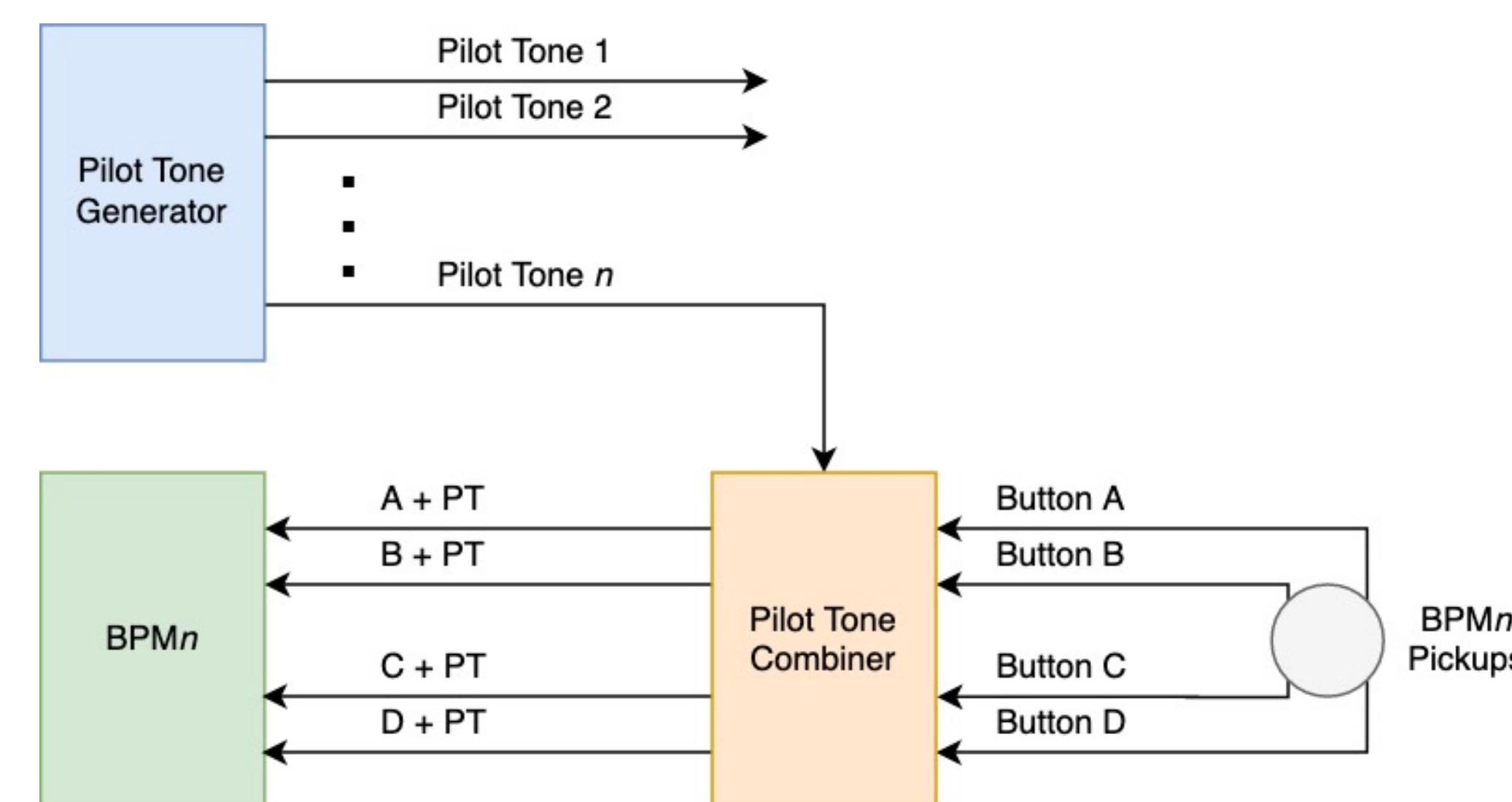
To reduce the engineering effort required to implement these systems, a philosophy based on design reuse is employed wherever feasible. Examples of this include: identical hardware designs for the AR and SR, common PC boards and internal chassis components, and common panel components (i.e. connectors, displays, buttons, labels). In addition, modular firmware and embedded software are reused to minimize porting code across platforms and applications.

Many of the ALS-U instrumentation hardware designs use the Marble [1] digital platform, developed at LBNL. RFSoC platforms that integrate high speed data converters (DACs and ADCs) with programmable logic and dedicated CPUs in a single chip are used in the highest performance analog front end designs.

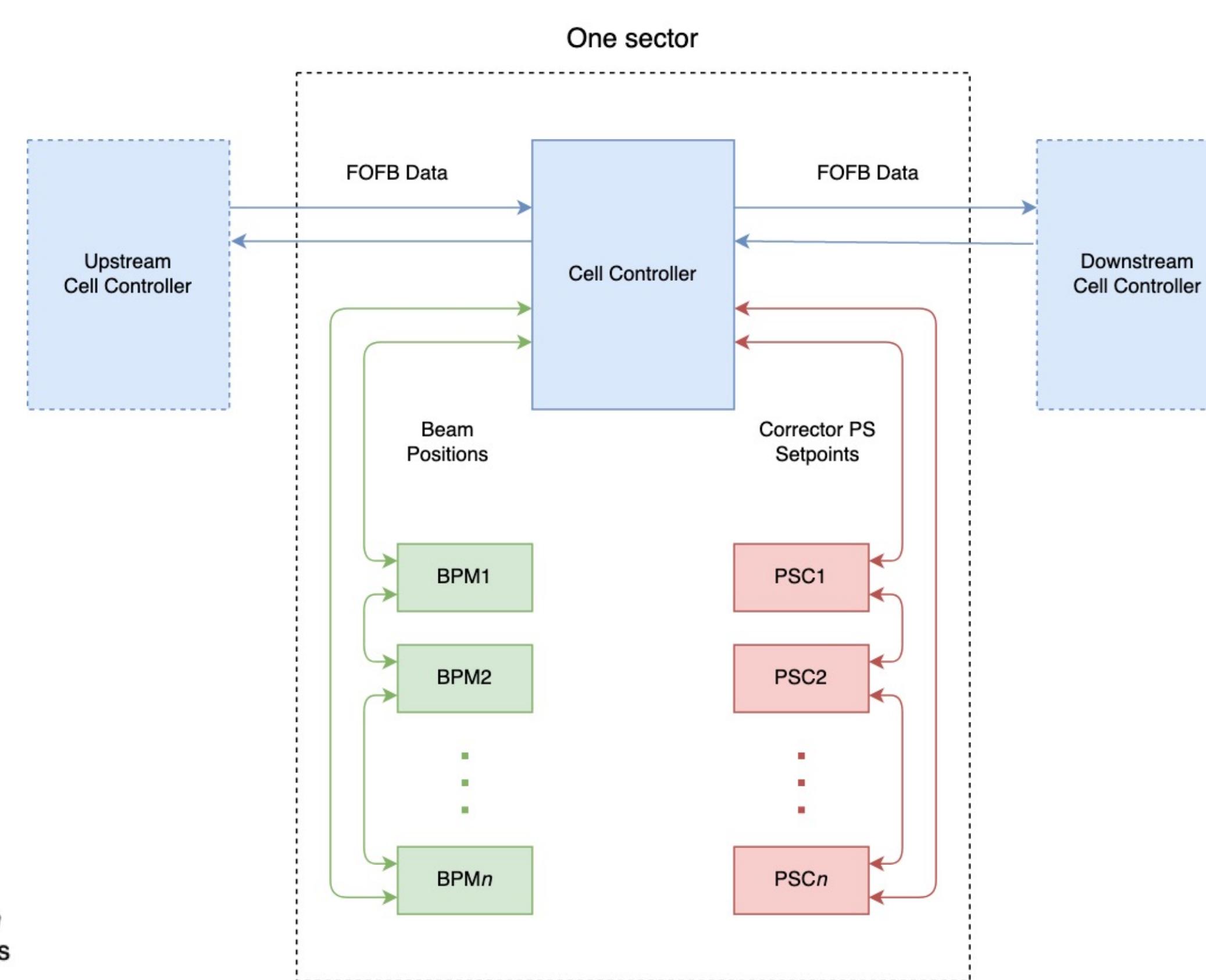
Orbit Stability

Orbit stability instrumentation includes FOFB and BPM systems, based on existing ALS designs. Each sector contains a cell controller that collects all the local sector BPM position data, sends the data on the FOFB network to all other cell controllers, collects all position data from other cell controllers, calculates the local corrector power supply setpoints, and sends them to the local corrector power supply controllers (PSCs).

BPM system block diagram, including BPM readback electronics, pilot tone generator, and pilot tone combiner.



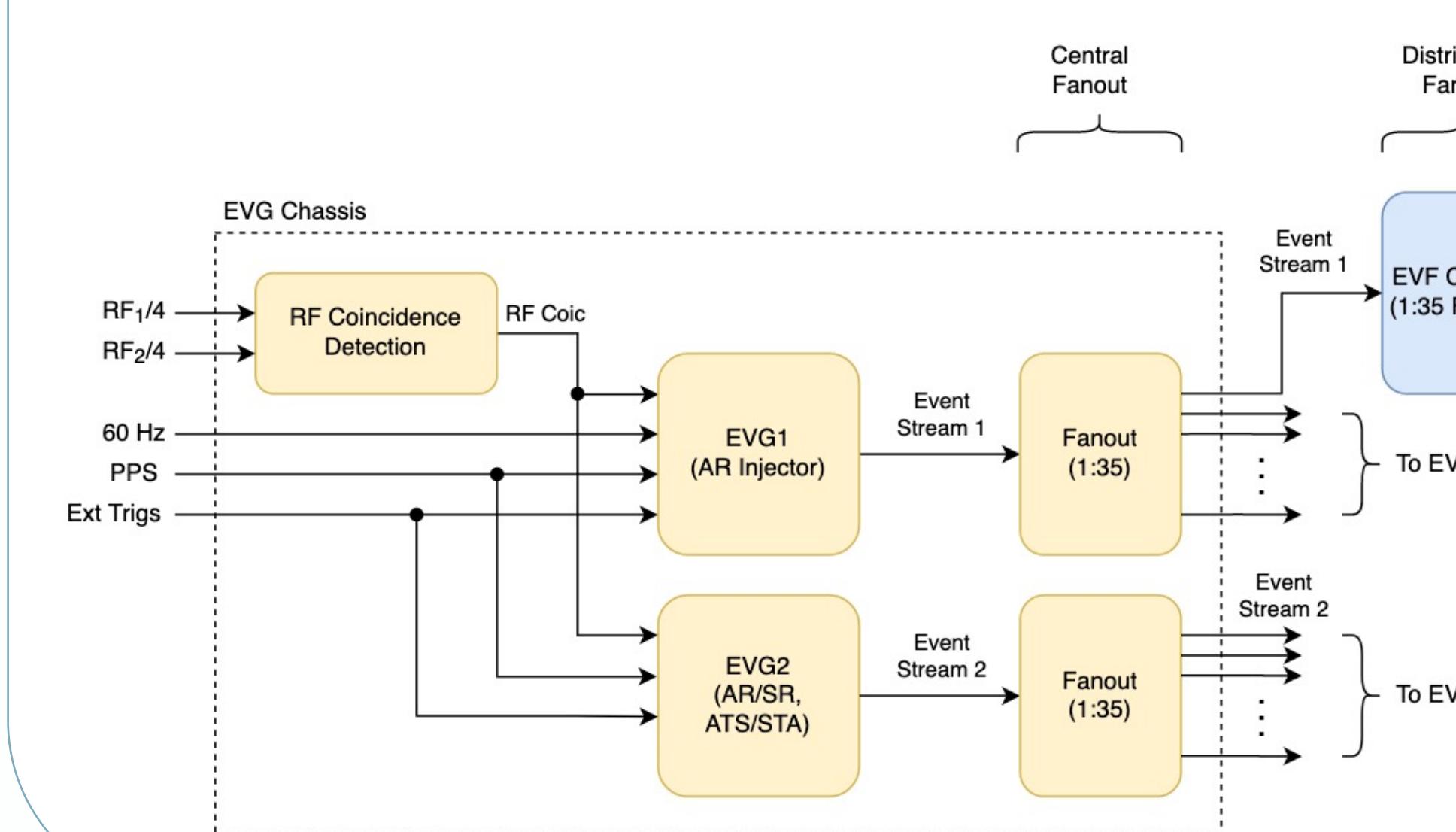
Fast Orbit Feedback system architecture block diagram, including cell controllers, BPMs and corrector PSCs.



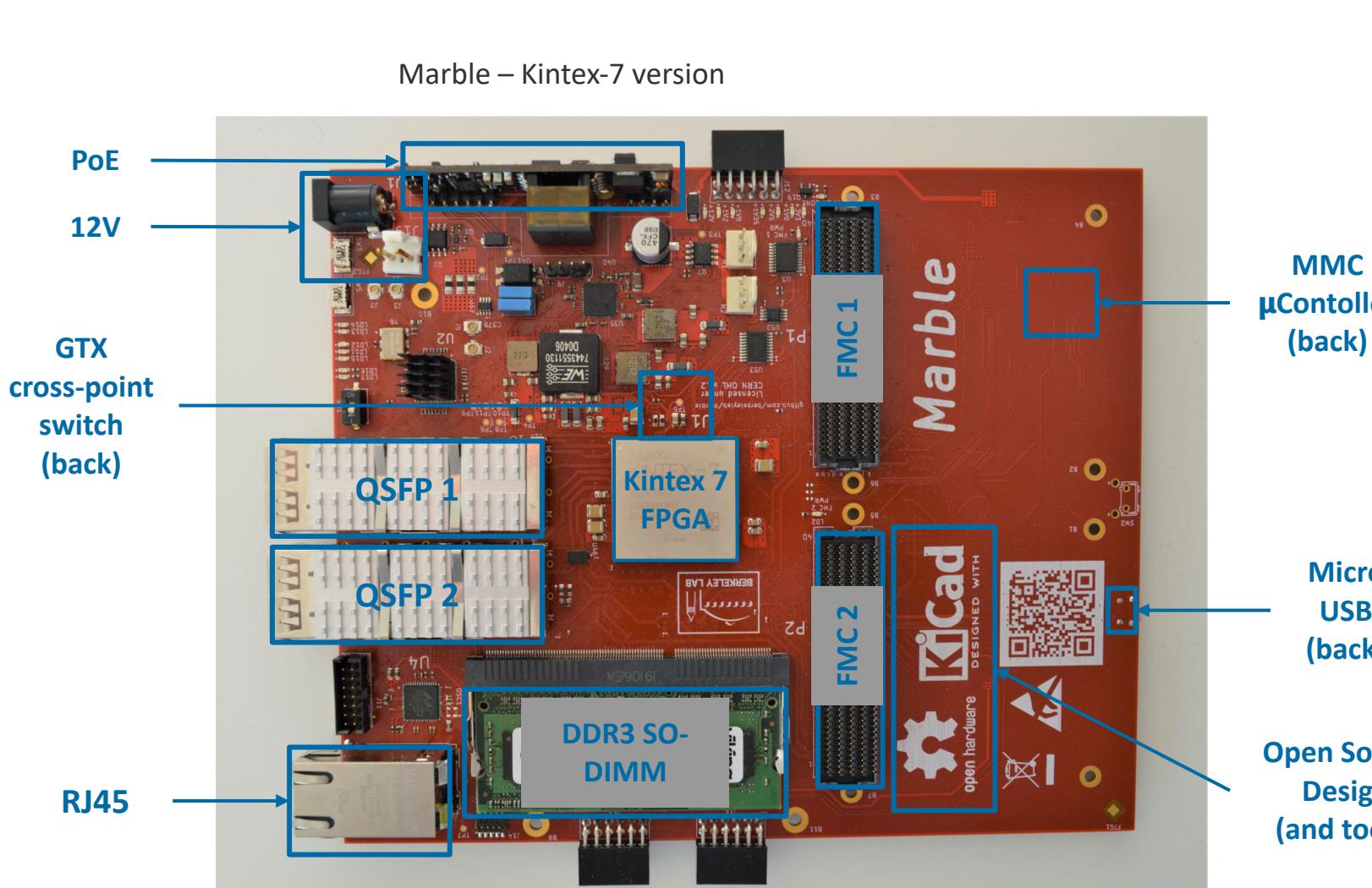
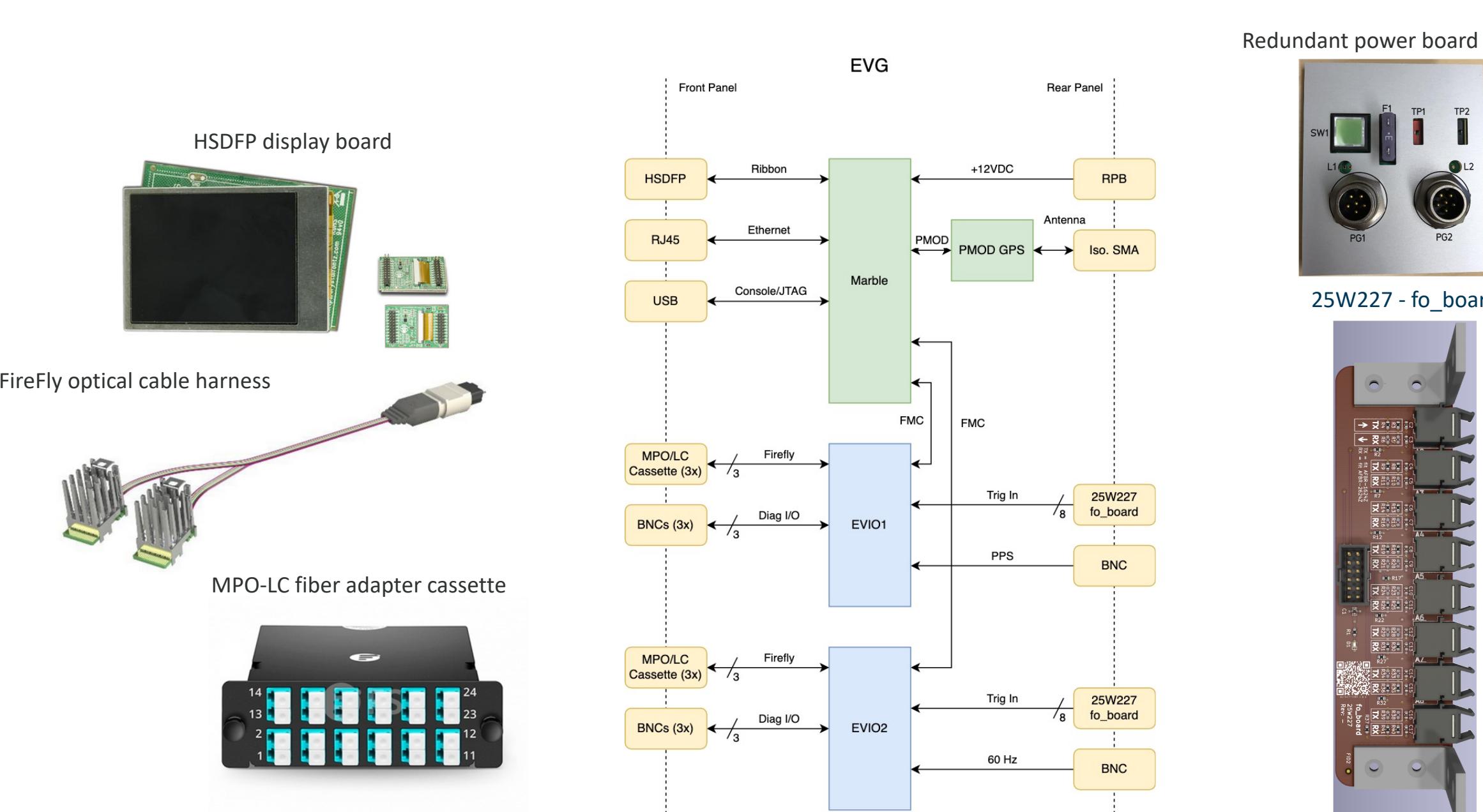
Timing

All event hardware, including Event Generator (EVG), Event Fanout (EVF), and Event Receiver (EVR) chassis are designed by LBNL. Since the existing ALS injector sections (Gun, Linac, Booster ring) remain after the ALS-U upgrade, the timing event protocol must be compatible with existing ALS timing system hardware in the injector.

Timing system architecture block diagram, including separate event stream generation and distribution for two RF frequency domains.



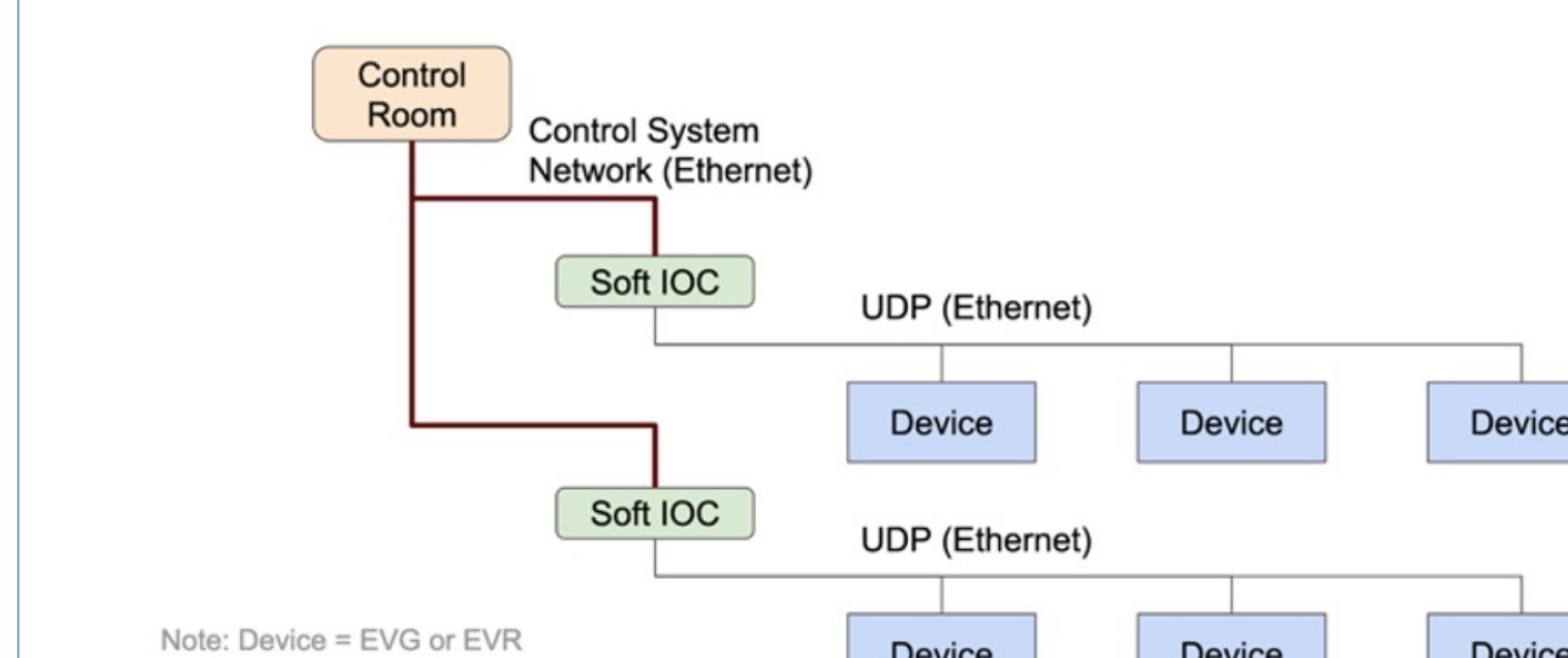
Event Generator (EVG) chassis block diagram, and key components.



Network-attached device (NAD) model

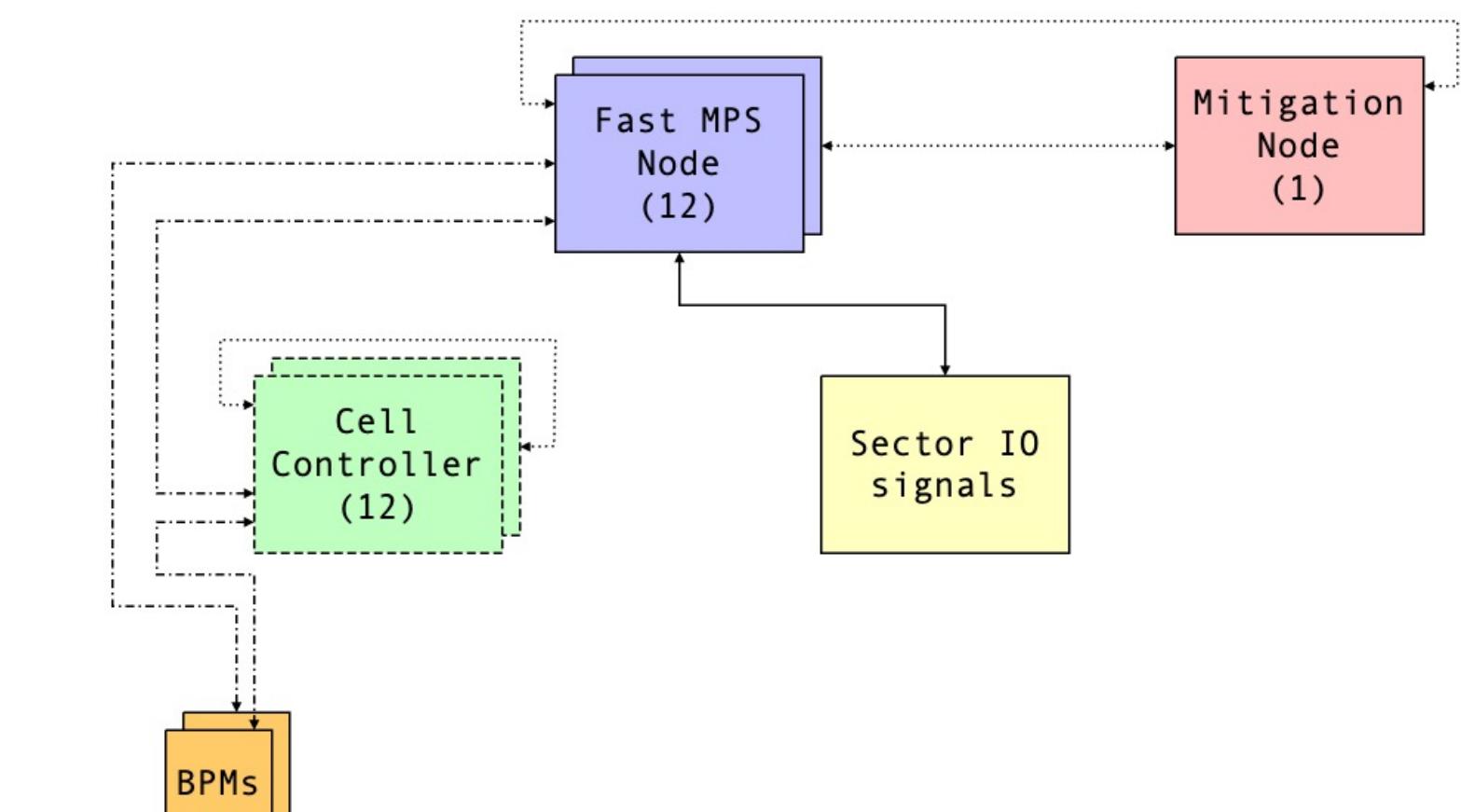
ALS-U Instrumentation systems use a network-attached device (NAD) model, in which electronic devices communicate with soft IOCs over a simple Ethernet UDP interface, as shown in Fig. 1. The architecture is flexible in that the number of soft IOCs required to support devices and how they are connected can be adjusted to trade off network bandwidth, CPU performance, and maintenance complexity.

Example network-attached device (NAD) architecture.



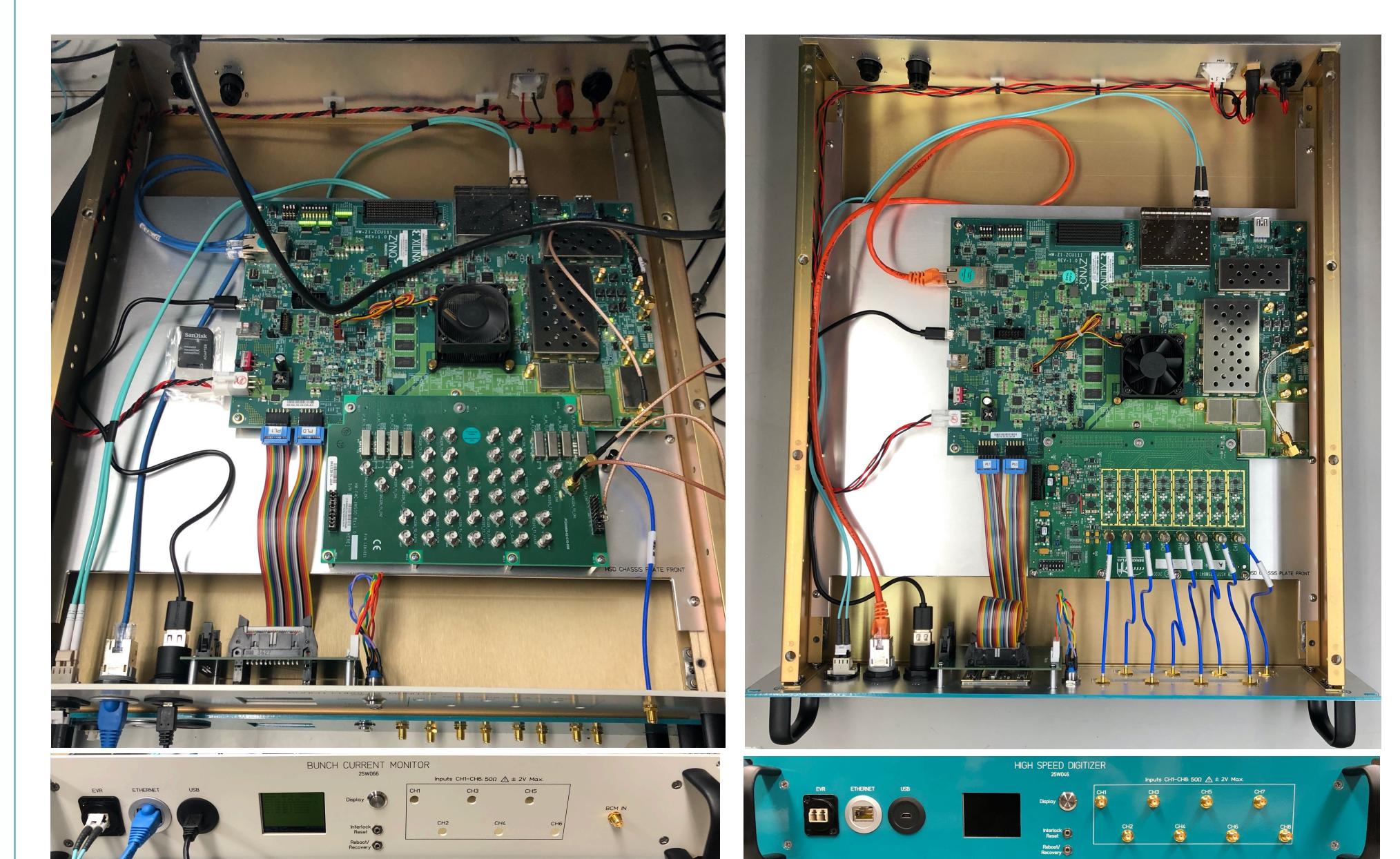
Fast MPS

Fast MPS system architecture block diagram, including sector nodes and mitigation node.



Fast Acquisition

ALS Bunch Current Monitor (left) and High Speed Digitizer (right).



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