MICROTCA.4 BASED OPTICAL FRONTEND READOUT ELECTRONICS AND ITS **APPLICATIONS**



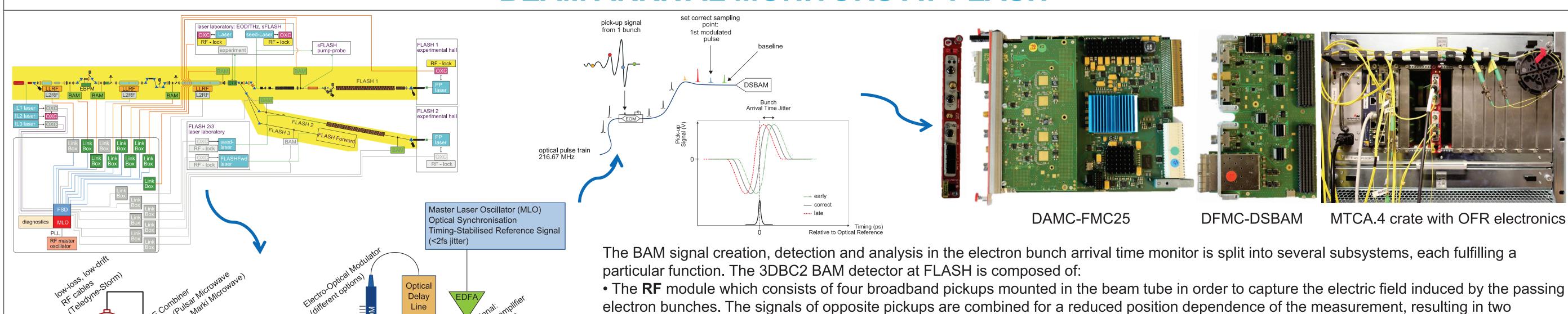
K. Przygoda*, L. Butkowski, M. K. Czwalinna, H. Dinter, C. Gerth, F. Ludwig, S. Pfeiffer, H. Schlarb,

C. Schmidt, M. Viti, Deutsches Elektronen-Synchrotron, Germany

R. Rybaniec, E. Janas, Warsaw University of Technology, Warsaw, Poland

Abstract In the paper we want to present the MicroTCA.4 based optical frontend readout (OFR) electronics and its applications for beam arrival time monitor (BAM) and fast beam based feedback (BBF). The idea is to have a possibility to monitor the modulation density of the optical laser pulses by the electron bunches and apply this information for the BBF. The OFR composed of double width fast mezzanine card (FMC) and advanced mezzanine card (AMC) based FMC carrier. The FMC module consists of three optical channel inputs (data and clock), two optical channel outputs (beam arrival time), 250 MSPS ADCs, clock generator module (CGM) with integrated 2.8 GHz voltage control oscillator (VCO). The optical signals are detected with 800 MHz InGaAs photodiodes, conditioned using 2 GHz current-feedback amplifiers, filtered by 3.3 GHz differential amplifiers and next direct sampled with 16-bits 900 MHz of analog bandwidth ADCs. The CGM is used to provide clock outputs for the ADCs and for the FMC carrier with additive output jitter of less than 300 fs rms. The BAM application has been implemented using Virtex 5 FPGA and measured with its performance at Free Electron LASer in Hamburg (FLASH) facility.

BEAM ARRIVAL MONITORS AT FLASH

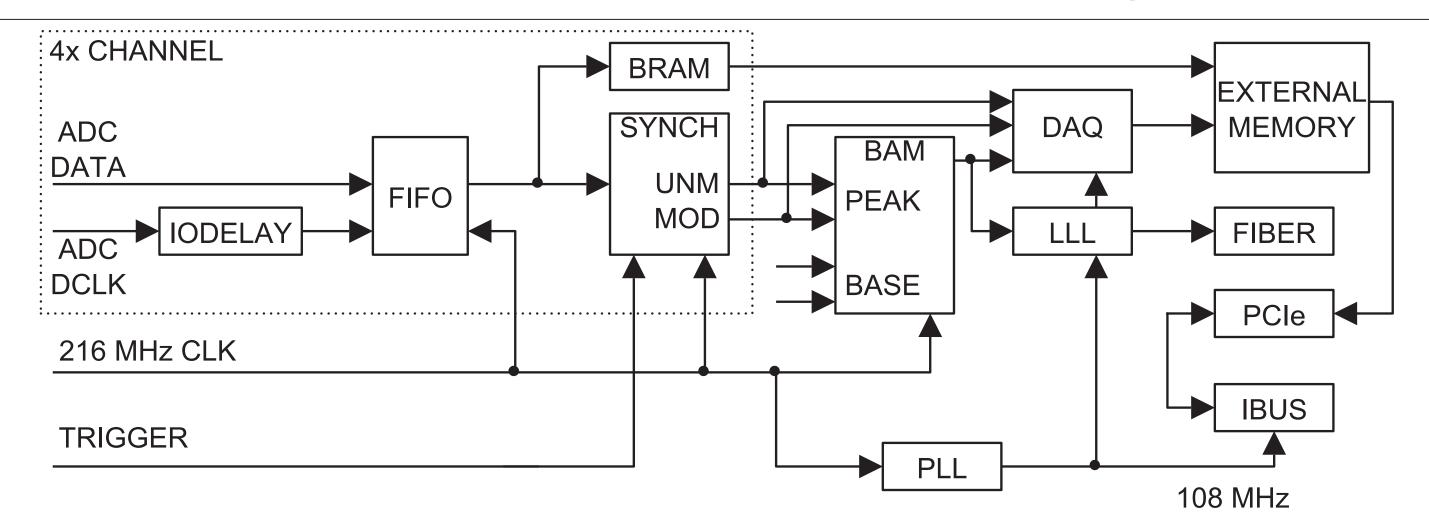


independent RF channels for the arrival time detection: coarse and fine. • The electro-optical modulator (EOM) unit translating the RF signal into an amplitude modulation of time-stabilized, ultra-short laser pulses

• Electronics for signal readout and control of the individual subsystems. This part also performs communication with high-level control systems.

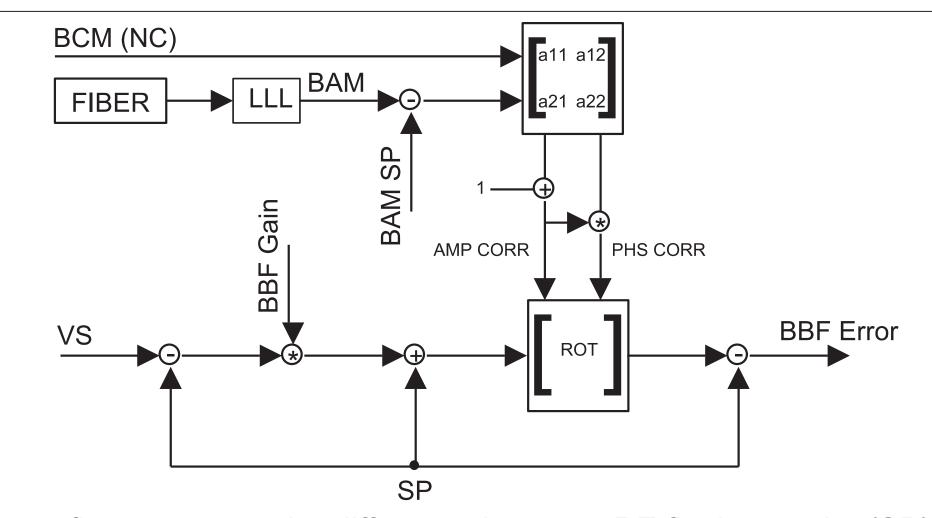
provided by the Master Laser Oscillator (MLO) synchronization system in order to achieve a high temporal sensitivity.

FPGA IMPLEMENTATION



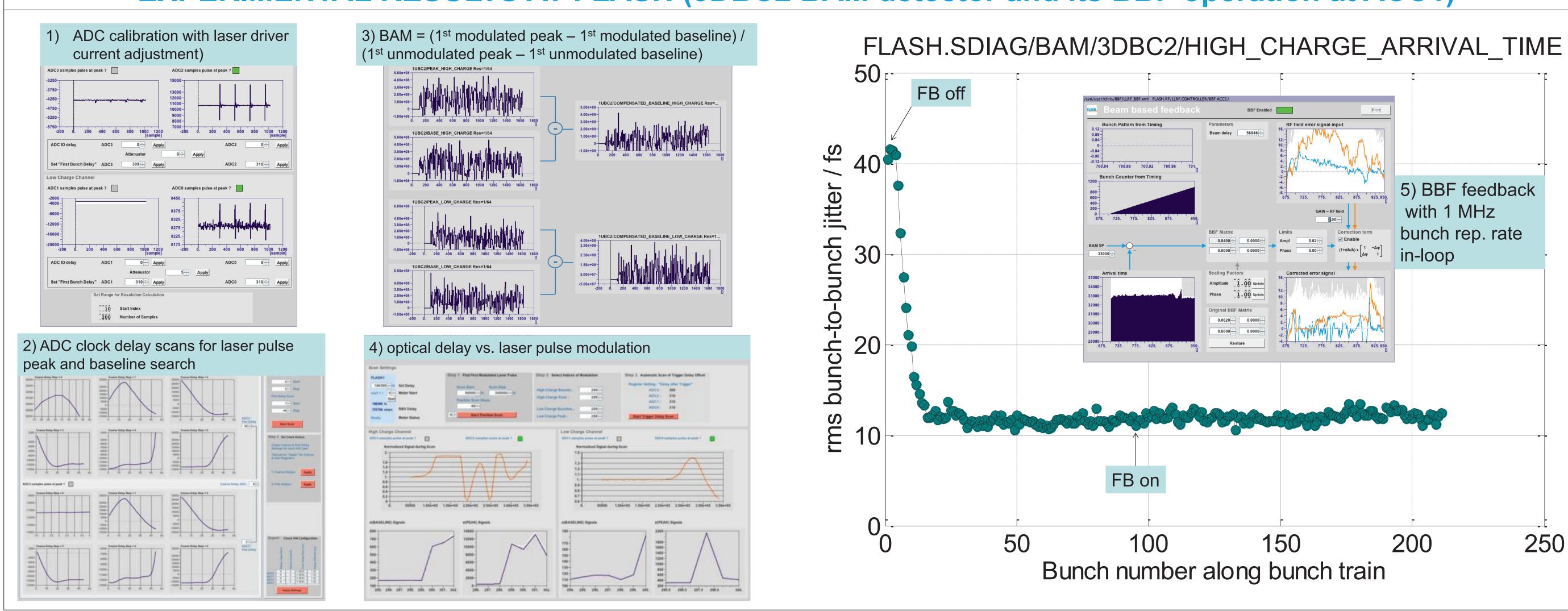
MicroTCA.4 based OFR

The OFR electronics firmware is processing two independent bunch arrival monitor (BAM) channels: The BBF firmware first computes the difference between RF field set-point (SP) and vector the peak and baseline of the optical pulse digitized by two ADCs. FIFO memories store ADC data sum (VS). The resulting field error is scaled by BBF Gain, which is one in case of no beam, using the 216 MHz ADC data clock (DCLK). IODELAY component allows shifting of the input clock to otherwise a user defined value. Next the field error is modulated by the beam error (AMP match the data lines from the ADC. The 216 MHz system clock is applied to the second port of the CORR and PHS CORR), which is done around the SP. The beam error is computed from FIFO. The 1024 data points are stored in the BRAM memory in the FPGA with full 216 MSPS bunch arrival monitor set-point (BAM SP) and bunch compression measurements. The acquisition frequency for PLL delay adjustments. The SYNCH block synchronizes the data from the FIFO to align with the input TRIGGER and match with the electron bunches. The BAM component uses information from two SYNCH blocks (two pairs of unmodulated and modulated pulses) to compute the bunch arrival time (BAT). Computed BAT is then sent to the main controller via a 3.125 Gbps fiber link using the proprietary LLL protocol. The BAT so as the other variables are stored in the data acquisition (DAQ) block for the post-processing with the high level software (HLS). The HLS also provides the configuration parameters by the PCIe bus. Internal registers in the FPGA are addressed using the internal bus (IBUS). Internal PLL in the FPGA synthesizes the divided 108 MHz clock which is used for components outside of the processing pipeline which do not require low latency operation.



beam scaling factor is a part of the transformation matrix $\widehat{G^{-1}} = \begin{bmatrix} a11 & a12 \\ a21 & a22 \end{bmatrix}$, where $\widehat{G^{-1}}$ is a matrix whose elements correspond to the weighting of bunch arrival time and bunch compression measurements, respectively. A limiter for beam related amplitude and phase is implemented to avoid undesired large field changes if one of the beam measurements is corrupted. Within the limits, the input is fed through to the output, while the output is truncated in case of reached predefined limits. Furthermore, the set-point correction is done by a manipulation [rot] of the predefined RF field set-point, leading to a beam based correction (BBF error).

EXPERIMENTAL RESULTS AT FLASH (3DBC2 BAM detector and its BBF operation at ACC1)



*Email: konrad.przygoda@desy.de