



# Nominal Device Support (NDSv3) as a Software Framework for Diagnostics

R. Lange, ITER Organization

M. Astrain, V. Costa, S. Esquembri, D. Rivilla, M. Ruiz, Universidad Politécnica de Madrid

J. Moreno, D. Sanz, GMV Aerospace and Defence



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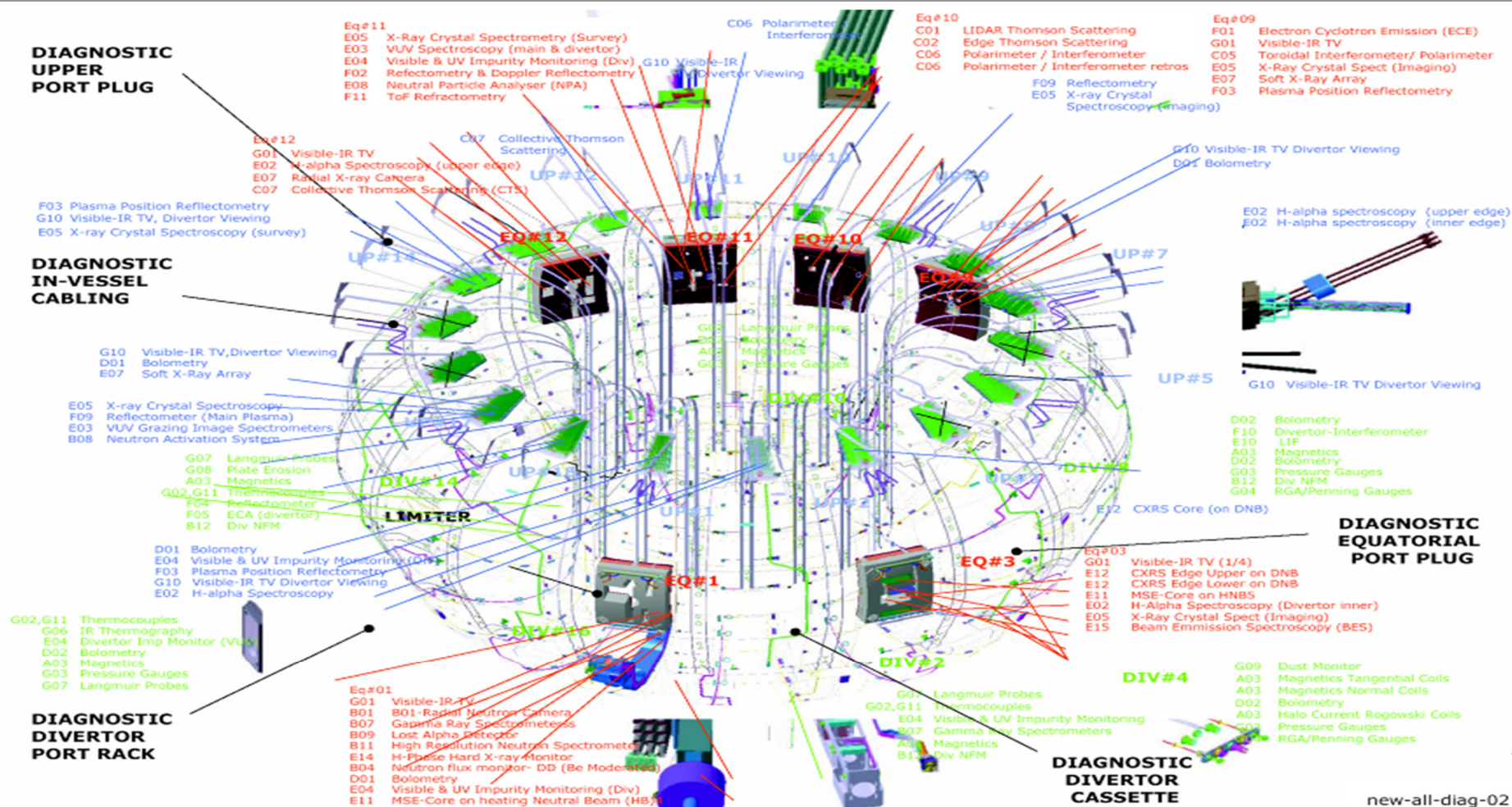
18th International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS2021),

14-22 October 2021

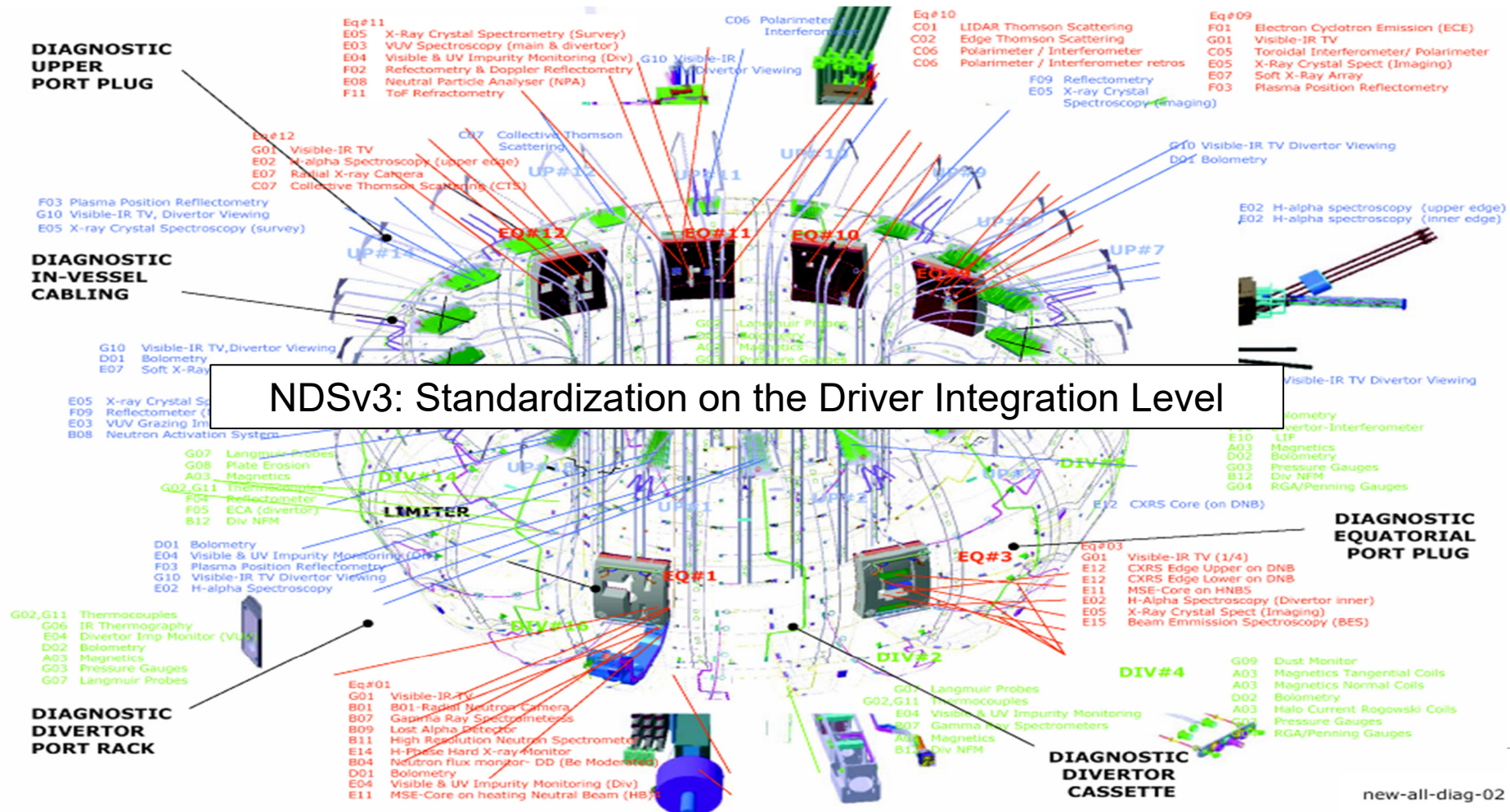
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# Motivation



# Motivation





# NDSv3 as a SW Framework for Diagnostics

- Nominal Device Support (NDS) Concept
- Main NDS Software Layers and Interfaces
- NDS Device Drivers for PXIe and MTCA Boards
- NDS Plugins for ITER Hi-Perf Networks and EPICS
- NDS System for Complex Setups
- Other NDS Solutions: NDS-IRIO-OpenCL
- Conclusions



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# NDS Basics

- Conceived by Cosylab, further developed by ITER partnering with UPM and GMV
- Goal: a driver development framework for ITER diagnostics measurement systems (focusing on DAQ and timing)
  - Small functional blocks (nodes) instantiated to build complex systems
  - Improved code reusability and testability
  - High software quality (automated tests and static code analysis)
  - Comprehensive user and developer documentation
- Allow development and operation using EPICS and other control systems



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# NDS Concepts

- C++ Library (device drivers as plugin libraries)
- Device drivers organized as hierarchy of nodes containing
  - Variables (NDS PVs) for communication
  - State machines
- Collection of standard nodes (base classes) covering
  - Analog input (DAQ), waveform generation, digital I/O
  - Timestamp and Future Time Event generation
  - Management of triggers and clocks
- Standard nodes w/ well-defined NDS PVs and functionality
- Adding a driver = new implementation of standard nodes



# NDS Concepts

- “Control System” API allows running in different contexts
  - Inside a test fixture
  - Inside an EPICS IOC
  - Inside a Tango device server – *not tested*
  - Inside the ITER Real-Time-Framework (RTF) – *planned*

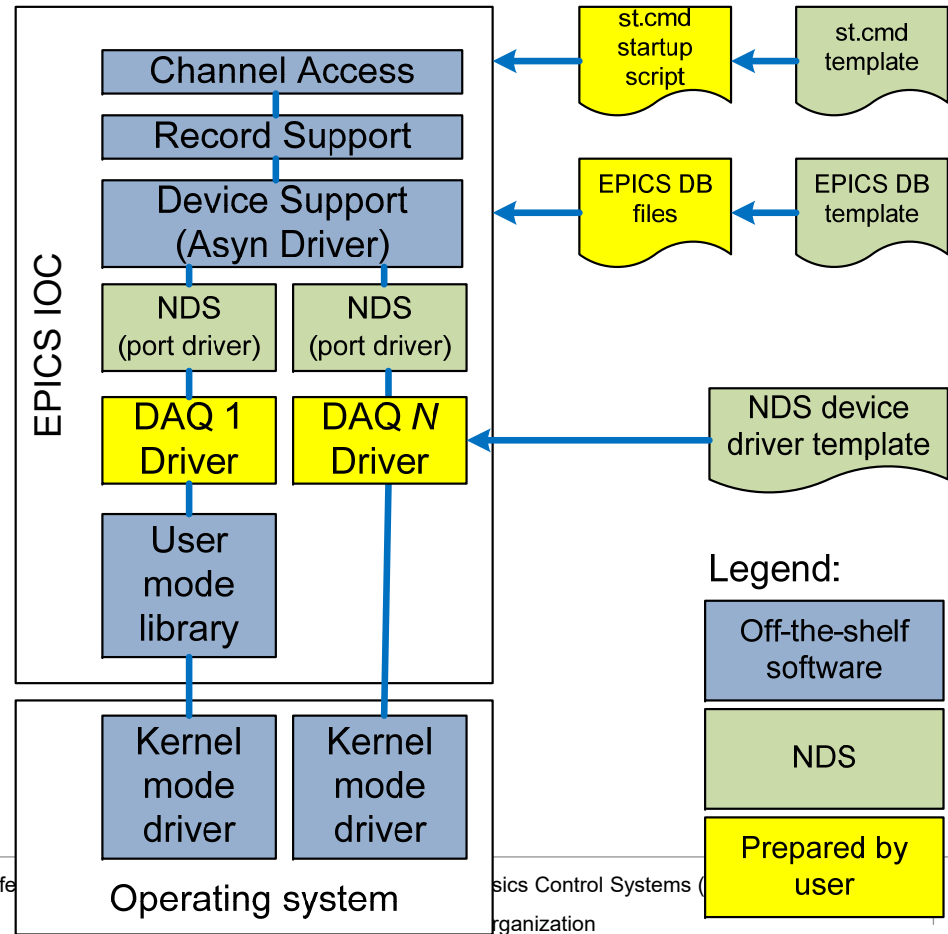


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# NDSv3 Device Inside an EPICS IOC

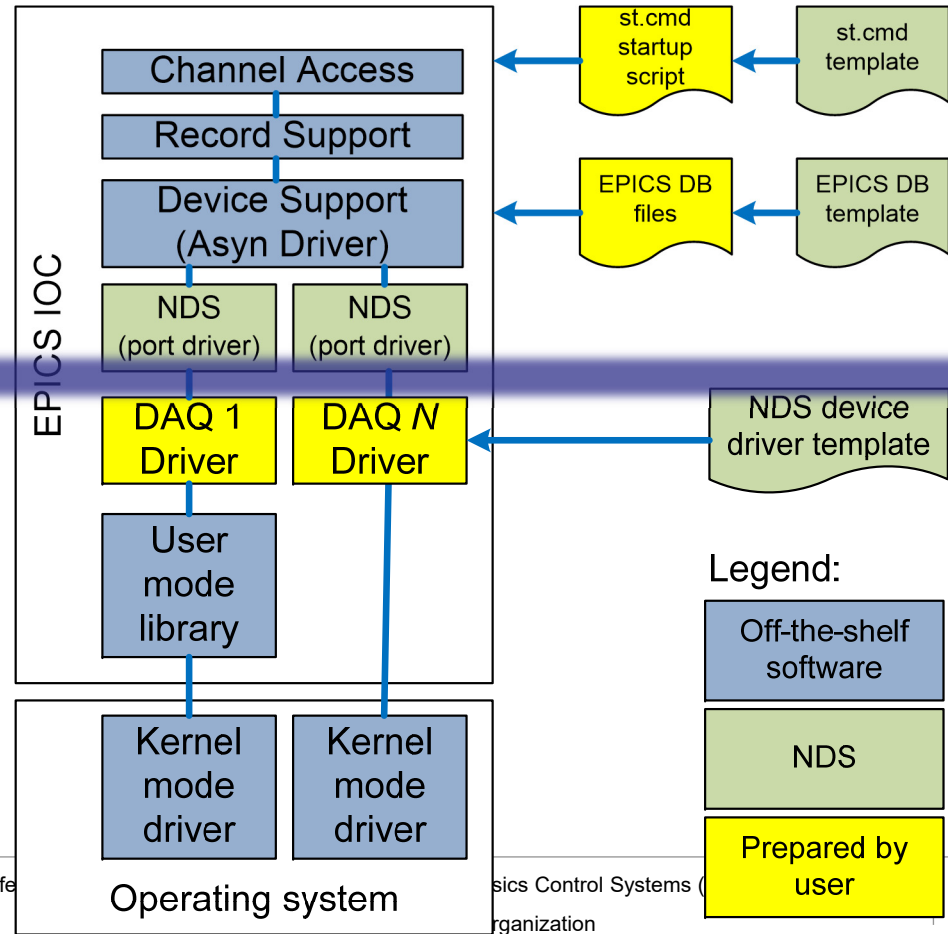
- EPICS Database is used for
  - Configuration
  - Control
  - Monitoring
- Specialized NDS nodes are used for
  - Device communication
  - Hi-perf archiving





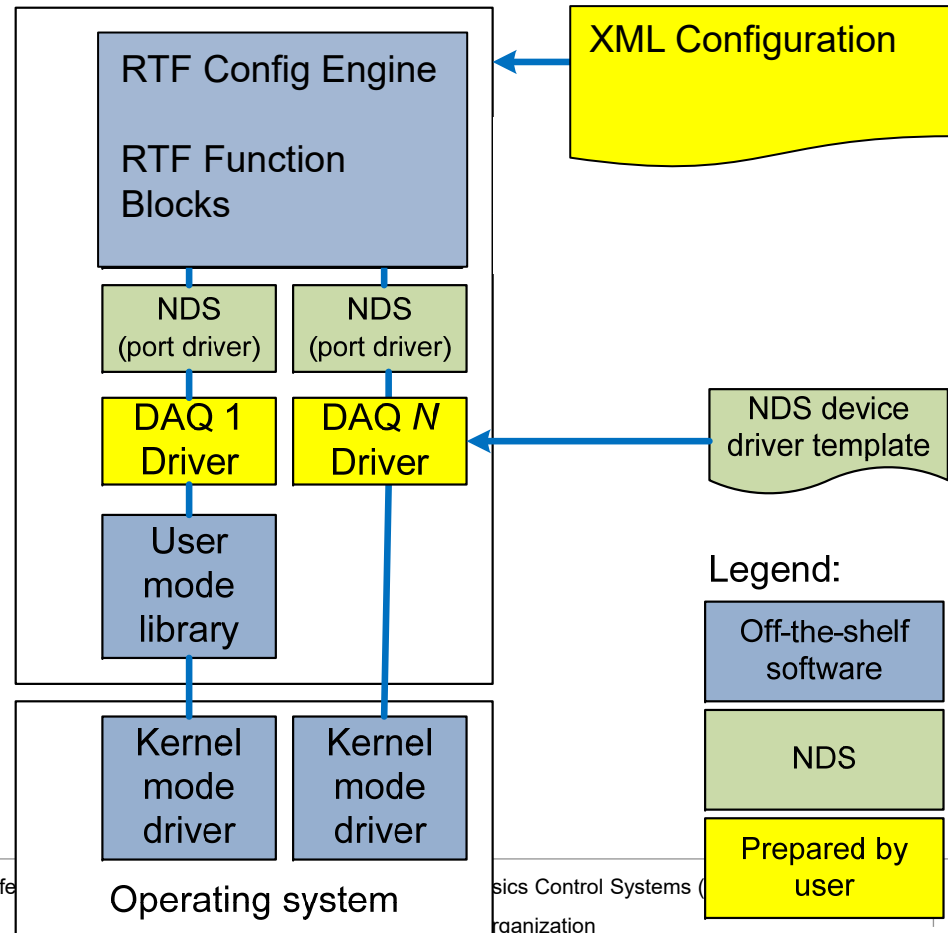
# NDSv3 Device Inside an EPICS IOC

- EPICS Database is used for
  - Configuration
  - Control
  - Monitoring
- Specialized NDS nodes are used for
  - Device communication
  - Hi-perf archiving



# NDSv3 Device Inside a Real-Time-Framework Node

- RTF will be used for
  - Configuration
  - Control
  - Monitoring
- Specialized NDS nodes are used for
  - Device communication
  - Hi-perf archiving



# NDS for PXIe Devices

- From the ITER hardware catalog
  - NI PXI6683H: timing (PTP) and triggering
  - NI X-Series (PXIe6363 and 6368): multi-functional DAQ
  - NI FlexRIO with NI5761 module

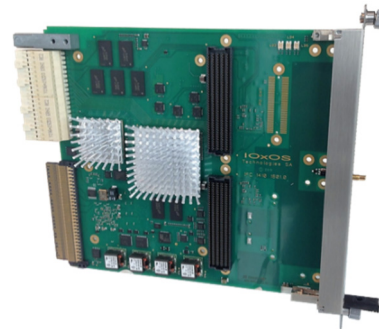
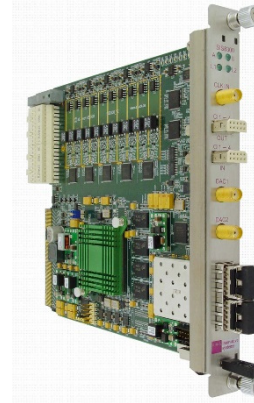


- Other developments (non-ITER)
  - Teledyne ADQ8/ADQ14 (UKAEA for JET/MAST)



# NDS for MTCA Devices

- ITER supported
  - DMCS PTM1588: timing (PTP) and triggering
  - DMCS MFMC FMC Carrier: multi-functional DAQ
- Other developments
  - Teledyne ADQ8/ADQ14 (UKAEA for JET/MAST)
  - IOxOS IFC\_1410 (ESS)
  - Struck SIS8300 (ESS)



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UPM  
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SCIENCE

gmv  
INNOVATING SOLUTIONS

# NDS Plugins: Communication

- NDS-SDN  
Publisher for ITER's real-time communication network
- NDS-DAN  
High-bandwidth stream to ITER's archiving system
- NDS-PVXS  
Integrating COTS devices using EPICS pvAccess
  - Supports read, write, monitor and RPC



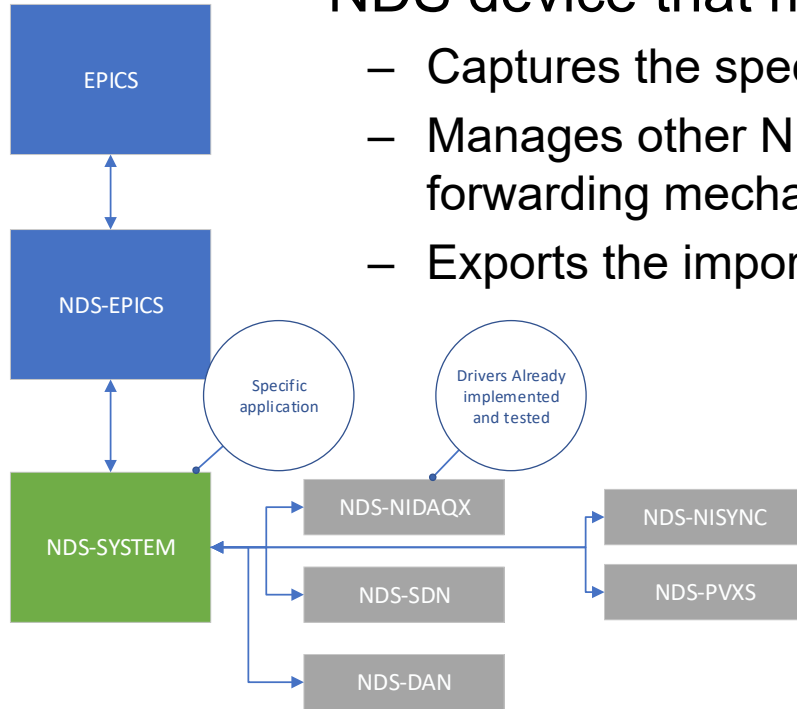
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# NDS System: Complex Setups

- NDS device that manages other NDS devices
  - Captures the specifics of a complex "measurement"
  - Manages other NDS devices through NDS PV value forwarding mechanisms and hierarchical state machines
  - Exports the important NDS PVs to the control system



## Sample NDS System module features

- NDS-NISYNC: Timing and triggering, Backplane routing
- PXIe6368: DAQ, Waveform generation, digital IO
- PVXS: accessing data on external EPICS IOC
- SDN: combining acquired data, timestamp, external data in a published SDN topic
- Hierarchical state machine to control the system
- OPI panel to interact with the NDS-System
- Archiving to DAN (available Q4 2021)



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# NDSv3 for FPGA-Based Systems

- NDS IRIO-OpenCL: UPM in-house development

Covers advanced DAQ/processing systems using SoCs and FPGAs

- Generic NDSv3 driver to interface SoC/FPGA using OpenCL
- Two platforms:
  - FPGA through PCIe on an INTEL host: Intel FPGA (OpenCL SDK)
  - SoC (ARM cpu + FPGA): XILINX (VITIS) and Intel FPGA (OpenCL SDK)
- Integrates traditional DAQ applications and HW accelerators for processing
- Adding machine learning



# Conclusions

- NDSv3 for Diagnostics is in good shape
  - Drivers for basic functionalities for PXIe and MTCA
  - Communication nodes (Real-Time, Archiving, EPICS)
  - Sample application for a complex system
  - Good and comprehensive documentation, high software quality level
  - First users/applications outside of ITER (ESS, UKAEA)
- Thank you!
  - To Cosylab, who initially developed NDS
  - To the groups at UPM and GMV for their great work
  - For your attention



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