

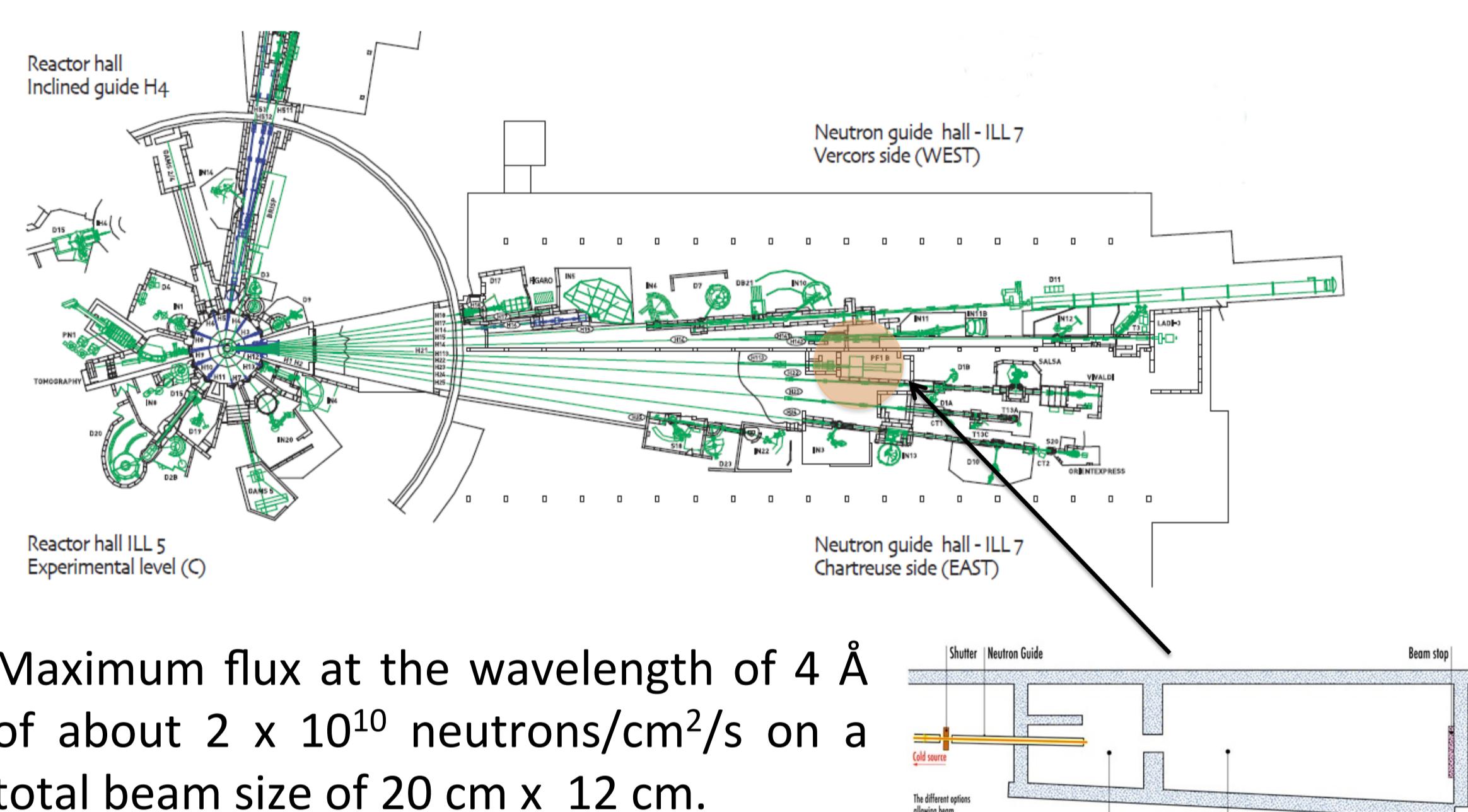
FPGA Implementation Of A Digital Constant Fraction For Fast Timing Studies In The Pico Second Range

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Abstract: Thermal or cold neutron capture on different fission systems is an excellent method to produce a variety of very neutron-rich nuclei. Since neutrons at these energies bring in the reaction just enough energy to produce fission, the fragments remain neutron-rich due to the negligible neutron evaporation thus allowing detailed nuclear structure studies. In 2012 and 2013 a combination of clover and standard coaxial Ge detectors plus very fast LaBr₃(Ce) scintillators has been installed at the PF1B cold neutron beam of the Institut Laue-Langevin (ILL). The present paper describes the digital acquisition system used to collect information on all gamma rays emitted by the decaying nuclei. Data have been acquired in a trigger-less mode to preserve a maximum of information for further off-line treatment with a total throughput of about 10 MByte/sec. Special emphasis is devoted to the FPGA implementation of an on-line digital constant fraction algorithm allowing fast timing studies in the pico second range.

Experimental Setup

PF1B Cold Neutron Beam



Target chamber

Sample holder capable of keeping the sample in a stable and reproducible position. The target material was suspended to the sample holder using a Teflon bag consisting of a foil of 25 mg/cm².



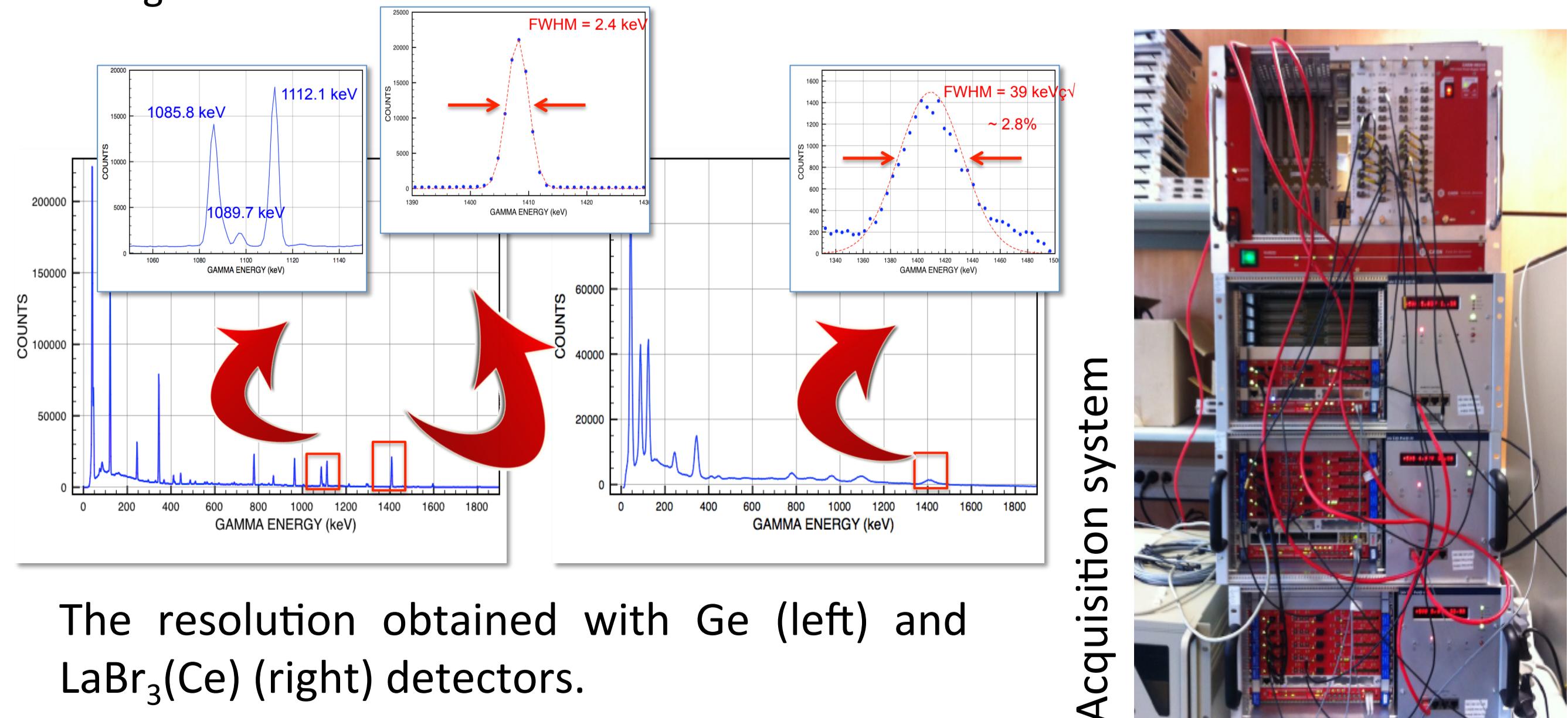
Evacuated inner chamber for the ²⁴¹Pu measurements.

Digital Acquisition

Digitizers: 10 digitizers CAEN v1724, 8 channels, 100MS/s 14 bits.

Processor board: 2 power PC based VME board computer equipped with 256 MB of memory.

Instrument control software: full graphical configuration interface, on line display and data storage.



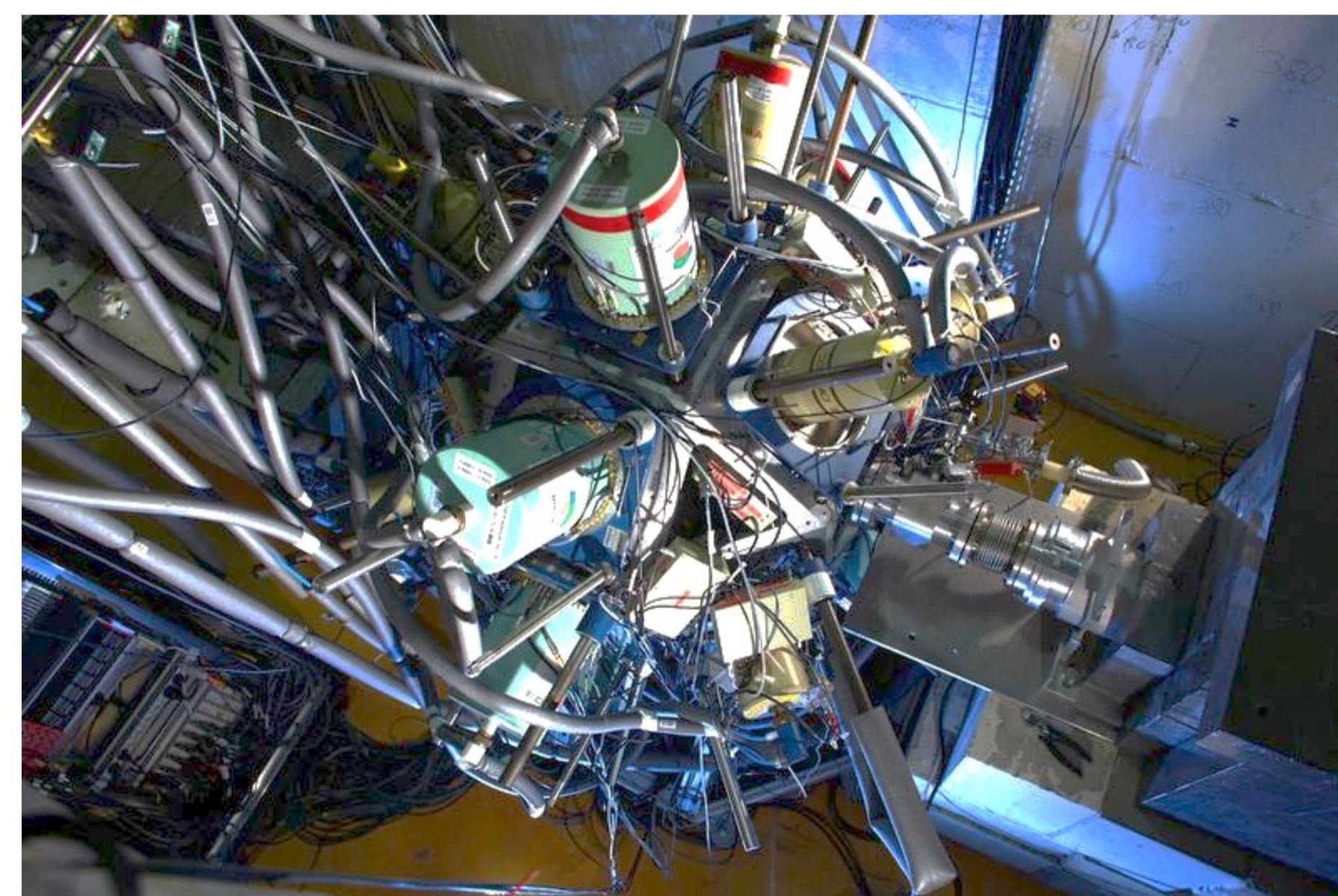
Event rate ≈ 900kHz → Data rate ≈ 7.2 MB/s

Collimation system

To reduce the beam size to match a diameter of about 1 cm at the sample position, we have introduced a series of boron and lithium collimators upstream.

24 different samples have been irradiated in a neutron beam of 10^8 n/cm²/s

Detector array



EXILL campaign 2 cycles → 100 days

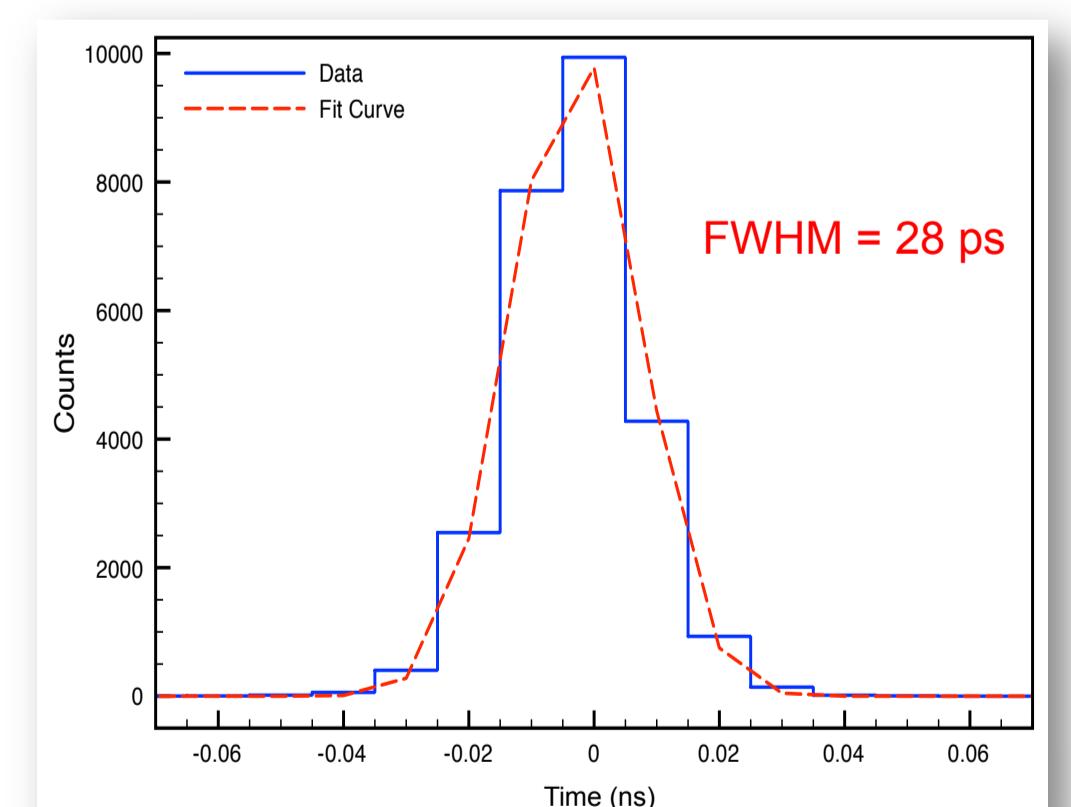
1st cycle: spectroscopy on both stable and ²³⁵U targets

2nd cycle: fast timing with ²³⁵U and spectroscopy with ²⁴¹Pu

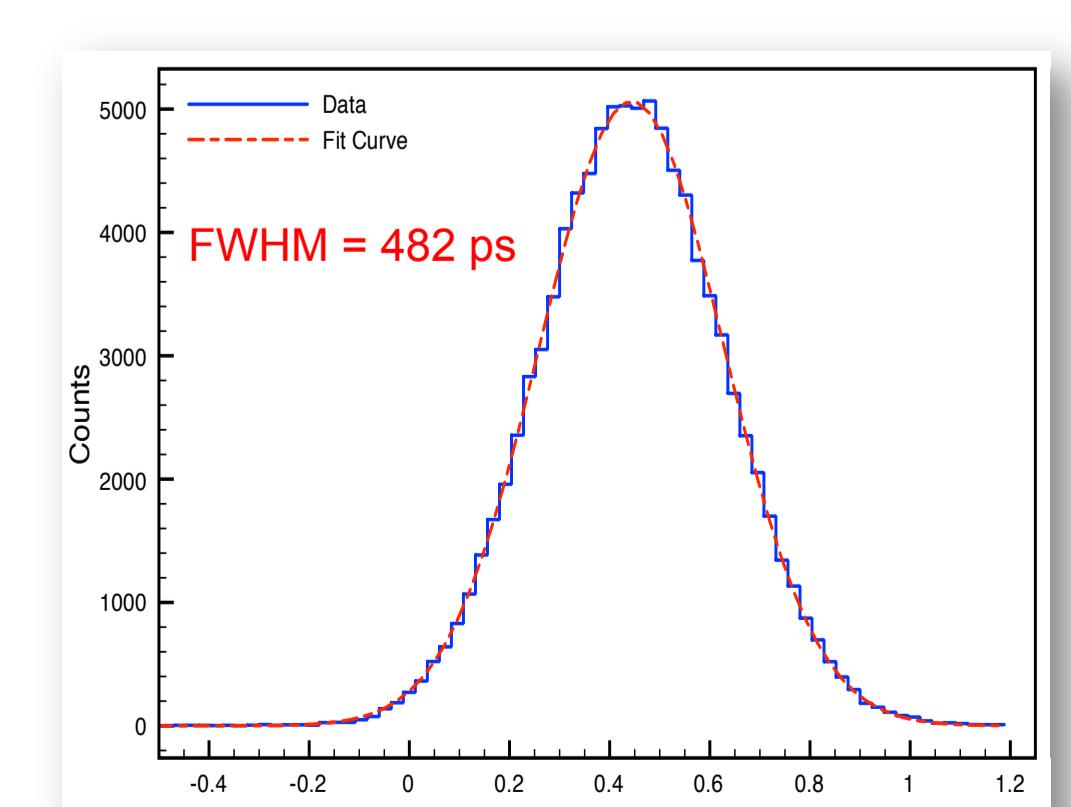
Constant Fraction Discriminator

Features:

- × 6U VME64x board with 2eSST support.
- × Based on latest XILINX Virtex-6T 40nm FPGA.
- × Modular IO Expansion with full front panel access (MPF – Multi-Purpose Front IO).
- × 5V tolerant VME64x P2 user IO with Spartan-6 IO Support.
- × On-board DDR3 Memory.
- × Native PCI Express GEN2 support over VME64x P0 and/or front-end MPF.
- × TOSCA II FPGA architecture:
 - Optimized for XILINX Virtex-6 FPGAs.
 - PCI Express GEN2 EP/RC.
 - Network on Chip (NoC) architecture.
 - Shared Memory.



Time dispersion obtained using a pulse generator sending the same pulse on 2 different digitizer channels.



Time dispersion obtained with two LaBr₃(Ce) detectors placed in front of a ²²Na source.

FPGA implementation of a CFD algorithm in combination with fast digitizers (1GS/s 10 bits) has shown its potential to replace complex analogue chain for fast timing measurements.