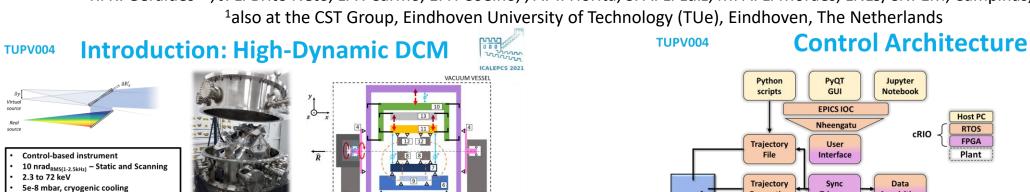
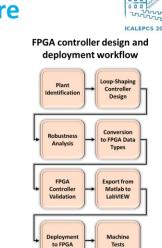
#### THE FPGA-BASED CONTROL ARCHITECTURE, EPICS INTERFACE AND ADVANCED OPERATIONAL MODES OF THE HIGH-DYNAMIC DOUBLE-CRYSTAL MONOCHROMATOR FOR SIRIUS/LNLS



R. R. Geraldes<sup>1,\*</sup>, J. L. Brito Neto, L. P. Carmo, E. P. Coelho, , A. Y. Horita, S. A. L. Luiz, M. A. L. Moraes, LNLS/CNPEM, Campinas, Brazil <sup>1</sup>also at the CST Group, Eindhoven University of Technology (TUe), Eindhoven, The Netherlands



#### Host PC **RTOS** FPGA Plant Acquisition Generation **Triggers FPGA** Actuator HD-DCM Controller Drivers Kinematics Follower Forward Average Sensor Kinematics Filter Drivers Undulator Brasilan Synchrotro Light Laboratory





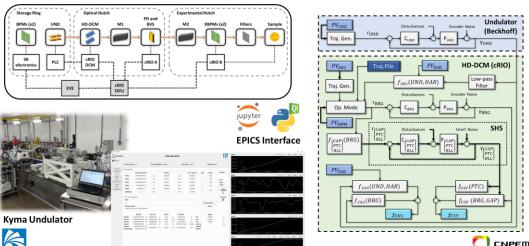
CNPEM

#### **TUPV004**

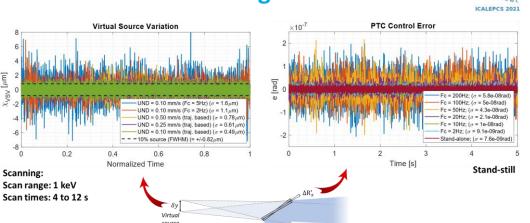
### **Integrated Control Diagram**



CNPEM



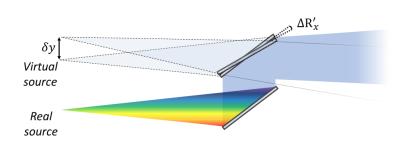
#### **Undulator Integration Results TUPV004**



# **Introduction: High-Dynamic DCM**

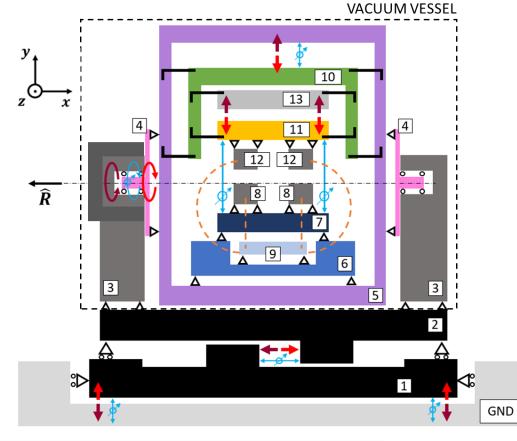


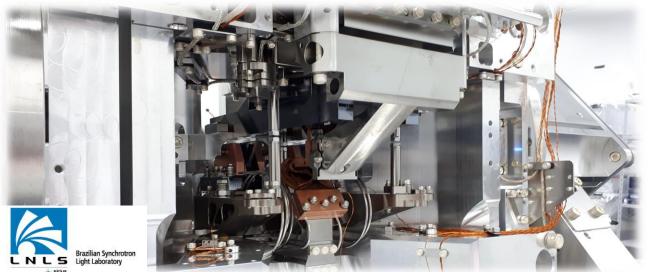
**ICALEPCS 2021** 

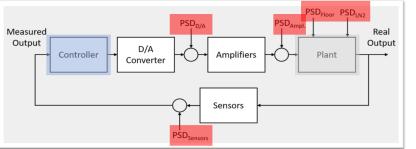


- **Control-based instrument**
- 10 nrad<sub>RMS(1-2.5kHz)</sub> Static and Scanning
- 2.3 to 72 keV
- 5e-8 mbar, cryogenic cooling







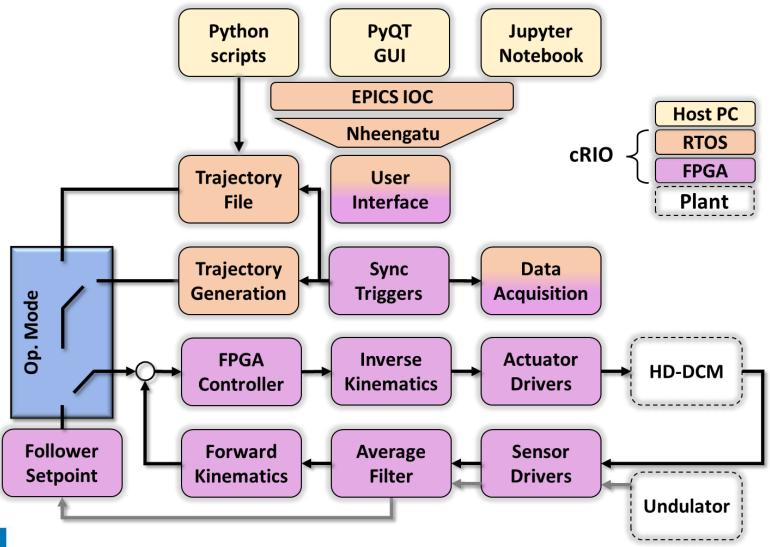




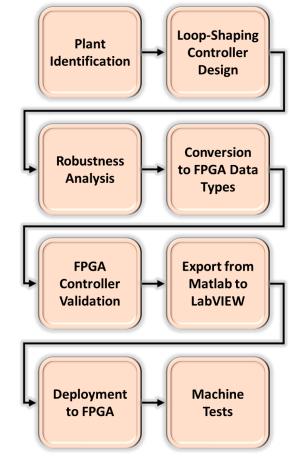


## **Control Architecture**





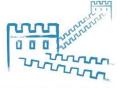
## FPGA controller design and deployment workflow



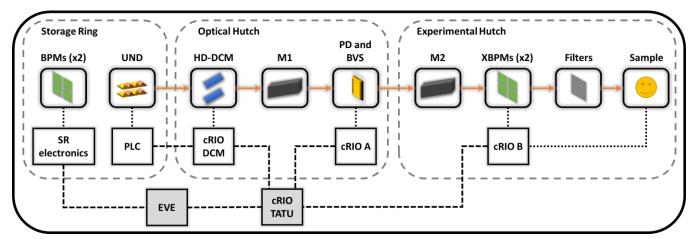




# **Integrated Control Diagram**

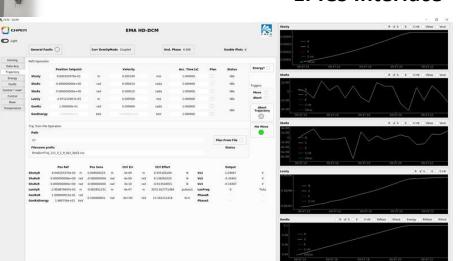


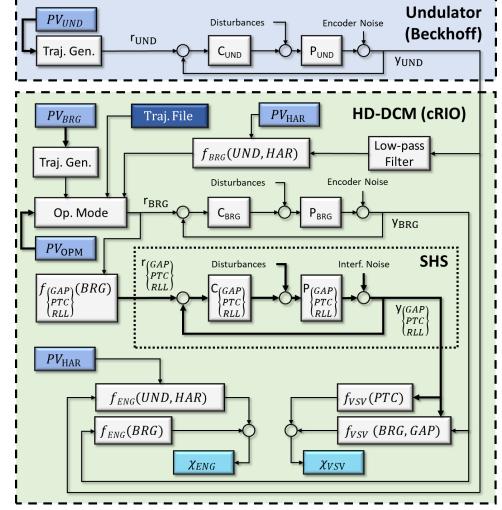






**EPICS Interface** 



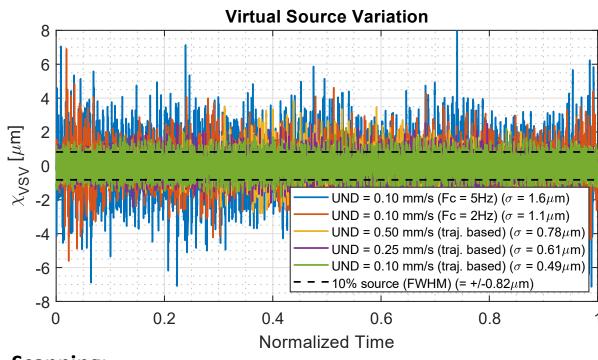


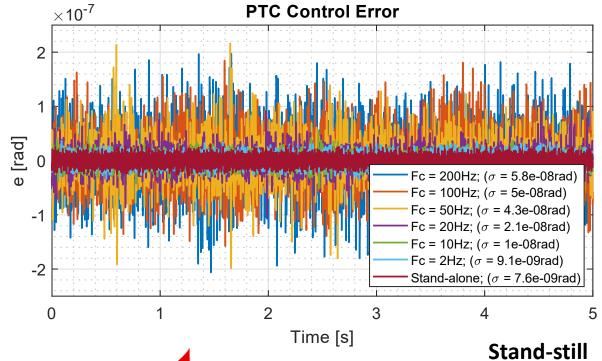




## **Undulator Integration Results**







**Scanning:** 

Scan range: 1 keV

Scan times: 4 to 12 s

