

# White Rabbit Status and Prospects

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ICALEPCS  
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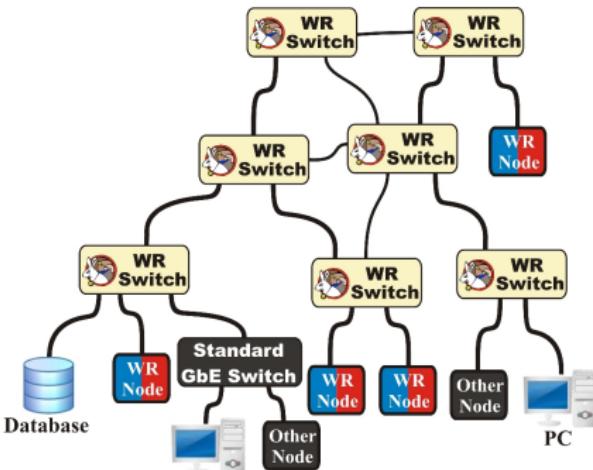
- 1 Introduction
- 2 Applications
- 3 Technology
- 4 Performance
- 5 Current developments
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# Outline

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# White Rabbit: an *extension* of Ethernet

- Bandwidth: 1 Gbps
  - Single fiber medium
  - Up to 10 km links
  - WR Switch: 18 ports
  - Allows non-WR Devices
  - Ethernet features (VLAN) & protocols (SNMP)



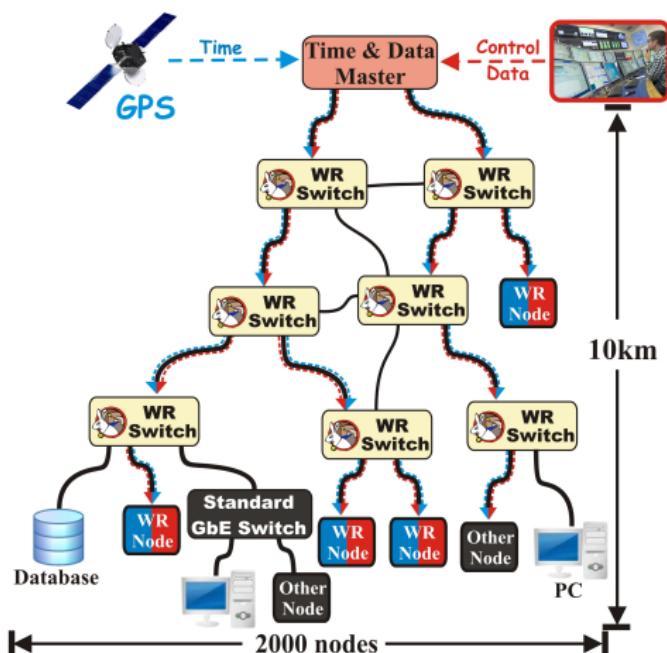
# White Rabbit: an *extension* of Ethernet

Two separate services  
(enhancements to Ethernet)  
provided by WR:

## ① Synchronization:

- accuracy better than 1 ns
- precision in the tens of ps

## ② Deterministic, reliable and low-latency Control Data delivery



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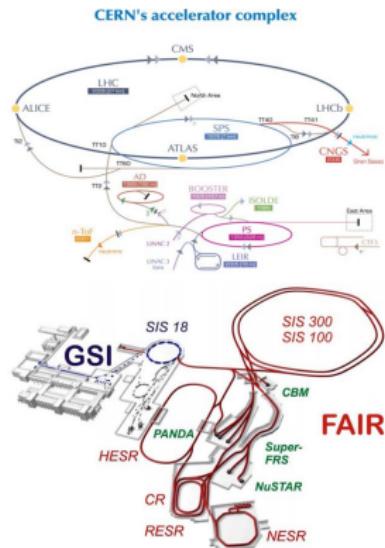
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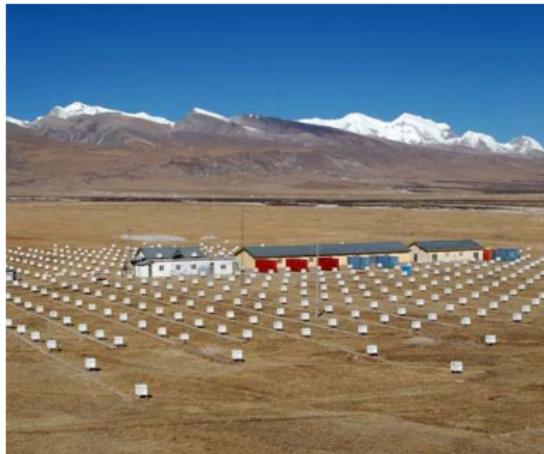
# White Rabbit application examples

- Under development:
  - CERN and GSI



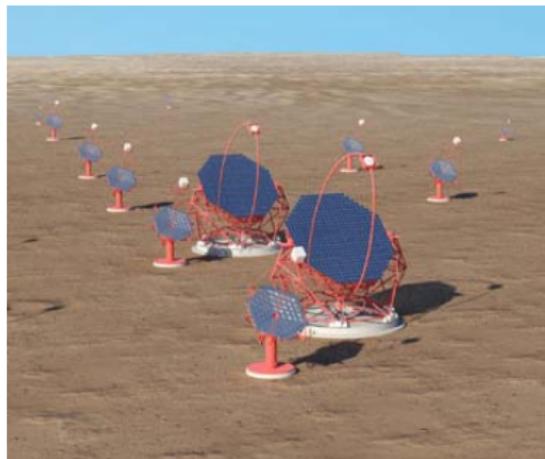
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- Under development:
  - CERN and GSI
  - **The Large High Altitude Air Shower Observatory (China)**



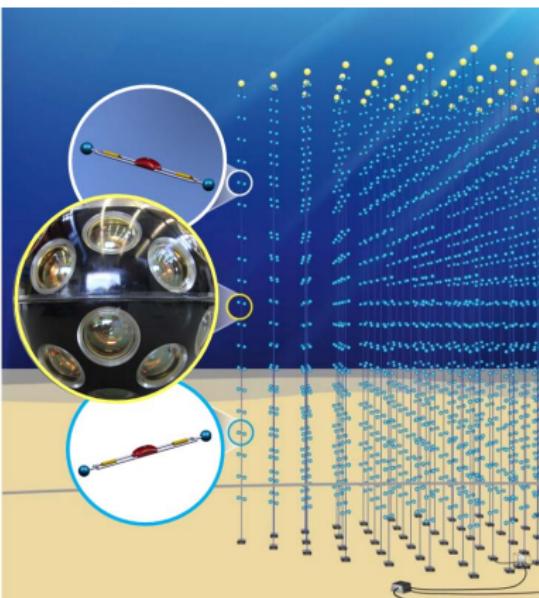
# White Rabbit application examples

- Under development:
  - CERN and GSI
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- Under evaluation:
  - **Cherenkov Telescope Array**



# White Rabbit application examples

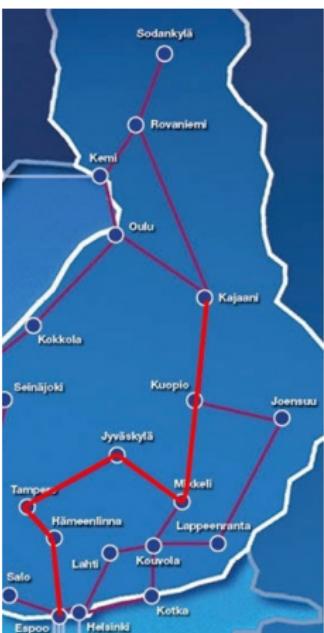
- Under development:
  - CERN and GSI
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  - **European deep-sea research infrastructure (KM3NET)**
  - Long distance Time Transfer



# NL: Time Distribution over 120 km with amplifiers



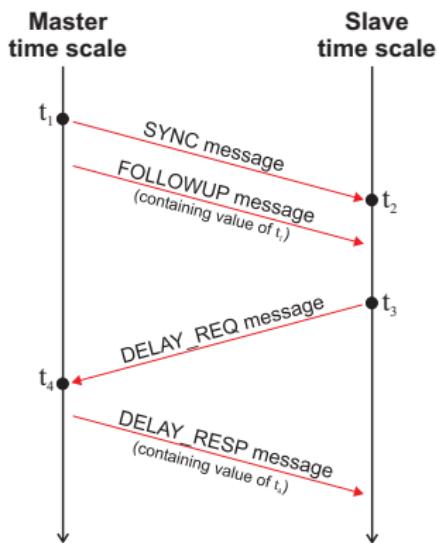
# FI: Time Distribution over 900 km with amplifiers



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# Precision Time Protocol (IEEE 1588)

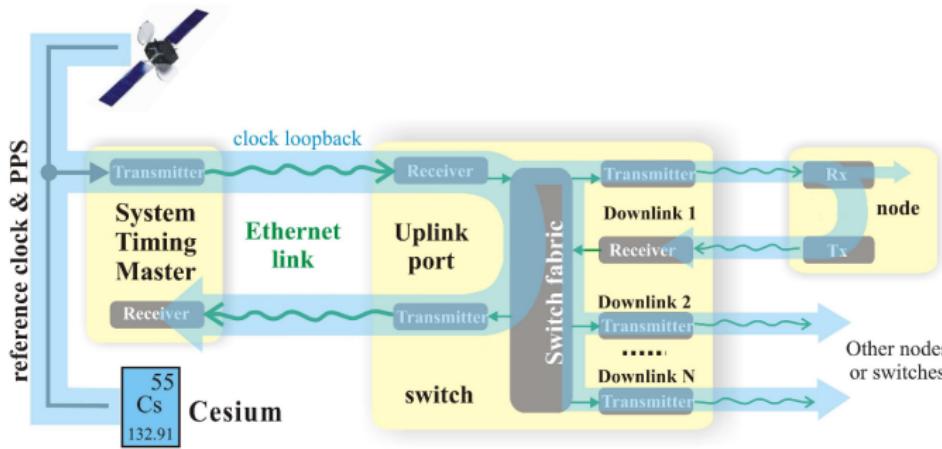


- Frame-based synchronization protocol.
- Synchronizes local clock with the master clock.
- Link delay evaluated by measuring and exchanging frames with tx/rx timestamps.

# Layer 1 Syntonization

Common clock for the entire network

- All network devices use the same physical layer clock.
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip.
- Phase detection allows sub-ns delay measurement.

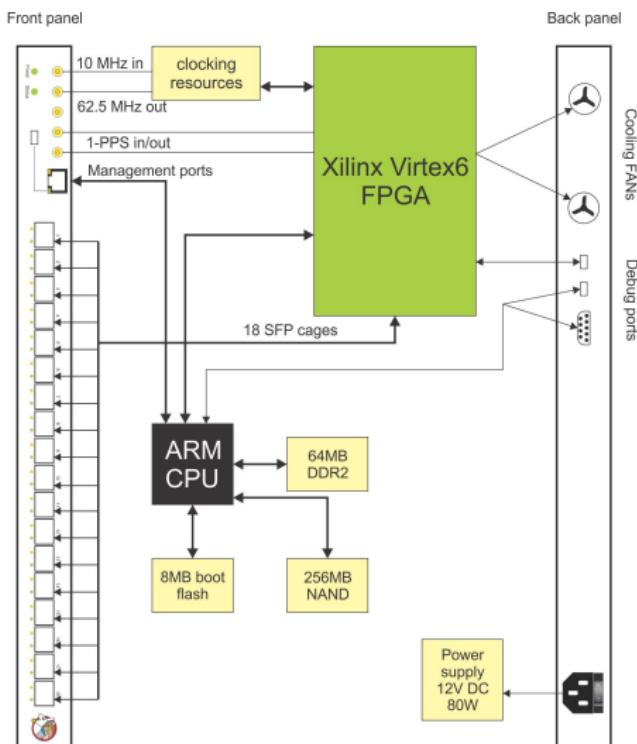


# White Rabbit Switch

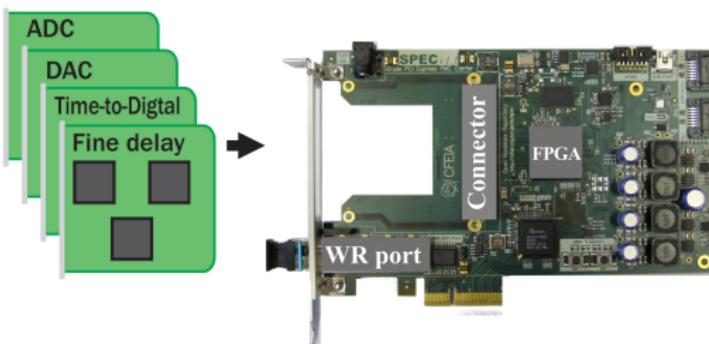


- Central element of WR network
- Original design optimized for timing, designed from scratch
- 18 1000BASE-BX10 ports
- Open design (H/W and S/W)
- Commercially available

# Simplified block diagram of WR switch



# WR Node: SPEC board



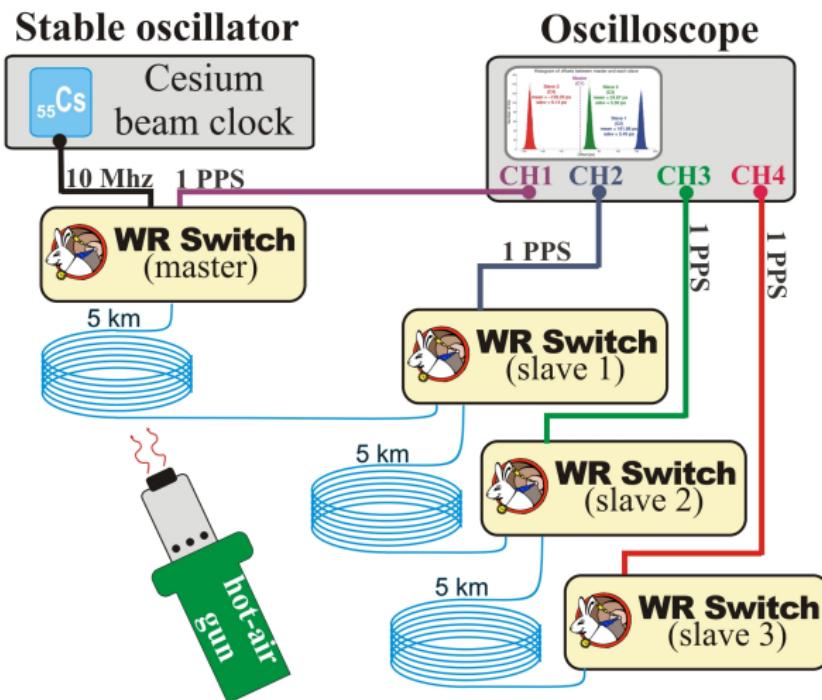
## FMC-based Hardware Kit

- All carrier cards are equipped with a White Rabbit port.
- Mezzanines can use the accurate clock and TAI (synchronous sampling clock, trigger time tag, ...).

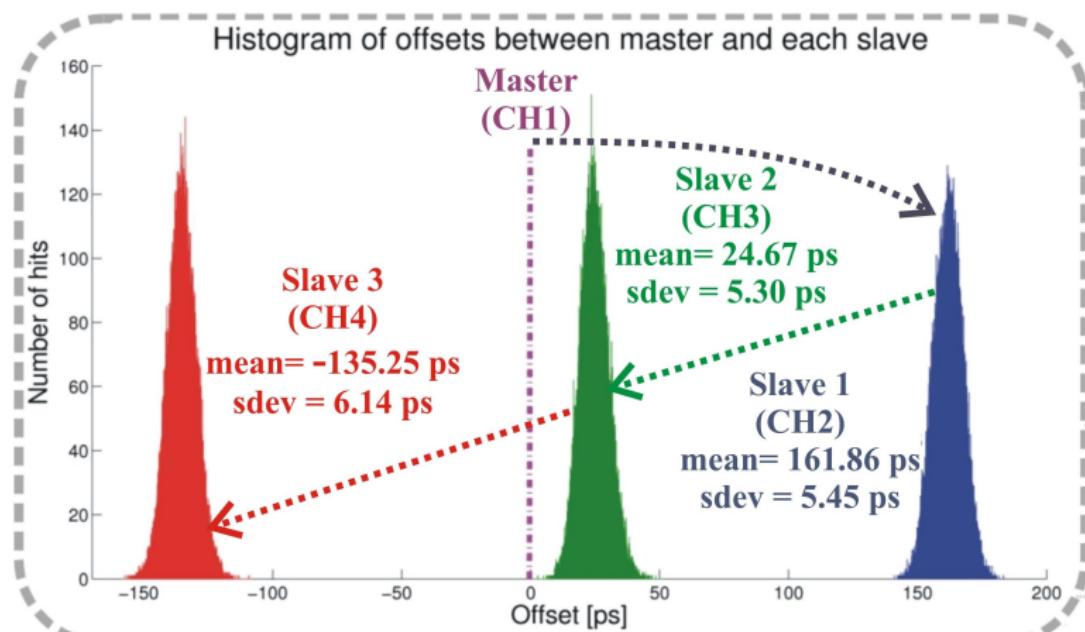
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# WR time transfer performance: test setup



# WR time transfer performance: test results



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You know what the frame latency will be because you have the VHDL source of the switch FPGA. IEEE 802.1Q headers supported.

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## Low latency

Cut-through design. Current latency through the switch is  $\sim 3\mu s$  without much effort. Good for (some) feedback systems.

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## Low latency

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## Suitable for time-based control and data acquisition

Combining a low upper bound in latency and a good common notion of time.

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Work for the switch now revolves around better diagnostics and remote management.

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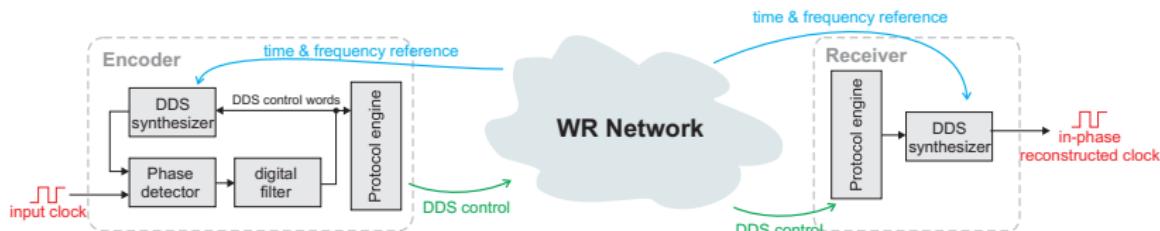
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## Robustness

Based on redundant information and fast switch-over between redundant switches.

# Ethernet Clock distribution a.k.a. Distributed DDS



## Distributed Direct Digital Synthesis

- Replaces dozens of cables with a single fiber.
- Works over big distances without degrading signal quality.
- Can provide various clocks (RF of many rings and linacs) with a single, standard link.

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For more information see

<http://www.ohwr.org/projects/white-rabbit/wiki>