

The EPICS-Based Control and Interlock System of the Belle II PXD

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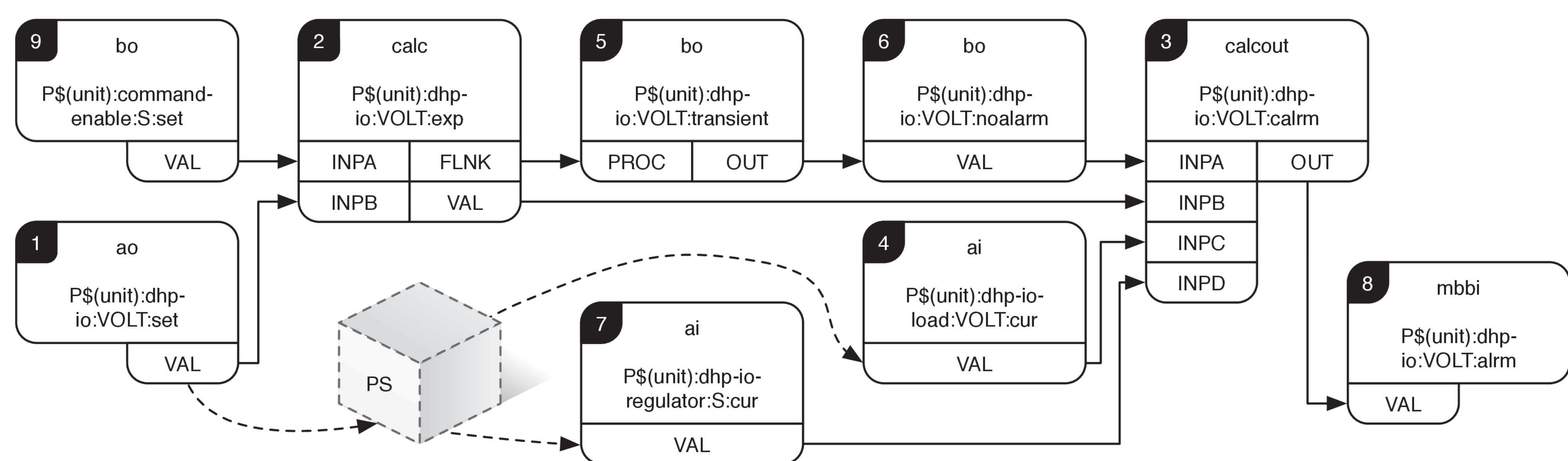
Introduction

The Belle II e^+e^- collider experiment at KEK will include a new pixelated detector (PXD) based on DEPFET technology as the innermost layer. This detector requires a complex control and readout infrastructure consisting of several ASICs and FPGA boards. We present the architecture and EPICS-based implementation of the control, alarm, and interlock systems and their interconnectivity to other legacy and heterogeneous subsystems. The interface to the NSM2-based Belle II run-control to orchestrate the PXD startup sequence is also presented. An installation of CSS is used to implement the user interface. The alarm system uses CSS/BEAST, and is designed to robustly minimize spurious alarms. The interlock system consists of two main parts: a hardware-based system that triggers on adverse environmental (temperature, humidity, radiation) conditions, and a software-based system. Strict monitoring including the use of heartbeats ensures permanent protection and fast reaction times. Especially the power supply system is permanently monitored for malfunctions, and all user inputs are verified before they are sent to the hardware. The control system is embedded into a larger slow-control landscape that also incorporates archiving, logging, and reporting in a uniform workflow for the ease of daily operation.

Robust Power Supply Alarm Generation

Problem: Many reasons for wrong voltage output. Create a meaningful alarm message:

Enabled (9)	Set Voltage (1)	Actual Voltage (4)	Mode (7)	State (8)
no	1.8 V	0.0 V	CV	OK
no	1.8 V	1.8 V	CV	Over-Voltage
yes	1.8 V	1.5 V	CV	Under-Current
yes	1.8 V	1.5 V	CC	Over-Current
yes	1.0 V → 1.8 V	1.5 V	CV	OK
yes	1.8 V	2.0 V	CC	Over-Voltage
yes	1.8 V	1.8 V	CV	OK



EPICS database structure to calculate alarms for a power supply channel.
"Expected" voltage (2) is 0.0 V, when the channel is off.
noalarm (6) is high for one second after the expected voltage changes.

- The implemented logic first calculates the voltage expected at the load.
- When it changes, it defines a one-second period during which mismatches are ignored to give the power supply time to react.
- The actual alarm state then also considers the current mode of the channel to differentiate between over-current and under-voltage conditions.

The PXD Control System



- Based on EPICS and CSS.
- BEAST alarm system.
- Scientific Linux 7 from RPM installation.
- Various devices and interfaces to handle:
 - FPGAs via IPbus.
 - ASICs via JTAG.
 - PLCs via Modbus.
 - FPGAs via a memory-mapped interface (with the IOC running on the on-chip PowerPC).
 - Power Supplies via CHROMOSOME, a fault-tolerant middleware with heartbeats.
 - ATCA crates and computing servers via IPMI.
 - Bragg fibre interrogators for environment monitoring via a proprietary protocol via Ethernet.
 - Belle II runcontrol via Network Shared Memory 2 (NSM2).
- Complex statemachine to bring up the system in a safe way.
 - First digital power to the ASICs, then configuration of the ASICs, finally analog power.
 - About 100 steps implemented via the EPICS sequencer module.
- Configuration Database to store the information required to start a run.
- Hardware and Software Interlocks for the Power Supply system.
 - Validation of all user input to prevent dangerous settings from reaching the power supplies.

DEPFET Current Status:

- All devices under control via EPICS.
- System integration is ongoing.

Deployment Plans:

- Next milestone is a testbeam in early 2016.
- One SC installation for a partial PXD system on the beam line during the commissioning phase of the accelerator.
- One SC installation for the PXD detector in the assembly room.

Logging Integration

Problem: Log messages from IOCs should not be overlooked.

- C++ library for IOCs and other services.
- Automatic backtrace generation when the application crashes.
- Messages passed on via the STOMP protocol to ActiveMQ.
- JMS2RDB stores the messages in an RDB.
- CSS to display the messages from all sources in one view.

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