



# XFEL-MPS

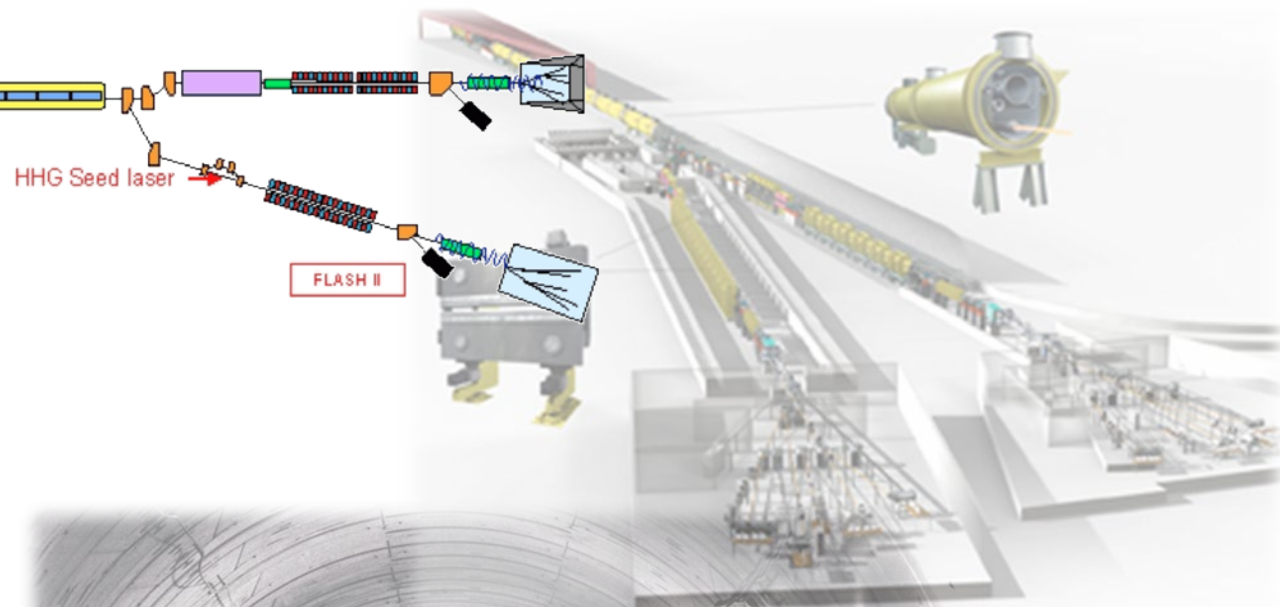
**XFEL Machine Protection System  
(MPS) based on uTCA**

**Sven Karstensen, DESY**

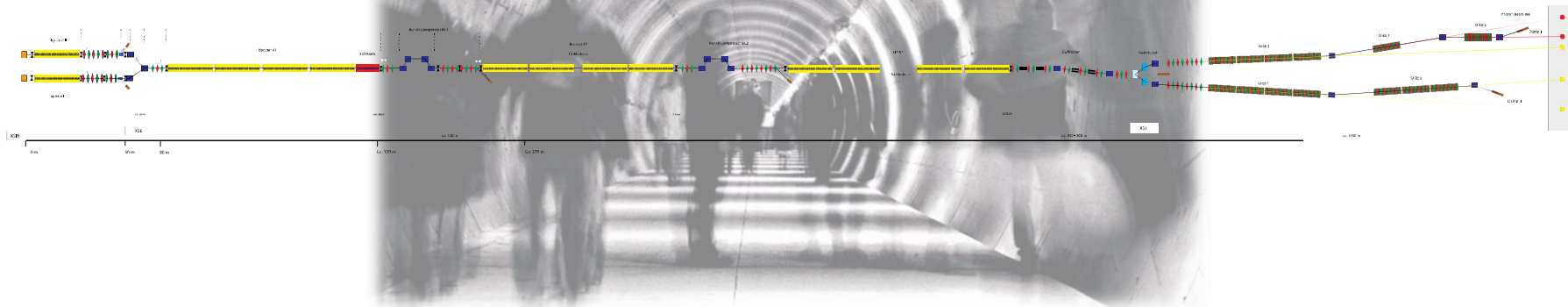


# FLASH 2 and XFEL

2

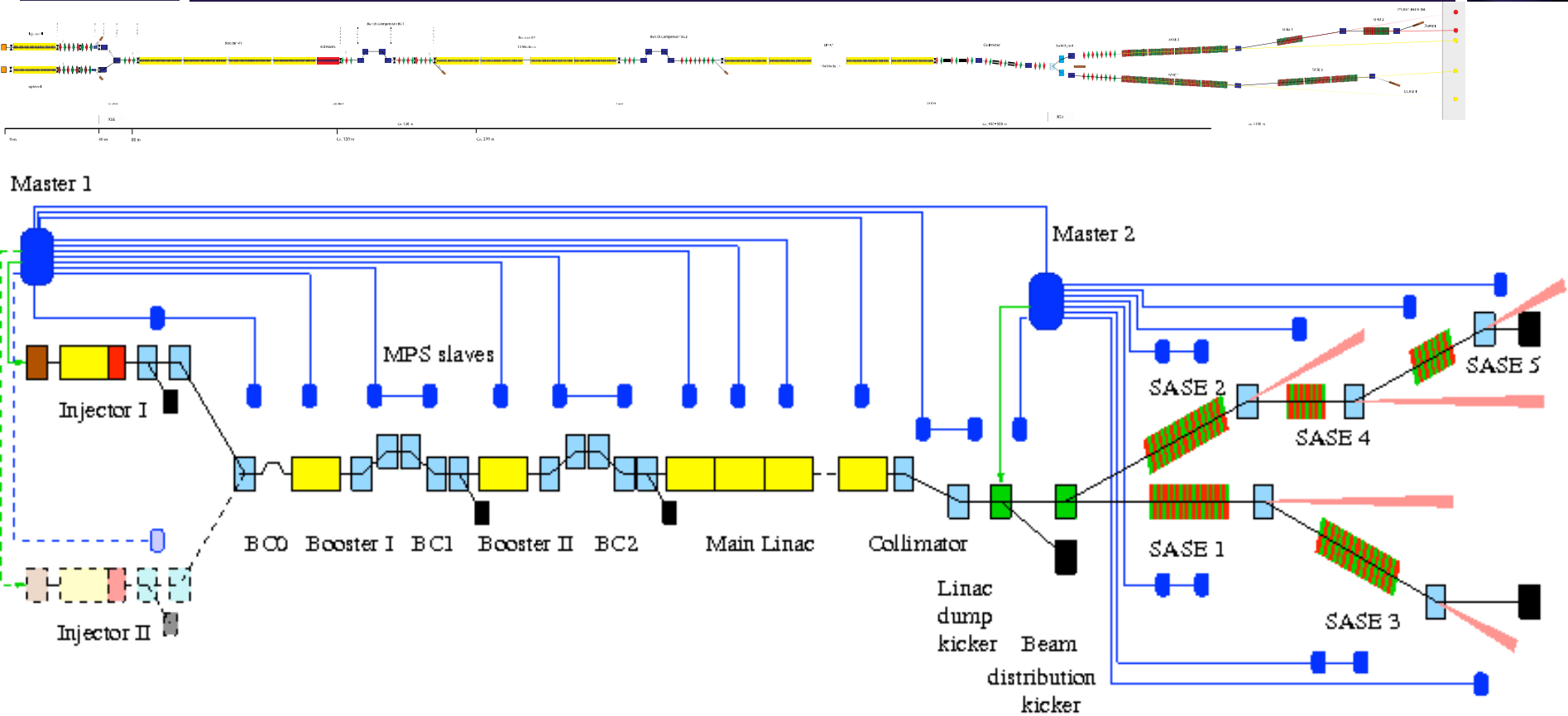


Overall length  
FLASH: 500m  
XFEL: 5.4 km



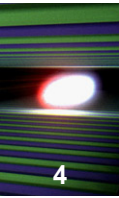
# MPS architecture in XFEL

3



2 Masters, >120 Slaves

# The Problems

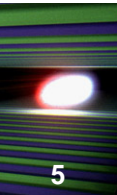
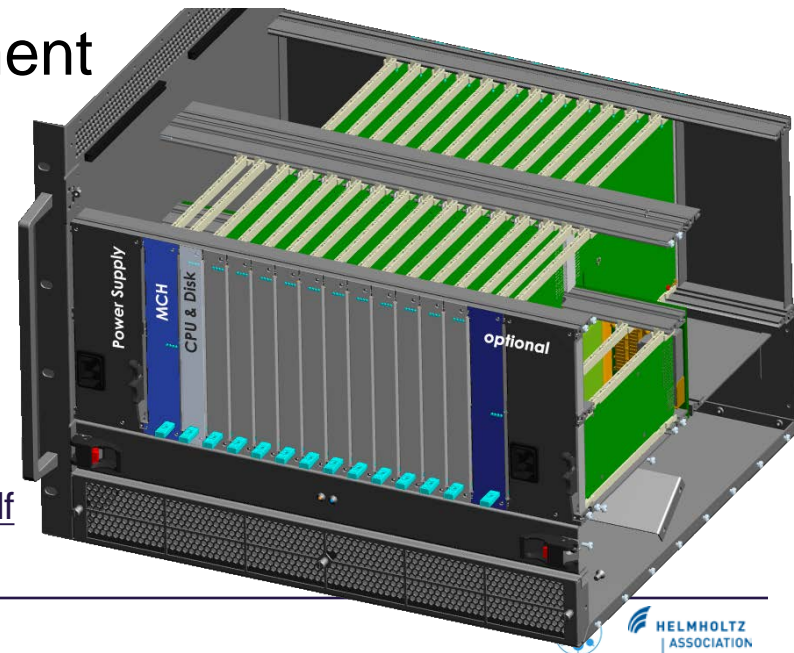
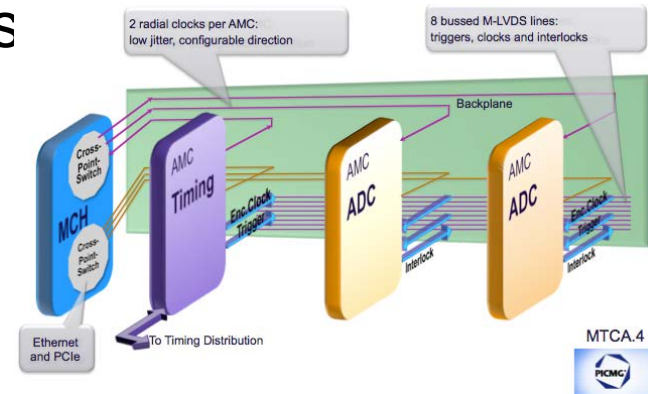


- Latency of signals
- Reliability of components
- Maintenance without shutdown the accelerator

# MTCA.4 in general

- IPMI Management for 12 AMC modules
- Management for up to 4 Power Modules
- Fabric Switching for up to 60 Ports
  - 12 GbE minimum
  - 12 x 4 lanes XAUI, PCI-E or SRIO
- Management for up to 2 Cooling Units
- Optionally provides Shelf Management
- Front Panel Alarms
- Clock Distribution system
- Fabric Channel Uplink
- HOT SWAPable

Source: [http://www.picmg.org/pdf/introduction\\_to\\_microtca.pdf](http://www.picmg.org/pdf/introduction_to_microtca.pdf)  
and Kay Rehlich, DESY





## ■ Modular + modern architecture

- Reusability + PCIe + Ethernet

## ■ High availability (.999 to .99999),

- Redundant power and fan optional
- IPMI management

$$A = \frac{E[\text{Uptime}]}{E[\text{Uptime}] + E[\text{Downtime}]}$$

## ■ High performance:

- Very low analog distortions
- 4 lanes PCIe: 400 MB/s ... 3.2 GB/s

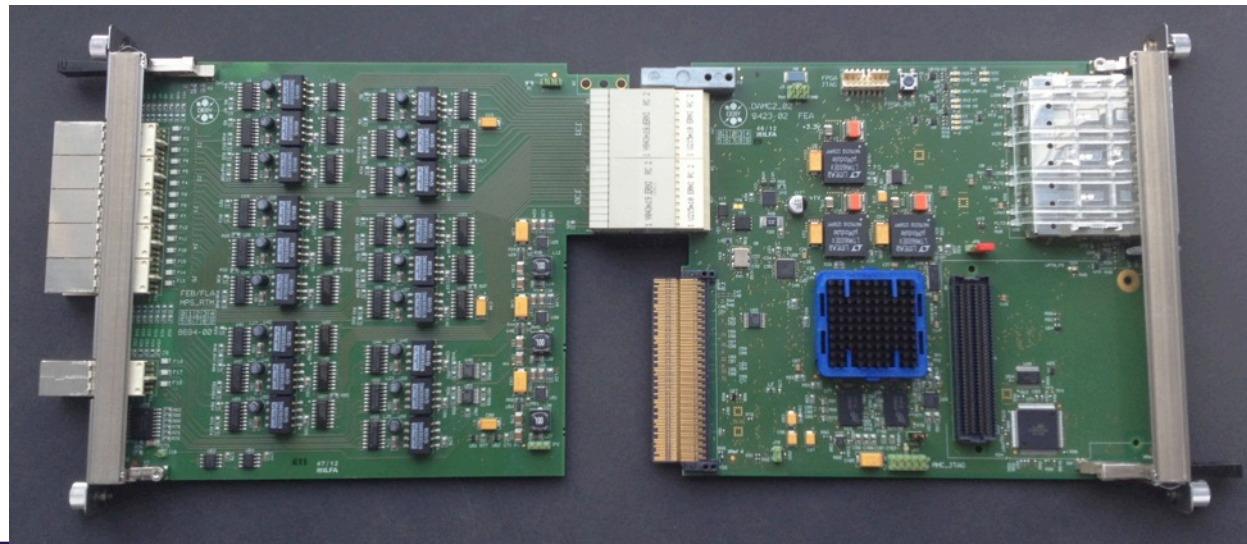
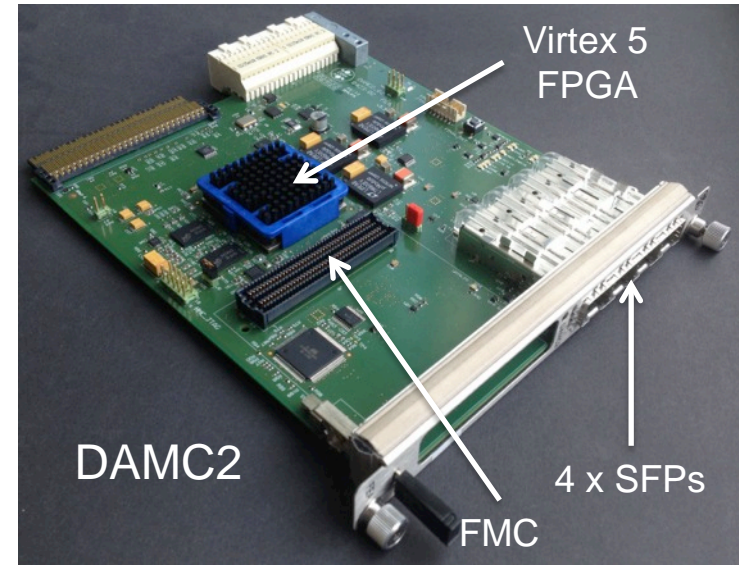
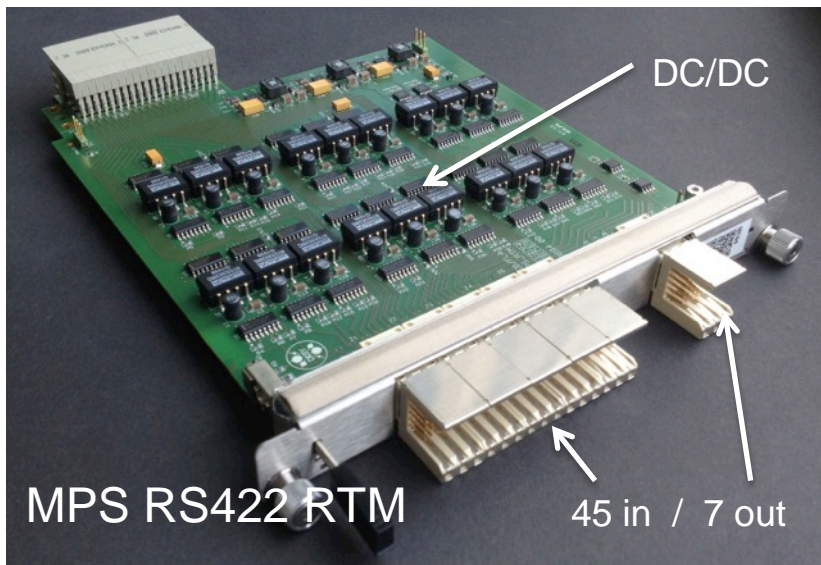
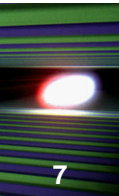
## ■ XFEL fast electronics will be based on **MTCA.4**: > 200 Crates



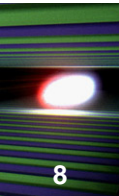
Courtesy to Kay Rehlich, DESY



# MPS MTCA components, DESY design



# Overall MPS features



- Scalability
- same firmware in every DAMC2
- Every DAMC2 slave holds all information of all prior connected slaves (debugging)
- Every slave can be connected to the timing system
- Every slave can be hold one I2C driven FMC Dosimetry board
- Configurable – NOT programmable



# Configuration Panel

mps\_flash2\_main\_static\_config.xml

Static Config - FLASH2 - uTCA MPS

Master Slave 1 Slave 2 Slave 3 Slave 4

Input names:	Inputs enabled:	Input simulations:	Inter-macro pulse checks:	Check count time resets:	Input flicker counter thresholds:	Flicker counter window size:	Fast lane out/ config:	Alarm transfer config:	Beam Modes bit config:	Section Pattern bit # config:
BLM018					0	0				0
BPM023					0	0				0
TPS012_0					32332	0				0
TPS012_1					32093	0				0
TPS012_2					32343	0				0
TPS012_3					32716	0				0
TPS012_4					32767	0				0
TPS012_5					32478	0				0
BLM019					0	0				0
CrvOK012					0	0				0
DOSI012_0					0	0				0
DOSI012_1					0	0				0
DOSI012_2					0	0				0

Identification

Board section | ID: 1 1

Server name: MPS\_SLAVE\_03

Device info: MPS\_TESTING

PCIe device driver: /dev/pciadevs1

Position X | Z: 1.1 111.1

Position name: Sven's crate slot 1

Magic # | ID: 50524fa 8

Version | Date: 1040015 20130822

States

Board reset!

:Reset pending

:Initial config uploaded

:Config changes uploaded

Status

Acknowledge

:PCIe communication

:Firmware conformity

:FPGA memory

Out/ names: OK013

Out/s enabled:

Out/s:

Digital outputs

Alarm transfer enabled:

Connectors enabled:

In/:

Out/:

SFPs

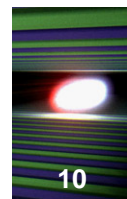
Back-plane

Beam Modes output

Section Pattern output

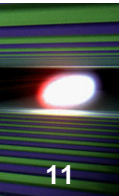
Offset: 0

# General MPS features for every DAMC2



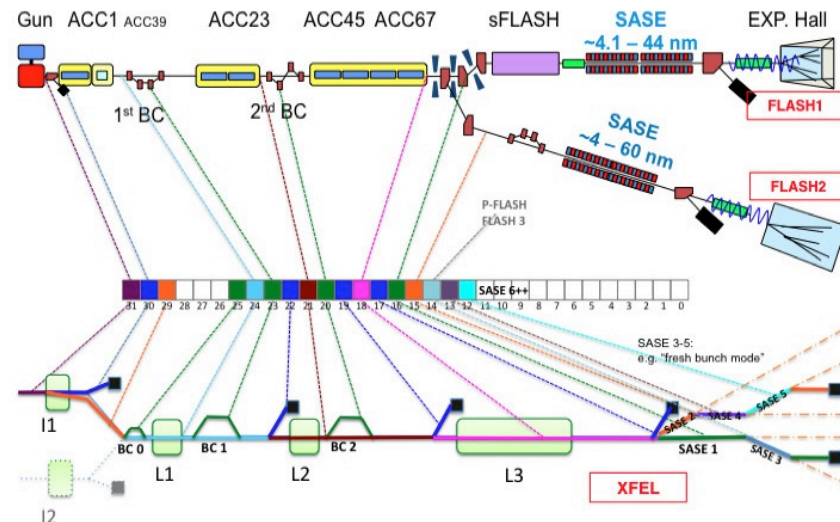
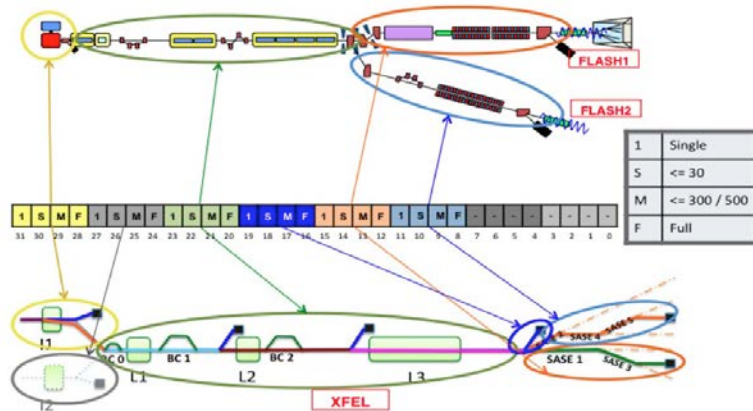
- 45 RS422 external input channels
- 3 internal input channels for FMC
- 7 RS422 output channels, 1 Backplane Output
- I<sup>2</sup>C support to FMC
- 4 SFP I/O fiber optic lines (0-4 Inputs, 0-4 outputs)
- Addressable up to 64 Sections, each equipped with 64 DAMC2 MPS modules
- Indirect redundancy
- Fast internal RS422 link from in- to outputs
- Debug Register
- LED status indicator (heart beat, server connection, initialization)

# IN- and OUTPUT channel features



- Options for each INput channel (48):
  - Enable / disable Inputs ; Test input; Check functionality of connected systems between Macro Pulses; Pulse counter within a given time, both configurable; Beam Mode generation; Section Pattern generation; Alarm Type generation; Save each Alarm into DOOCS history
  
- Options for each OUTput channel (8):
  - Enable / disable Outputs ; Test output; Fast output line; Save each action into DOOCS history; Fast Output configuration on same DAMC2 board

# The Protocol



## Beam Modes

63-52		51		50-48		47-40		39-32		31-0	
Sec 63-58	Addr 57-52	51	50-48	47-40		39-32		39-32		31-0	
FFF 12 (6+6)		P 1	CNT 3	spare 8 bit		ALARM Type 8 bit		ALARM Type 8 bit		BEAM Modes 32 bit	

## Section Pattern

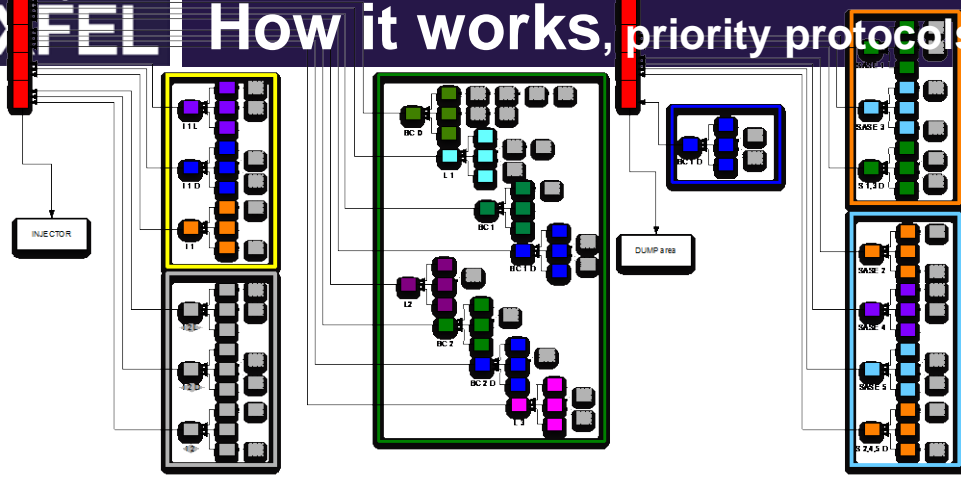
63-52						
63-58	57-52	51	50-48	47-40	39-32	31-0
FFE 12 (6+6)		P 1	CNT 3	spare 8 bit	spare 8 bit	SECTION PATTERN 32 bit

## Slave Info

63-52				
63-58	57-52	51	50-48	47-0
000 - FFD 12 (6+6)		P 1	CNT 3	single SLAVE information 48 bit

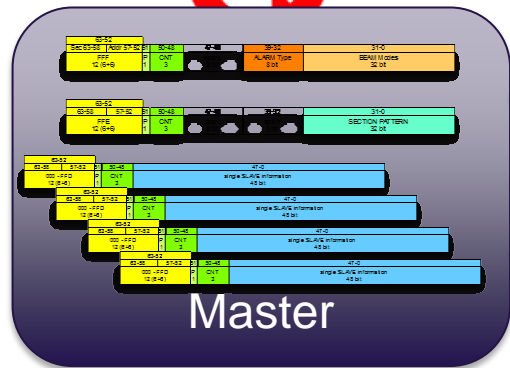


# How it works, priority protocols

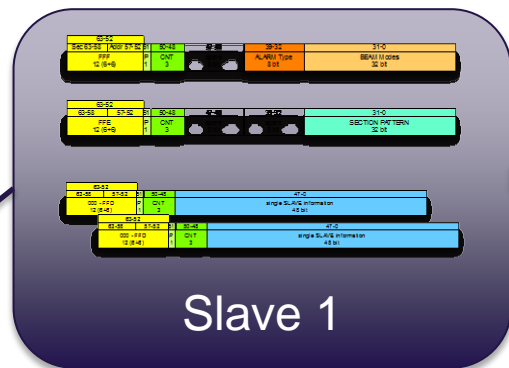


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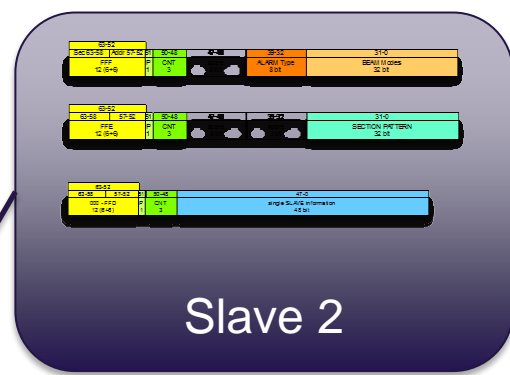
timing



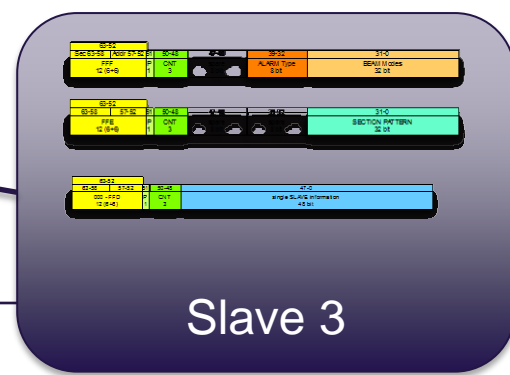
Master



Slave 1



Slave 2

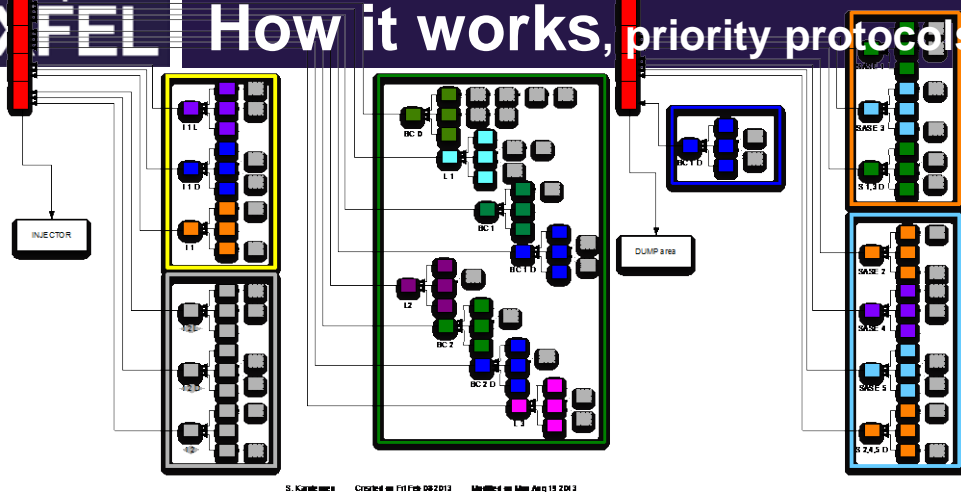


Slave 3

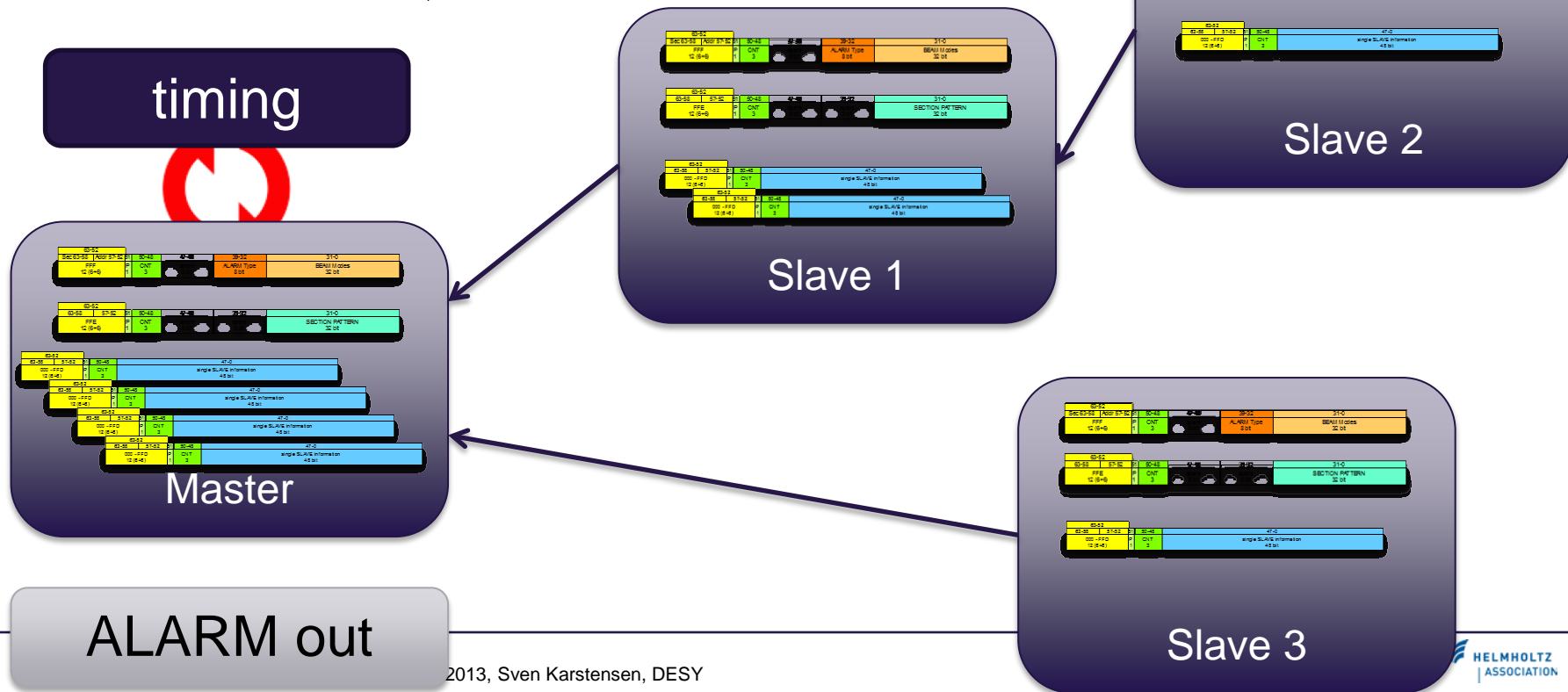
ALARM out

# How it works, priority protocols

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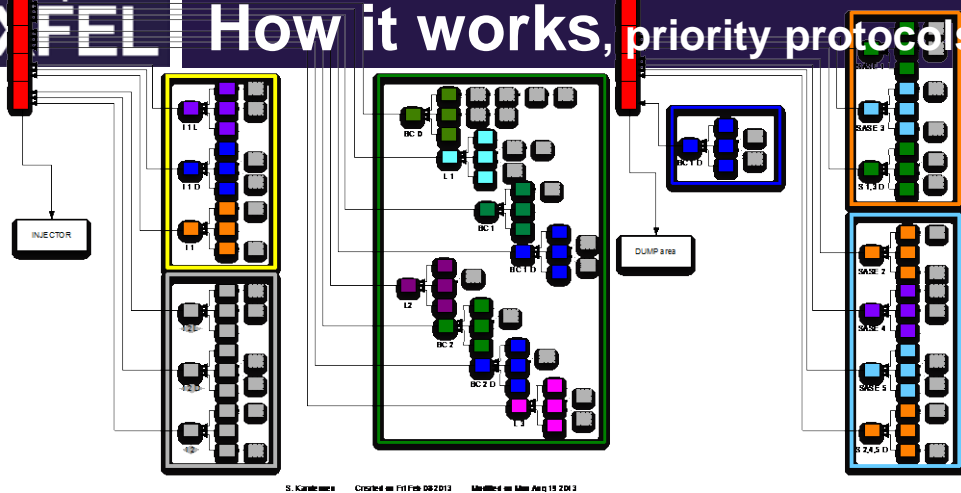


1.) Beam Modes **very high**



# How it works, priority protocols

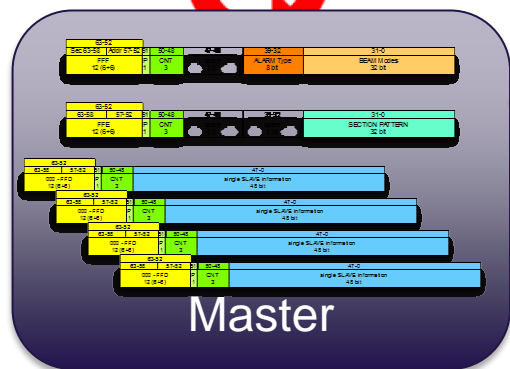
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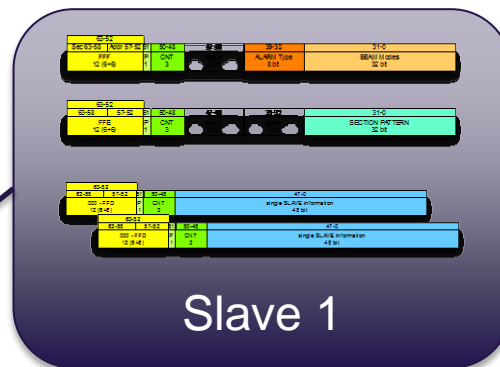
1.) Beam Modes **very high**

Alarm

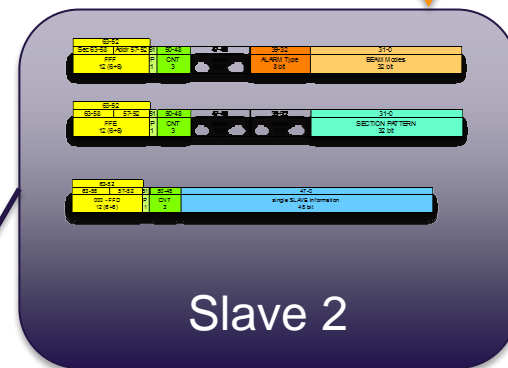
timing



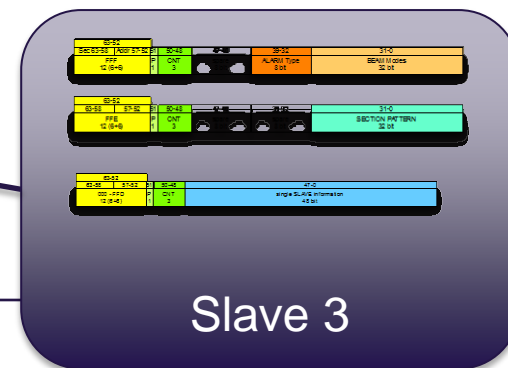
Master



Slave 1



Slave 2

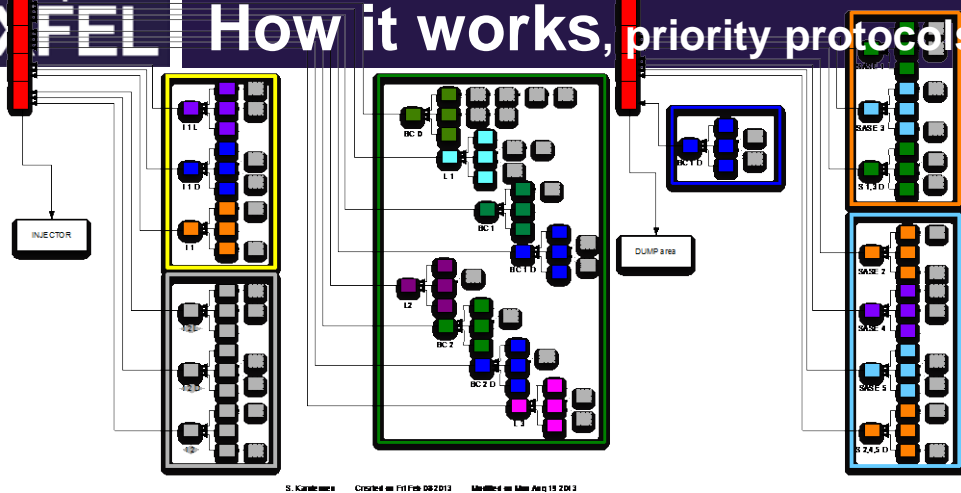


Slave 3

ALARM out

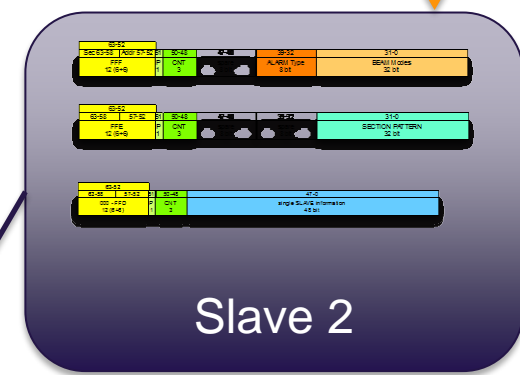
# How it works, priority protocols

17

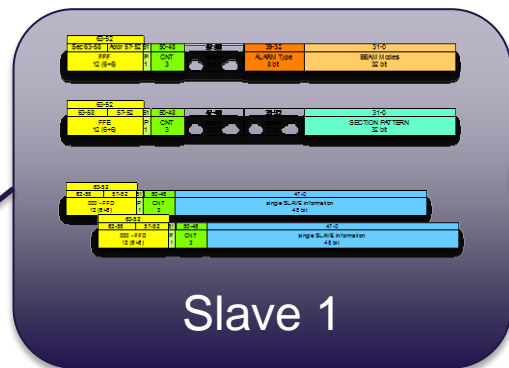


1.) Beam Modes **very high**

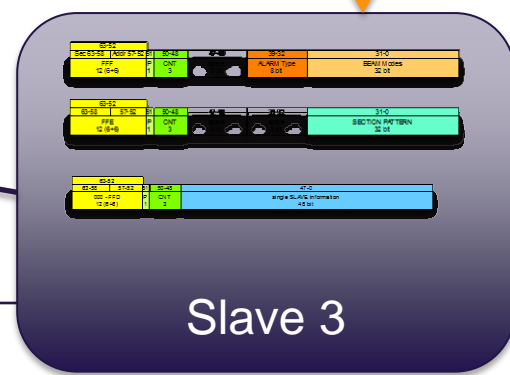
Alarm



Alarm

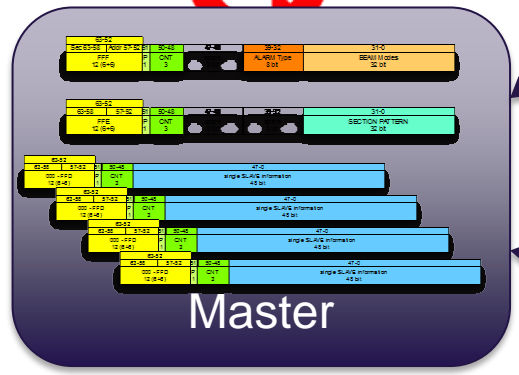


Slave 1



Slave 3

timing

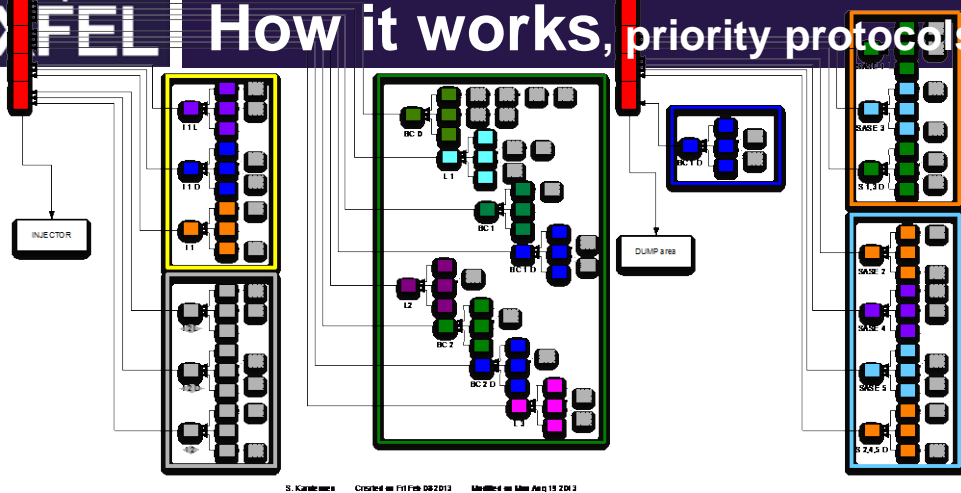


Master

ALARM out

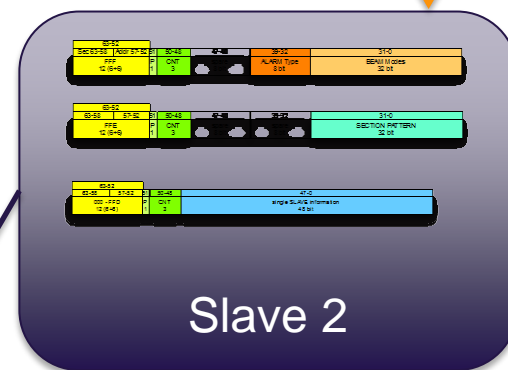
# How it works, priority protocols

18

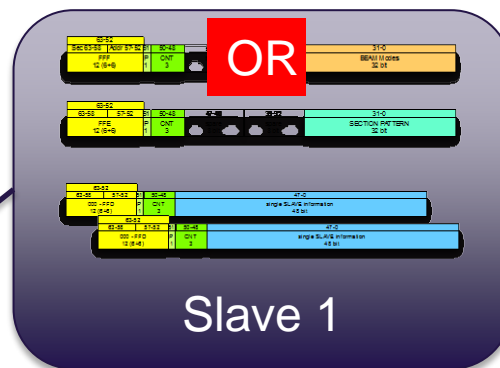


1.) Beam Modes **very high**

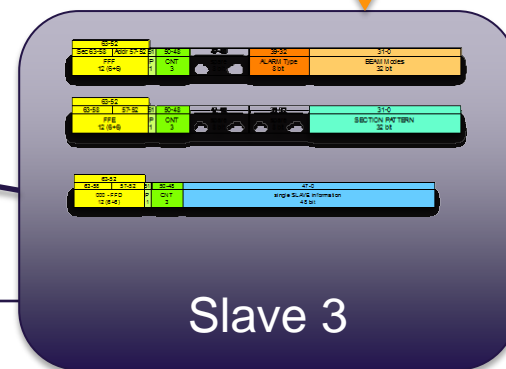
Alarm



Alarm

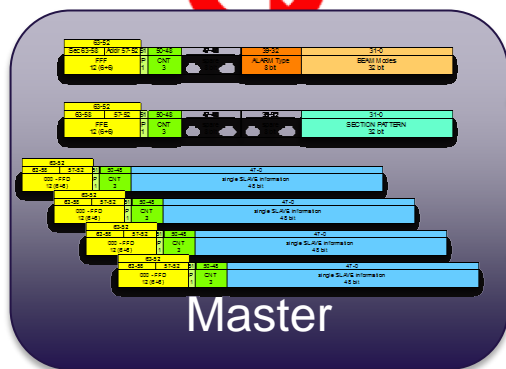


Slave 1



Slave 3

timing



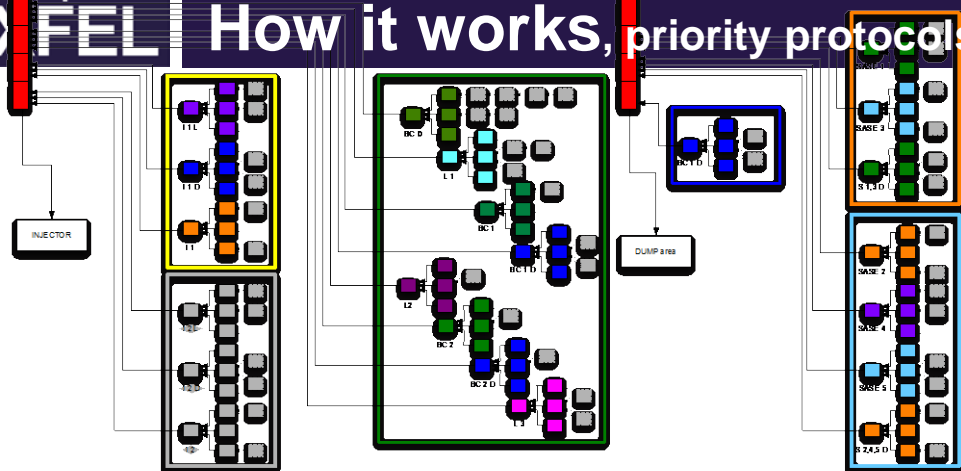
Master

ALARM out



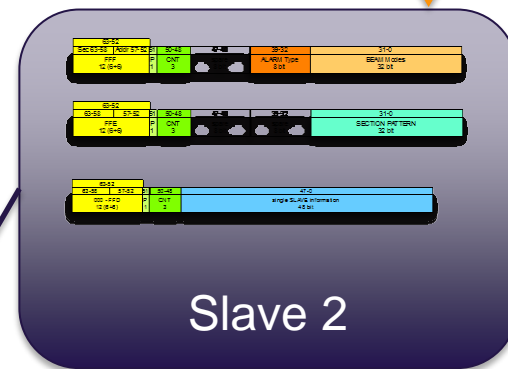
# How it works, priority protocols

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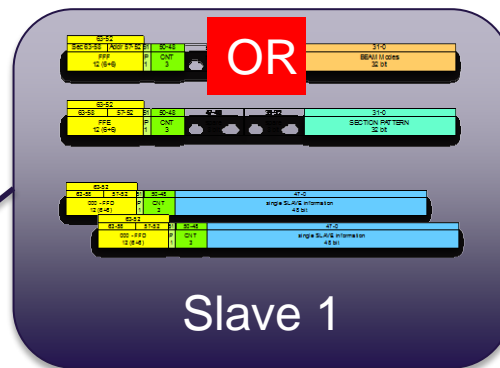


1.) Beam Modes **very high**

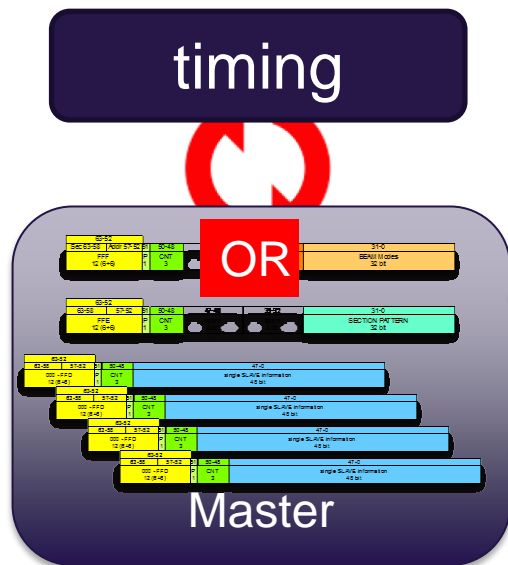
Alarm



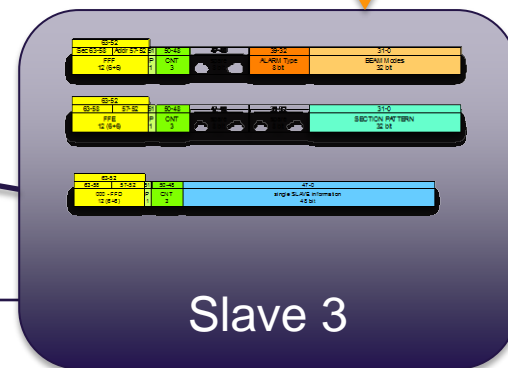
Alarm



Slave 1



Master



Slave 3

ALARM out

## 1.) Beam Modes **very high**



OR

## Slave 2

# Slave 1

# Alarm

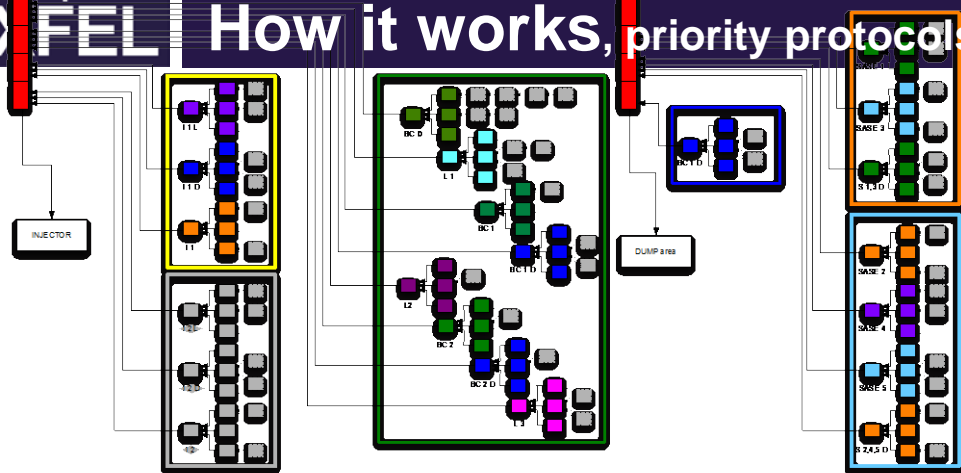
M...er

## Slave 3

# ALARM out

# How it works, priority protocols

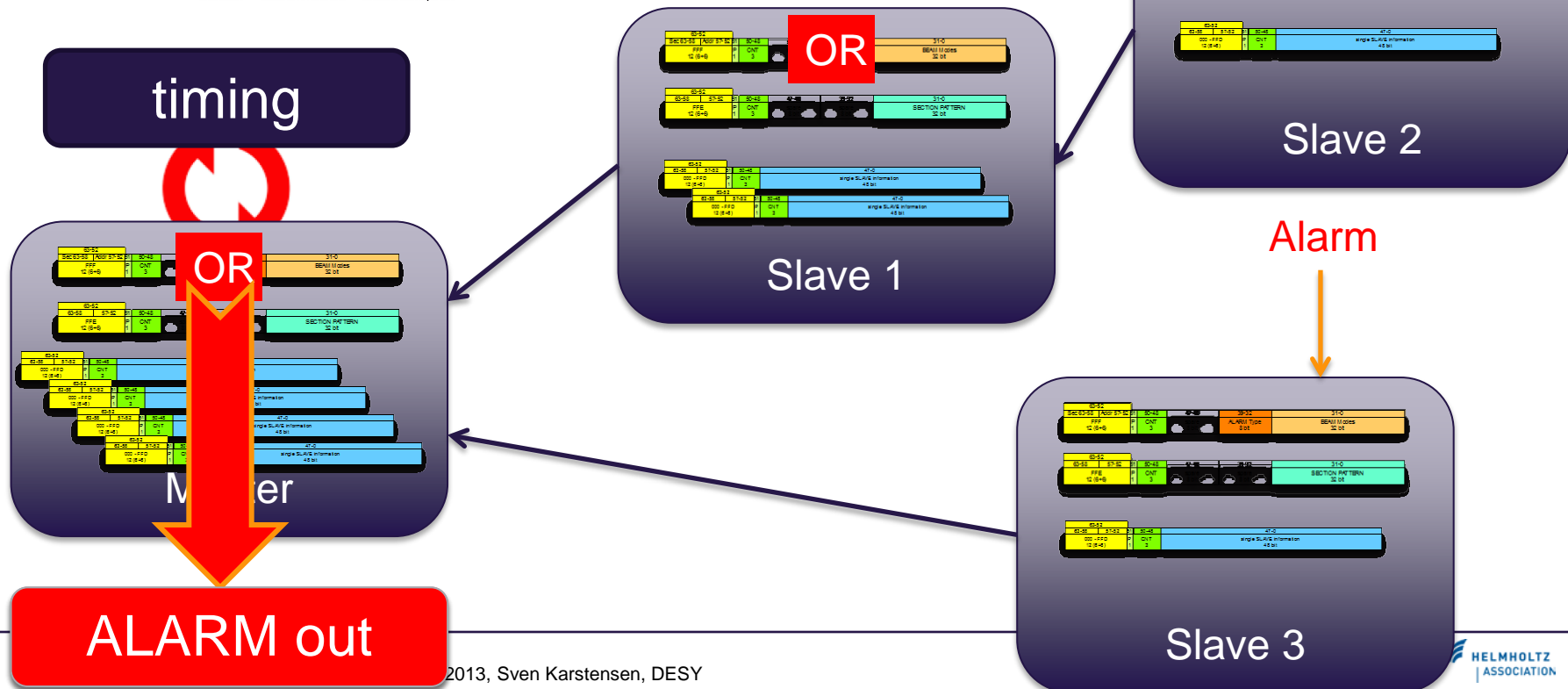
21



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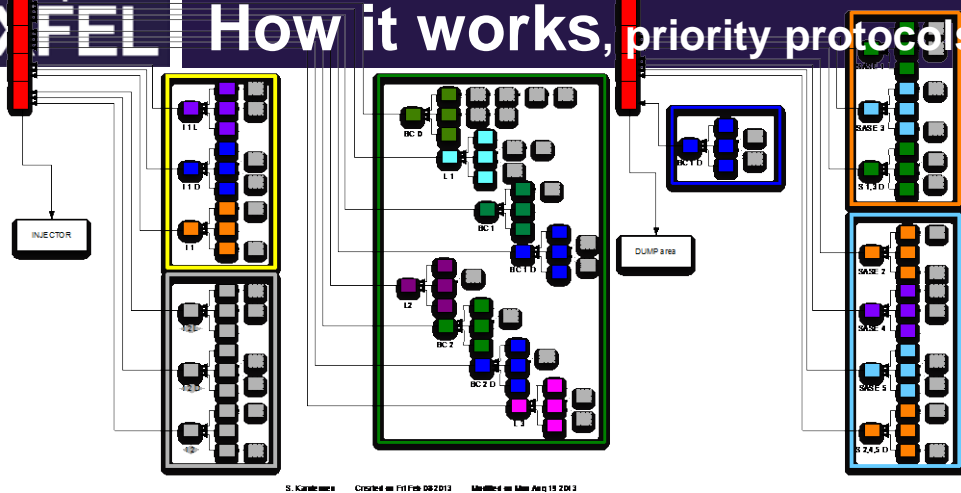
1.) Beam Modes **very high**

Alarm



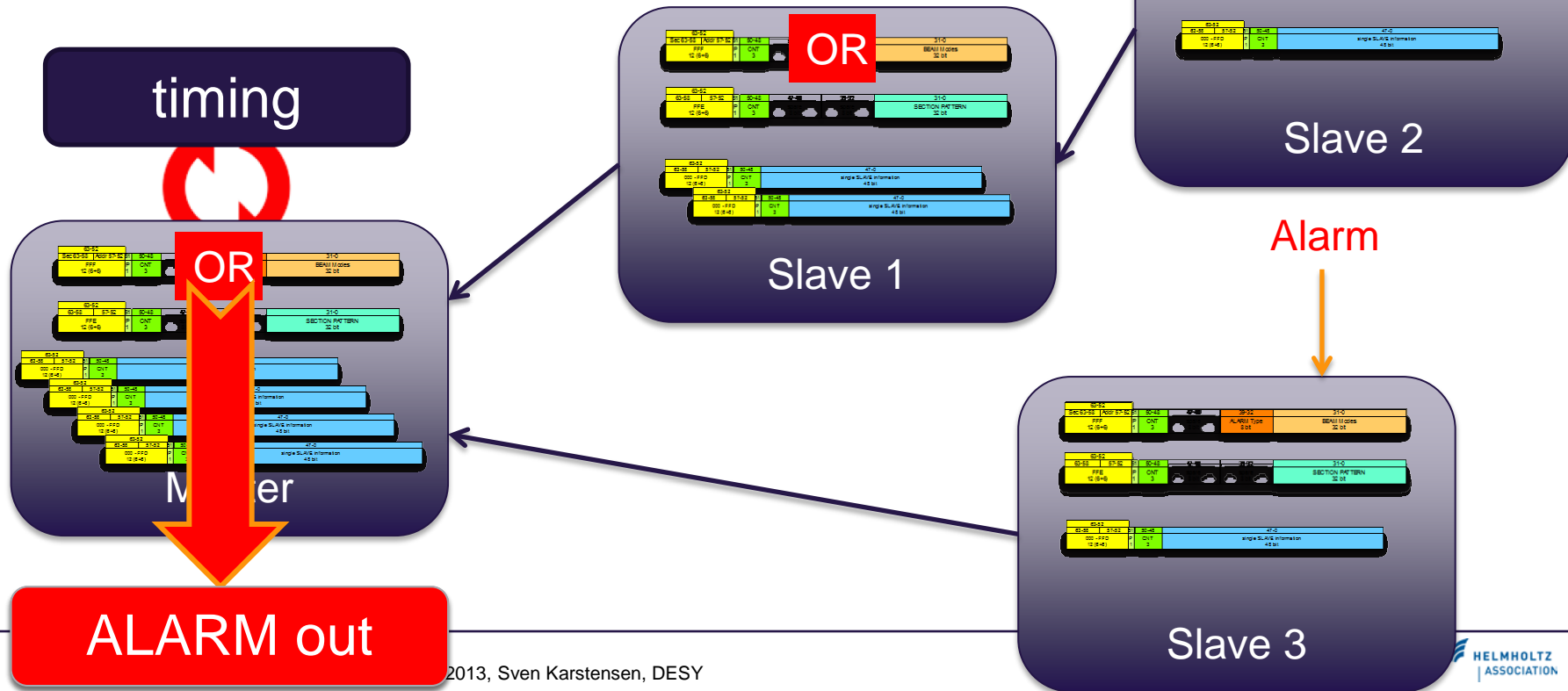
# How it works, priority protocols

22



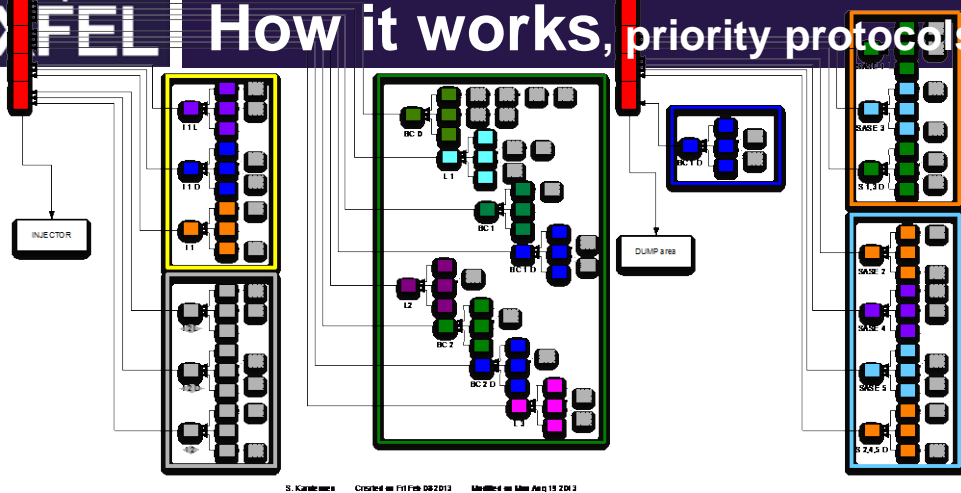
1.) Beam Modes **very high**

Alarm



# How it works, priority protocols

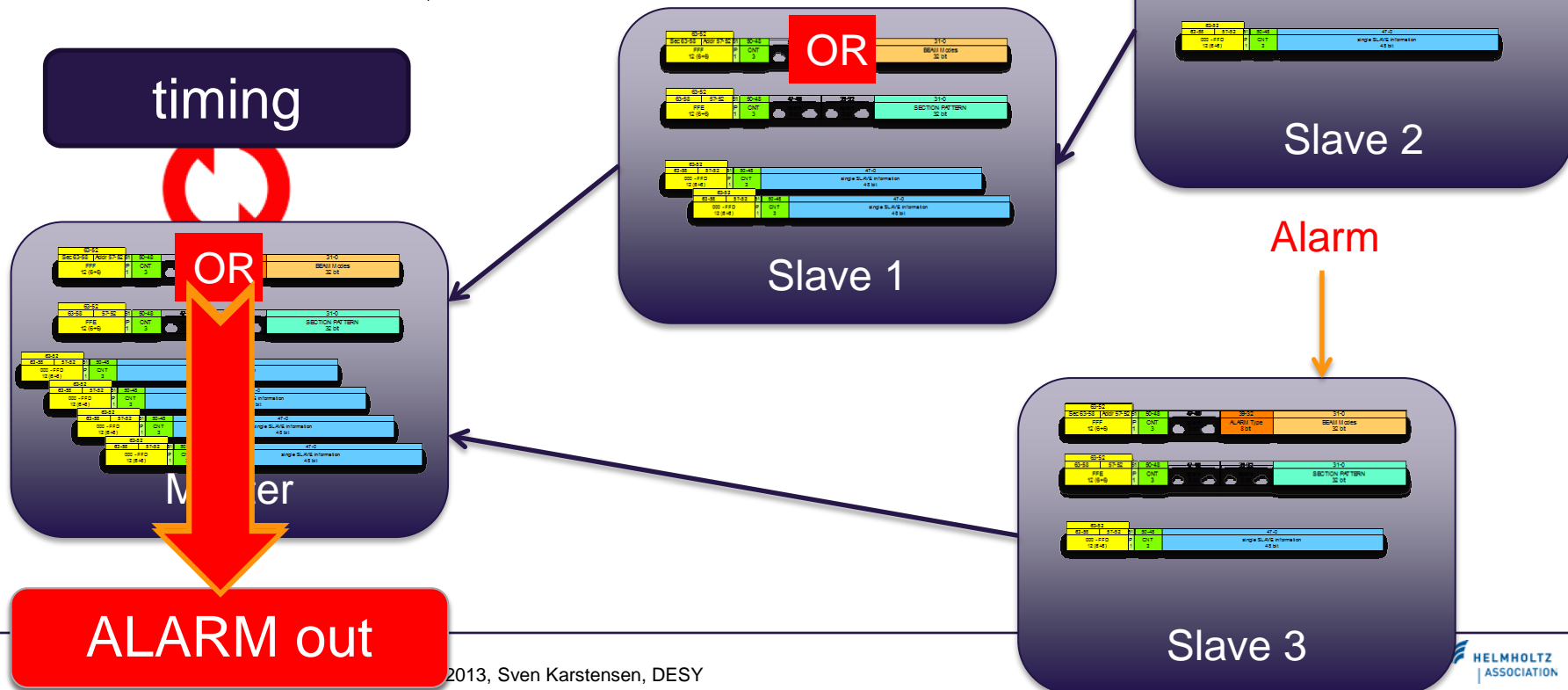
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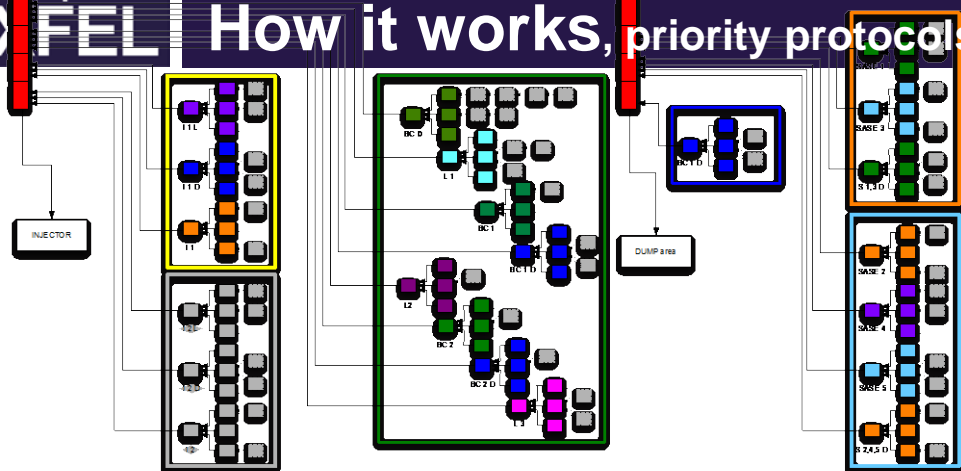
1.) Beam Modes **very high**

Alarm





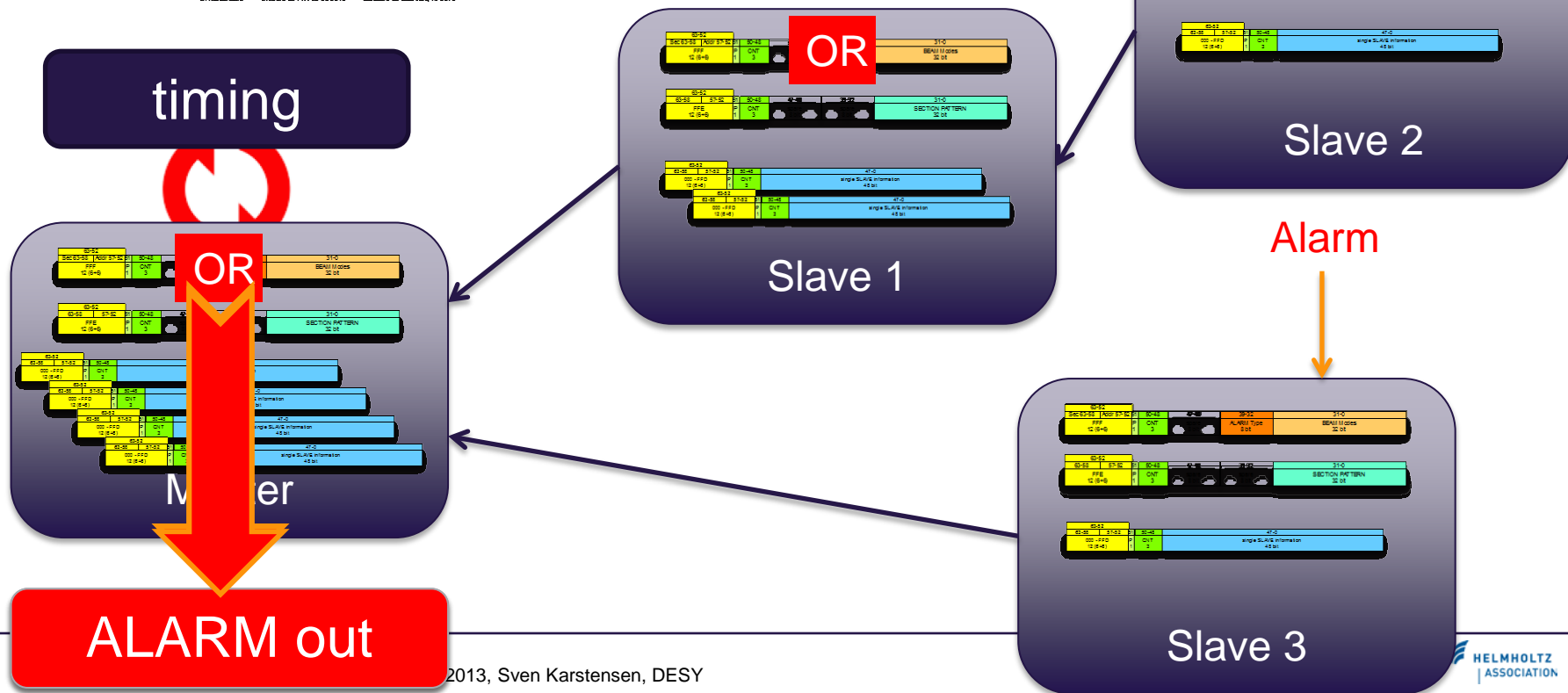
# How it works, priority protocols



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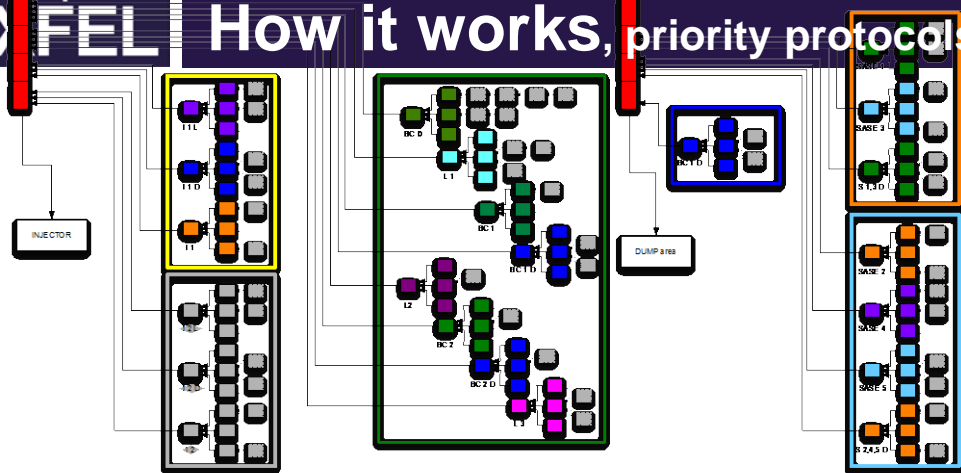
1.) Beam Modes **very high**

Alarm



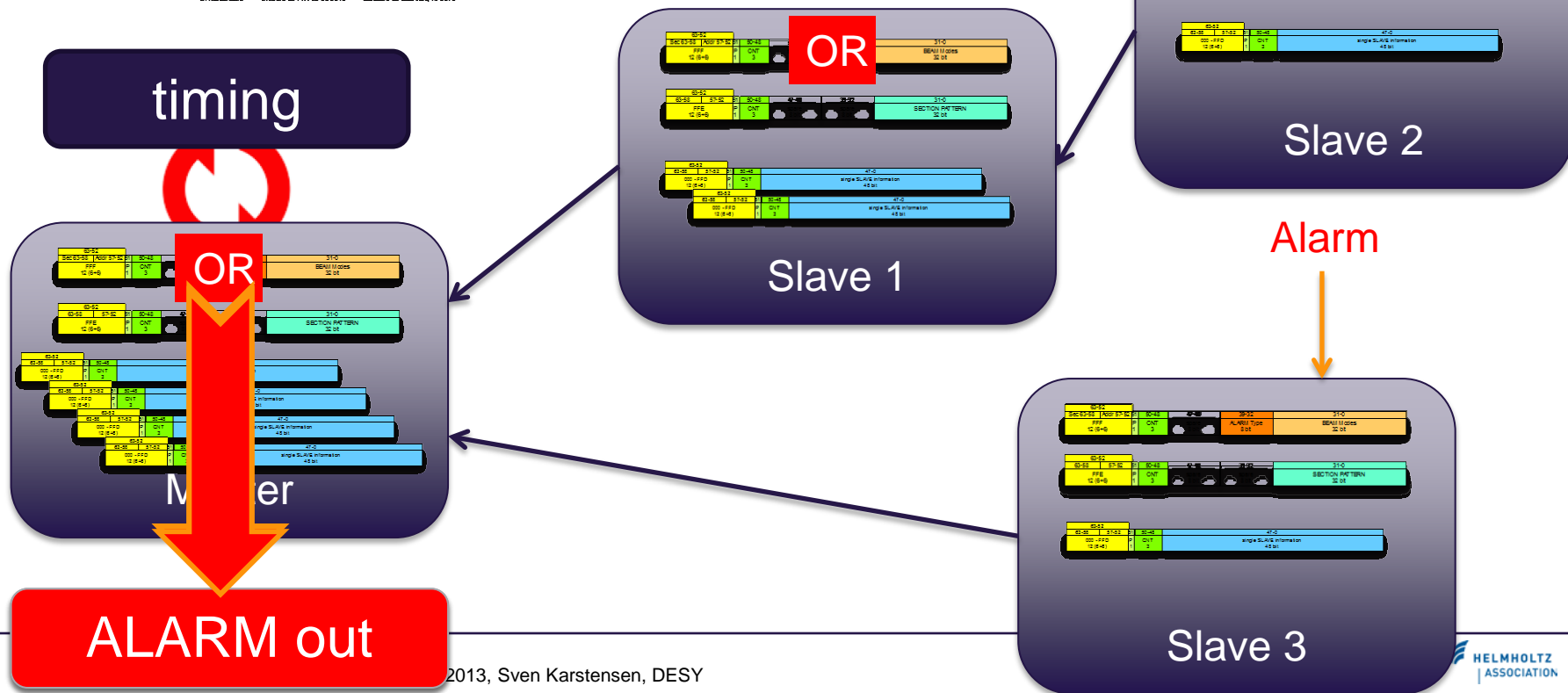
# How it works, priority protocols

25

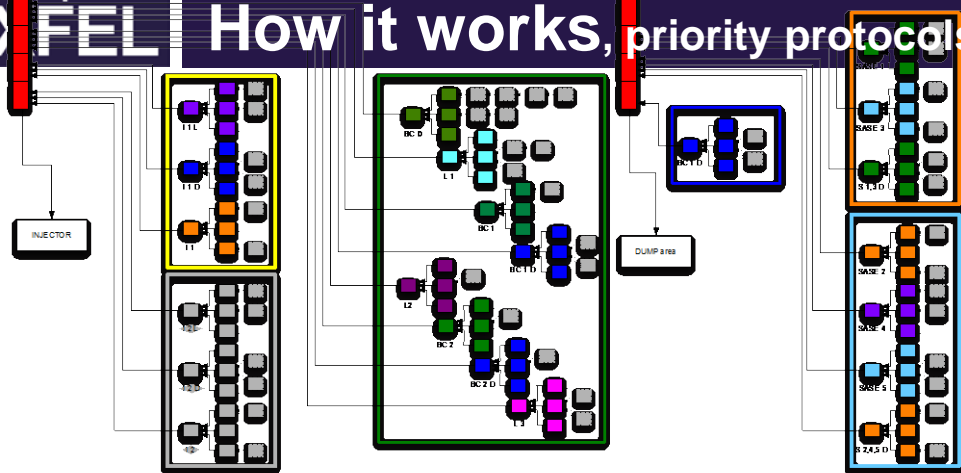


- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**

Alarm



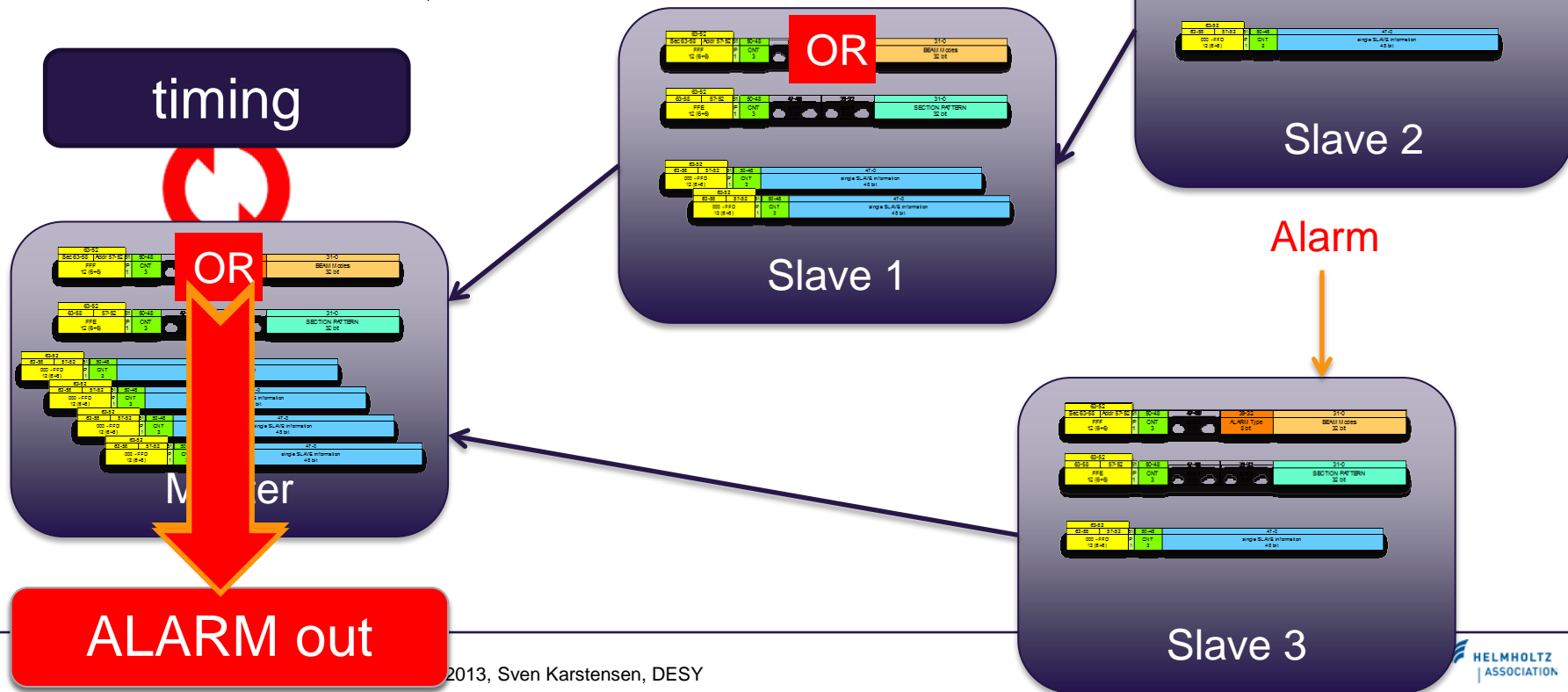
# How it works, priority protocols



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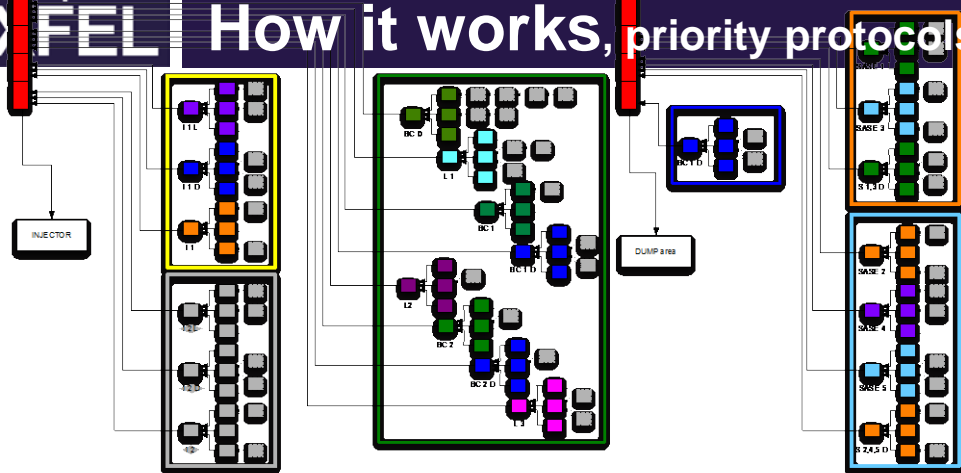
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**

Alarm



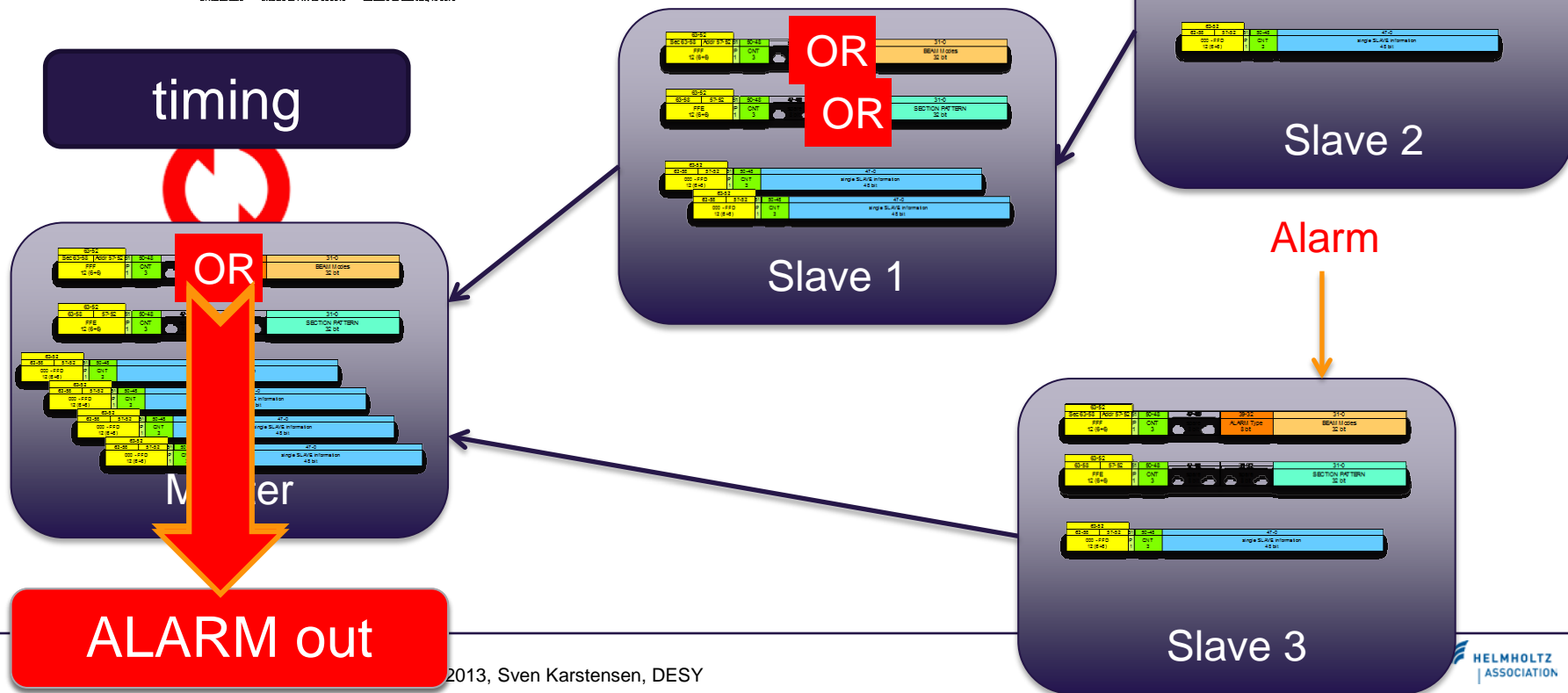
# How it works, priority protocols

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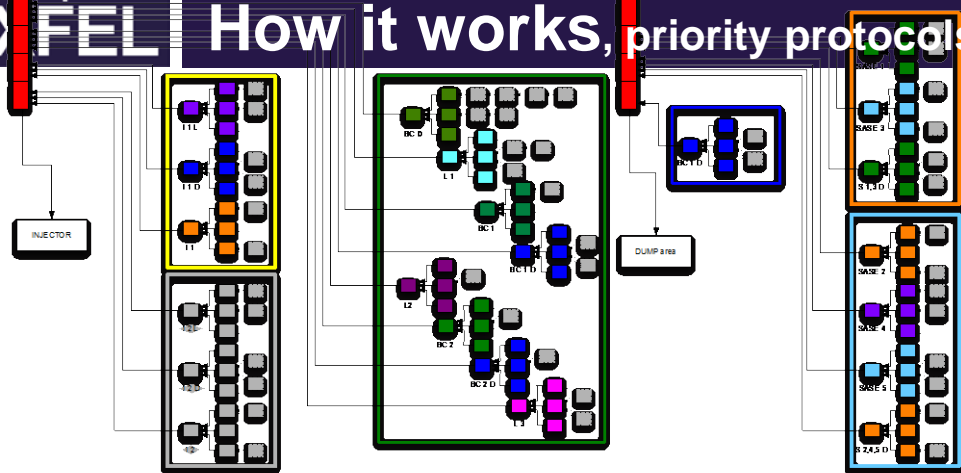
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**

Alarm



# How it works, priority protocols

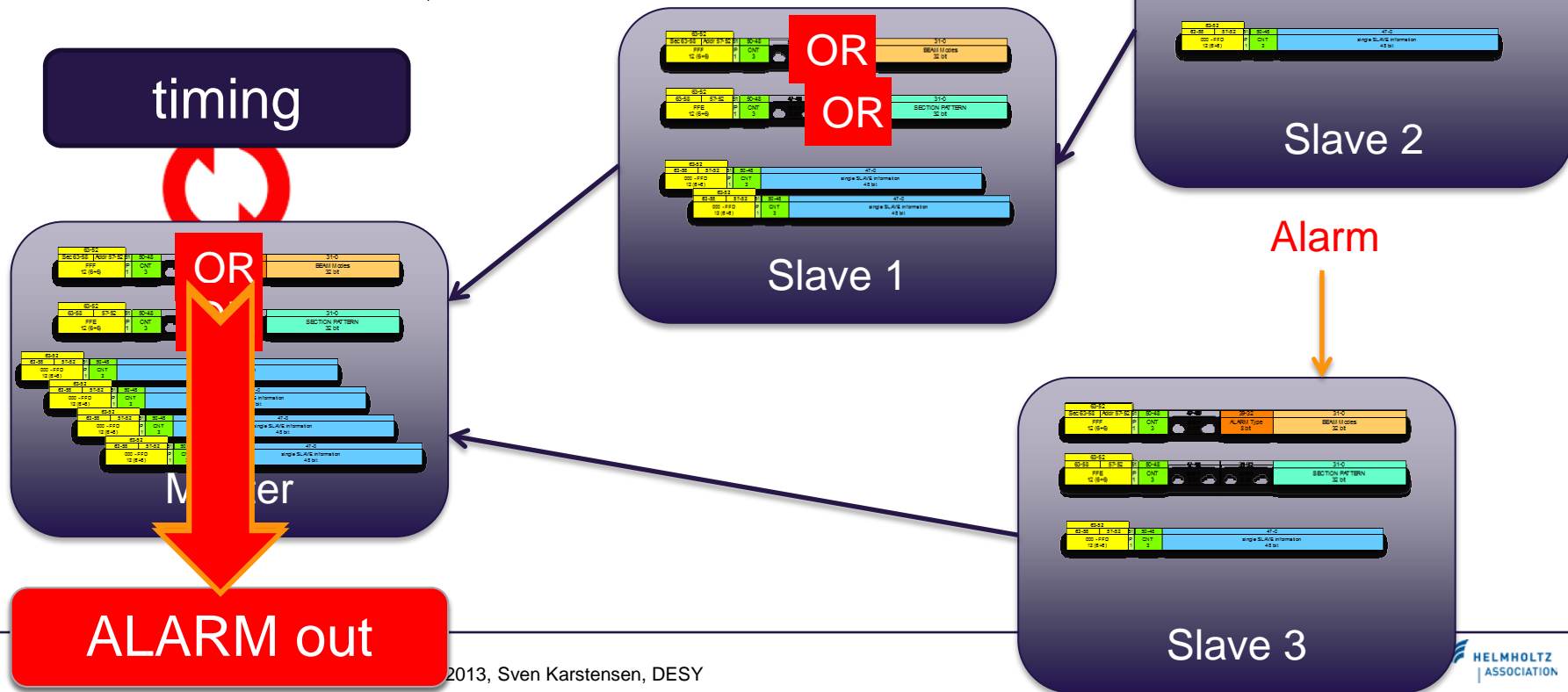
28



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- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**

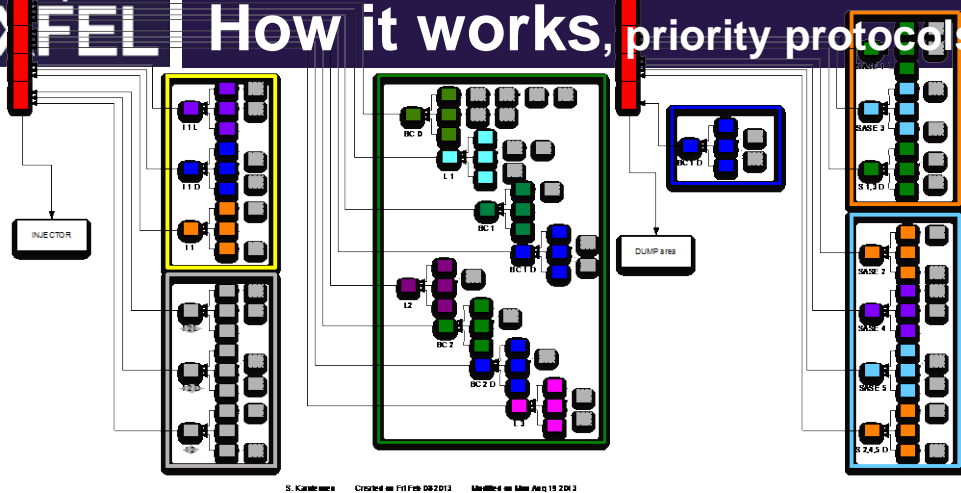
Alarm





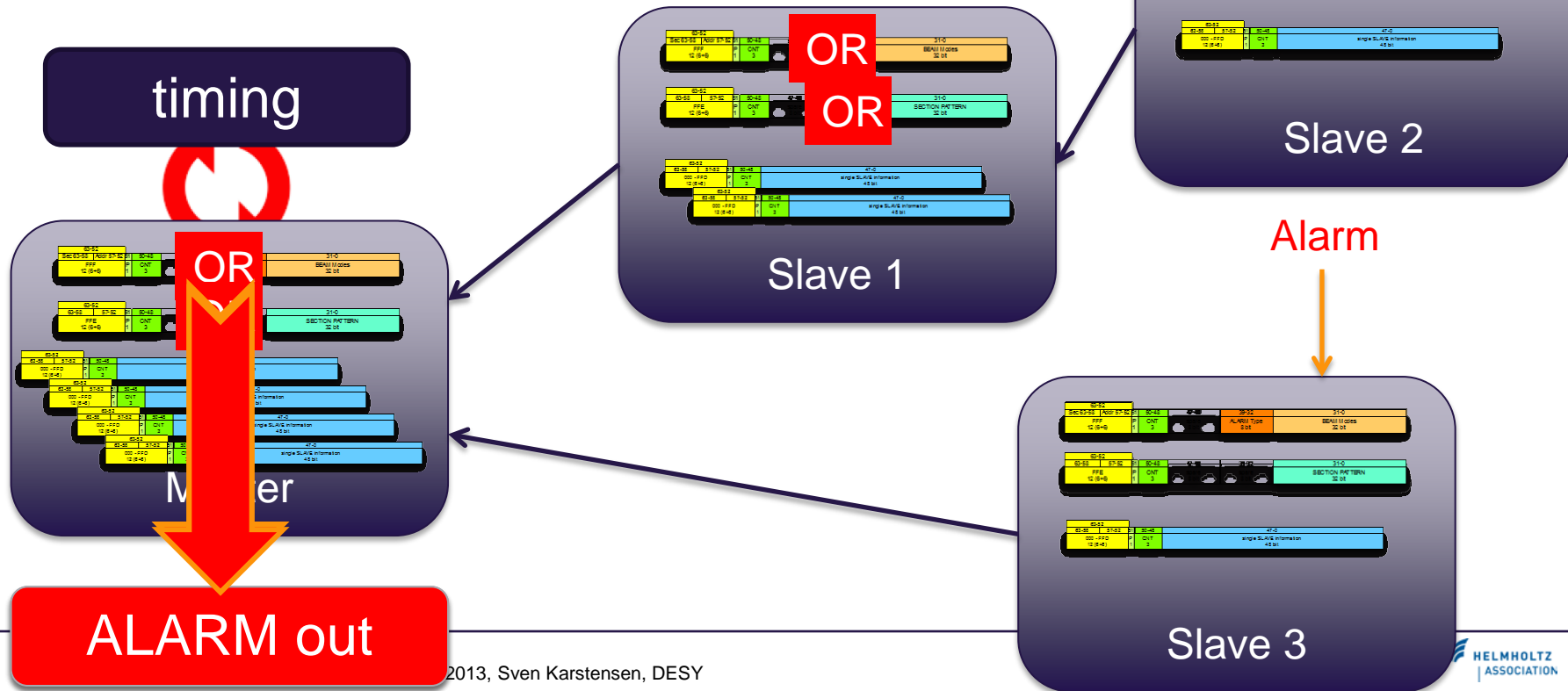
# How it works, priority protocols

29



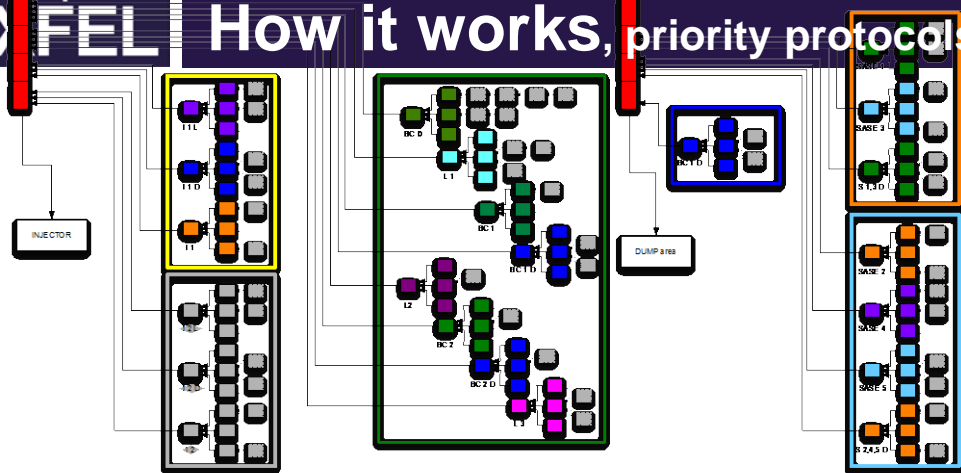
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**

Alarm



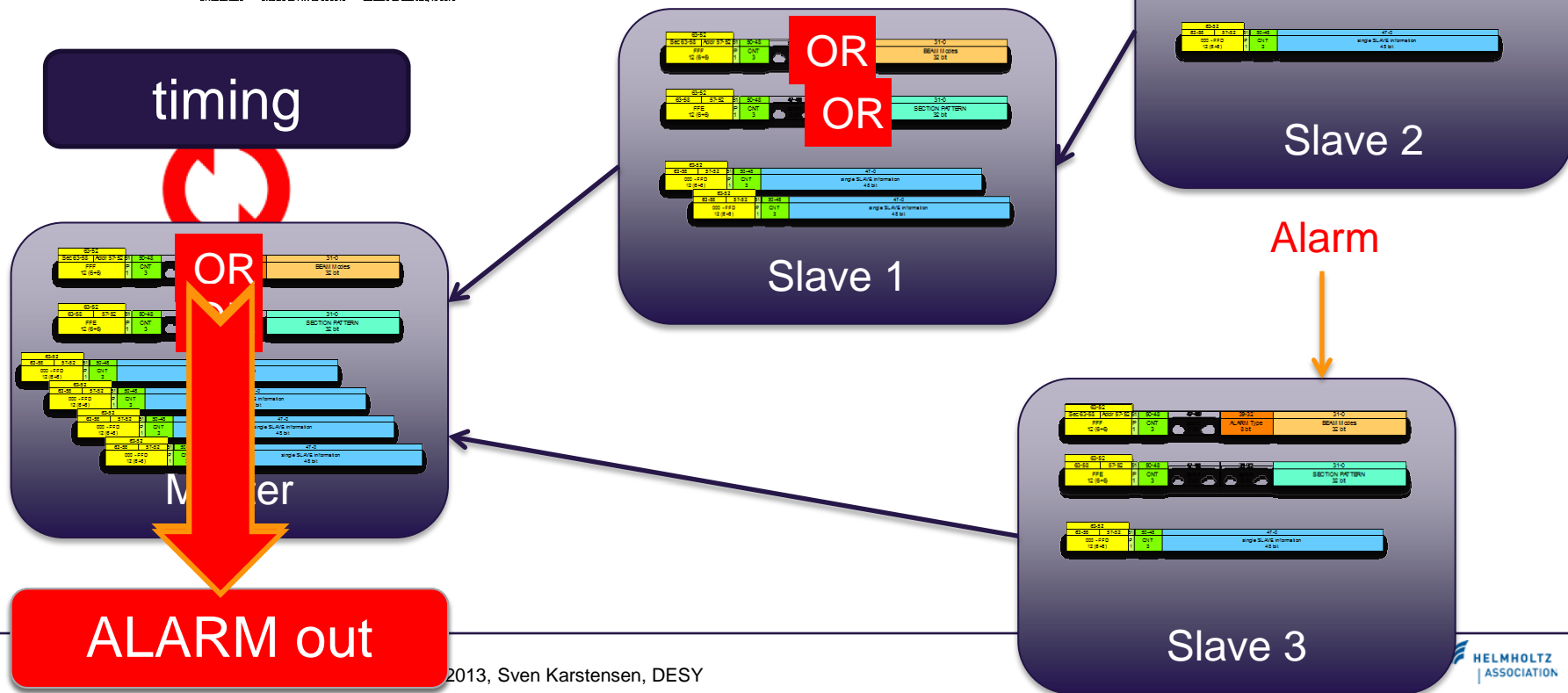
# How it works, priority protocols

30



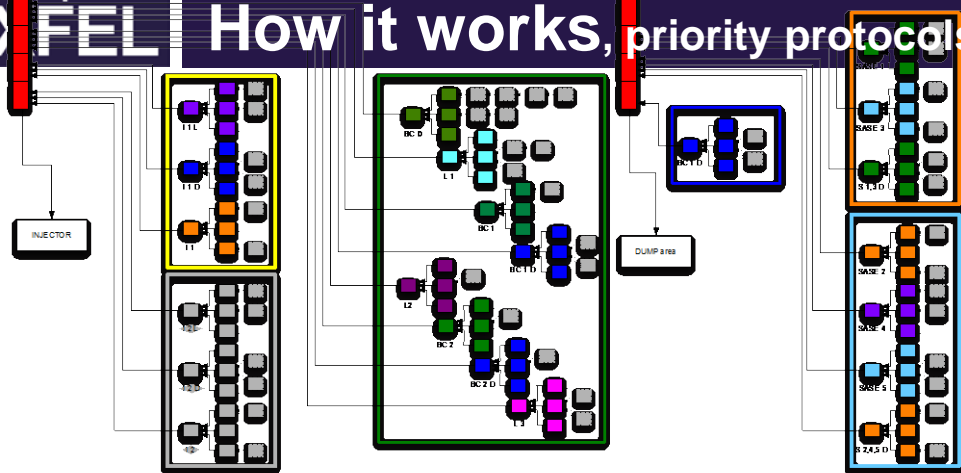
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**

Alarm



# How it works, priority protocols

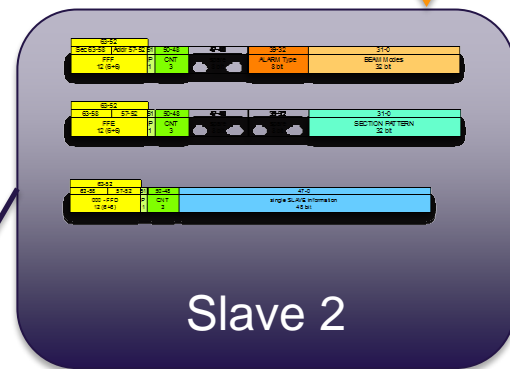
31



S. Karstensen Created on Fri Feb 08 2013 Modified on Mon Aug 19 2013

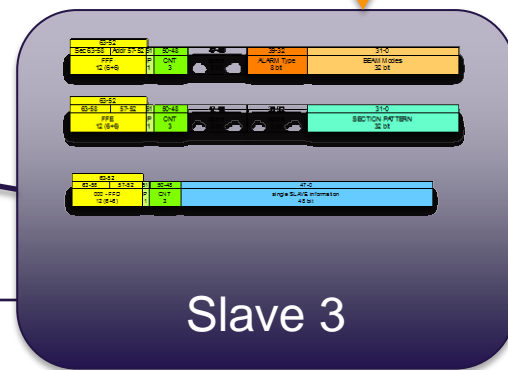
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**
- 3.) Slave info **low**

Alarm



Slave 2

Alarm



Slave 3

timing



OR

OR  
OR

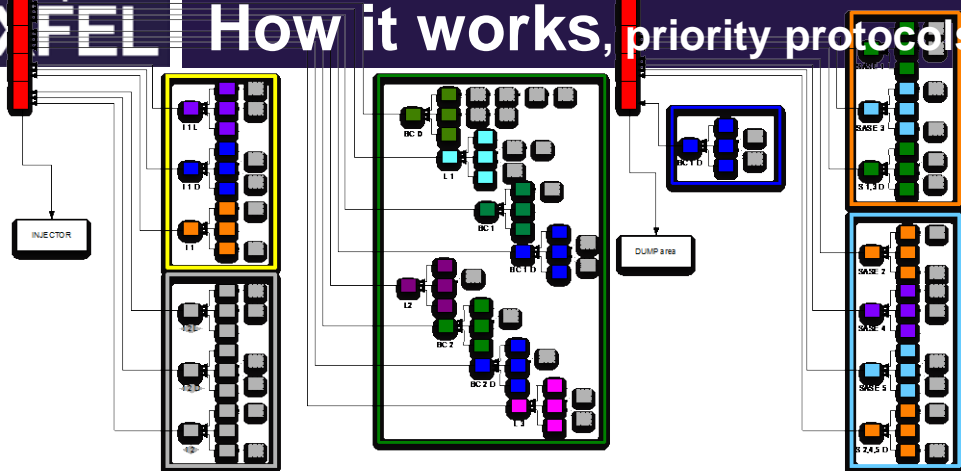
Slave 1

Master

ALARM out

# How it works, priority protocols

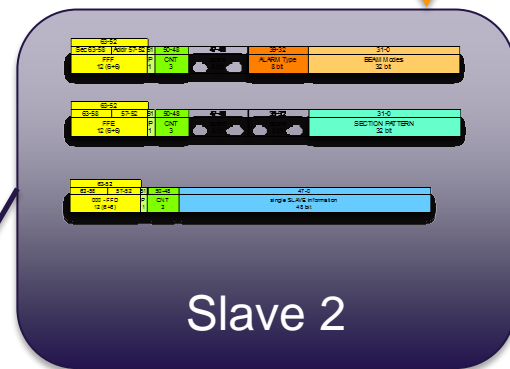
32



S. Karstensen Created on Fri Feb 08 2013 Modified on Mon Aug 19 2013

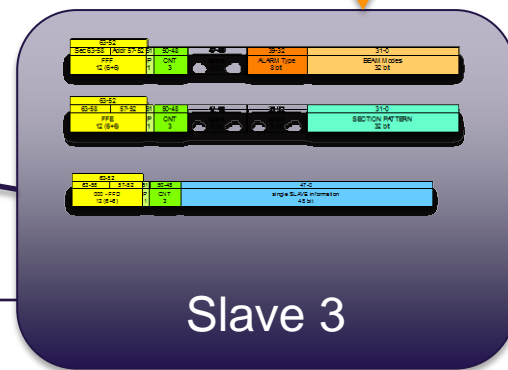
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**
- 3.) Slave info **low**

Alarm

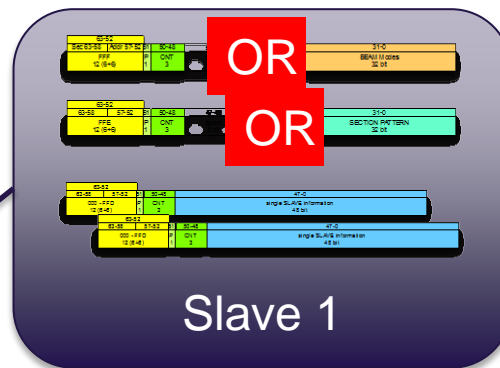


Slave 2

Alarm



Slave 3



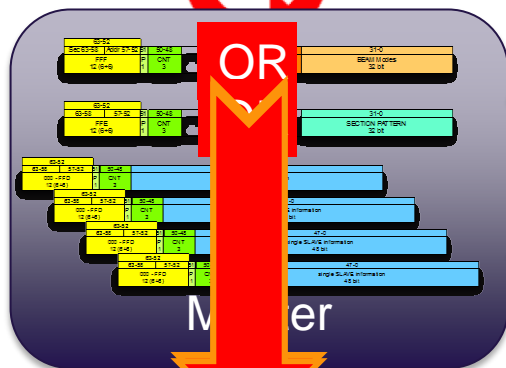
Slave 1

OR  
OR  
OR

timing



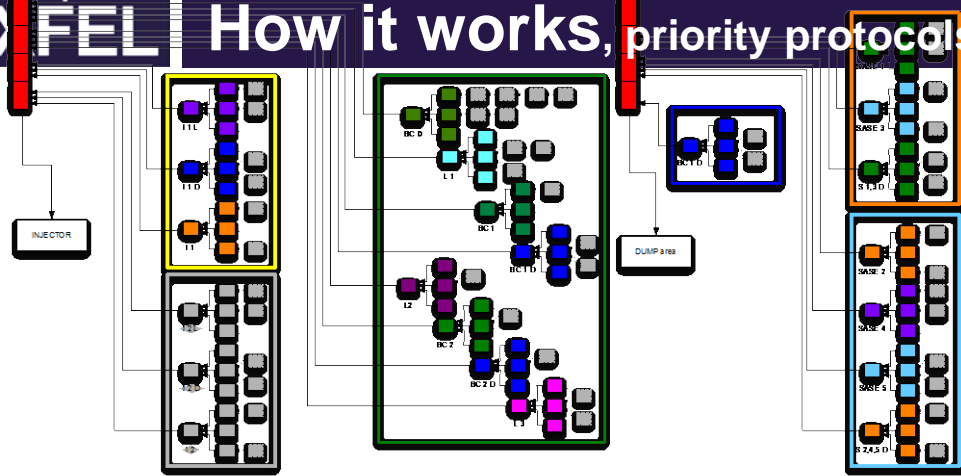
OR



Master

ALARM out

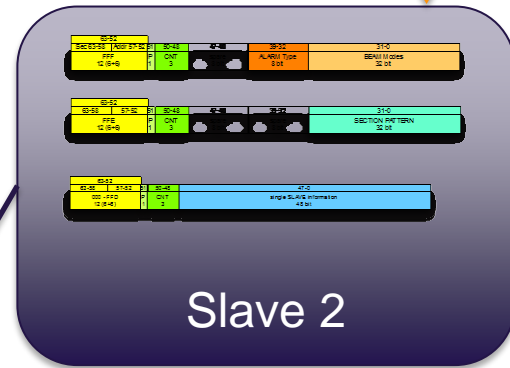
# How it works, priority protocols



S. Karstens - Created on Fri Feb 08 2013 Modified on Mon Aug 19 2013

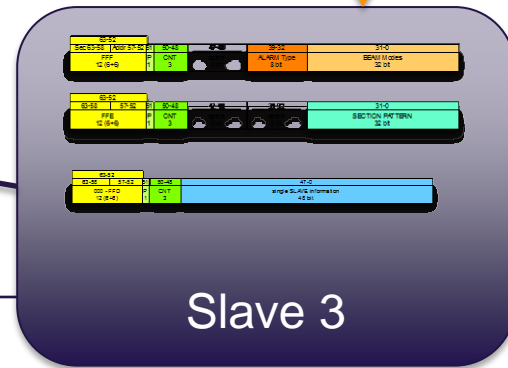
- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**
- 3.) Slave info **low**

Alarm

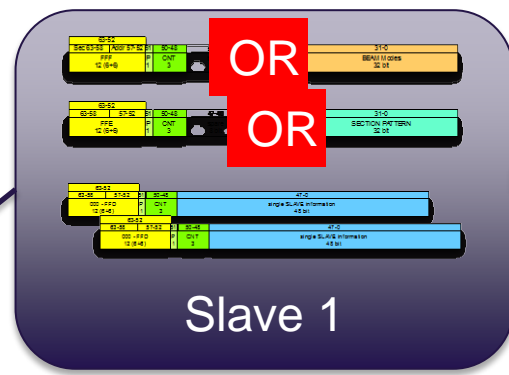


Slave 2

Alarm



Slave 3



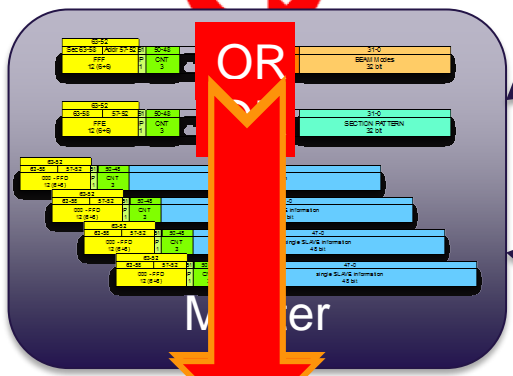
Slave 1

timing



OR

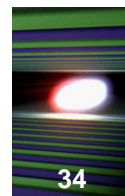
OR  
OR



Master

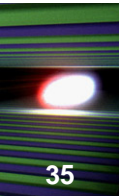
ALARM out

## Reaction Times in XFEL



Beam loss location	Distance from injector	Distance from dump	# of lost bunches
Injector	0 m	-1970 m	0
BC1	160 m	-1810 m	7
BC2	360 m	-1640 m	15
Linac center	1040 m	-930 m	44
Linac end	1650 m	-320 m	69
Beam distribution	2010 m	40 m	2
Last undulator	3010 m	1040 m	44

- ~ 50 bunches are inside accelerator
- Signal transport from dump to injector 20  $\mu$ s (2000 m)
- ~ 50 bunches generated before laser is blocked
- Using beam dump kicker reduces the number of lost bunches inside SASE Undulator sections.



What does all information of the  
slides before now mean for our  
largest problem:  
the Latency?

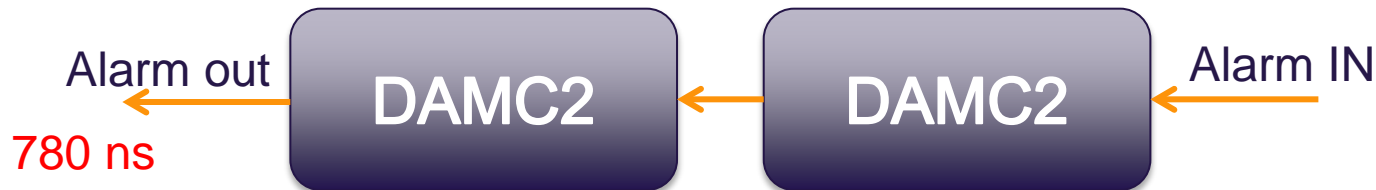


## Latency MPS-DAMC2 boards (August 2013)

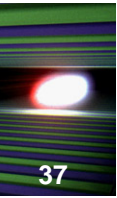
36

Fiber optics: unattended (5ns / m)  
Speed: 1.25 GBps

Latency between DAMCs will be improved.  
Factor 3 is aspired.

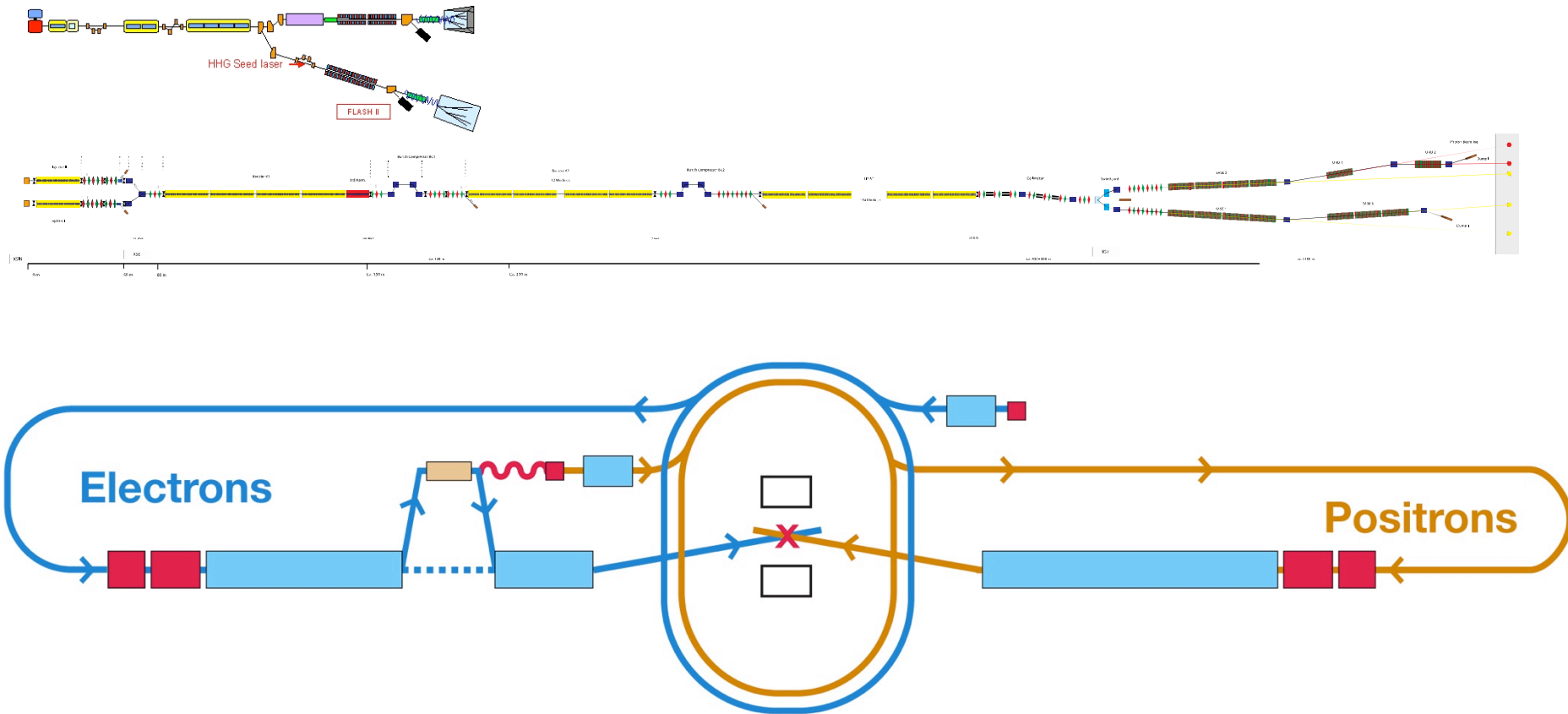


XFEL needs 20  $\mu$ sec, we peak:  $1400 \text{ ns} + 2000 \text{ m} * 5 \text{ ns/m} = 11,4 \mu\text{sec}$

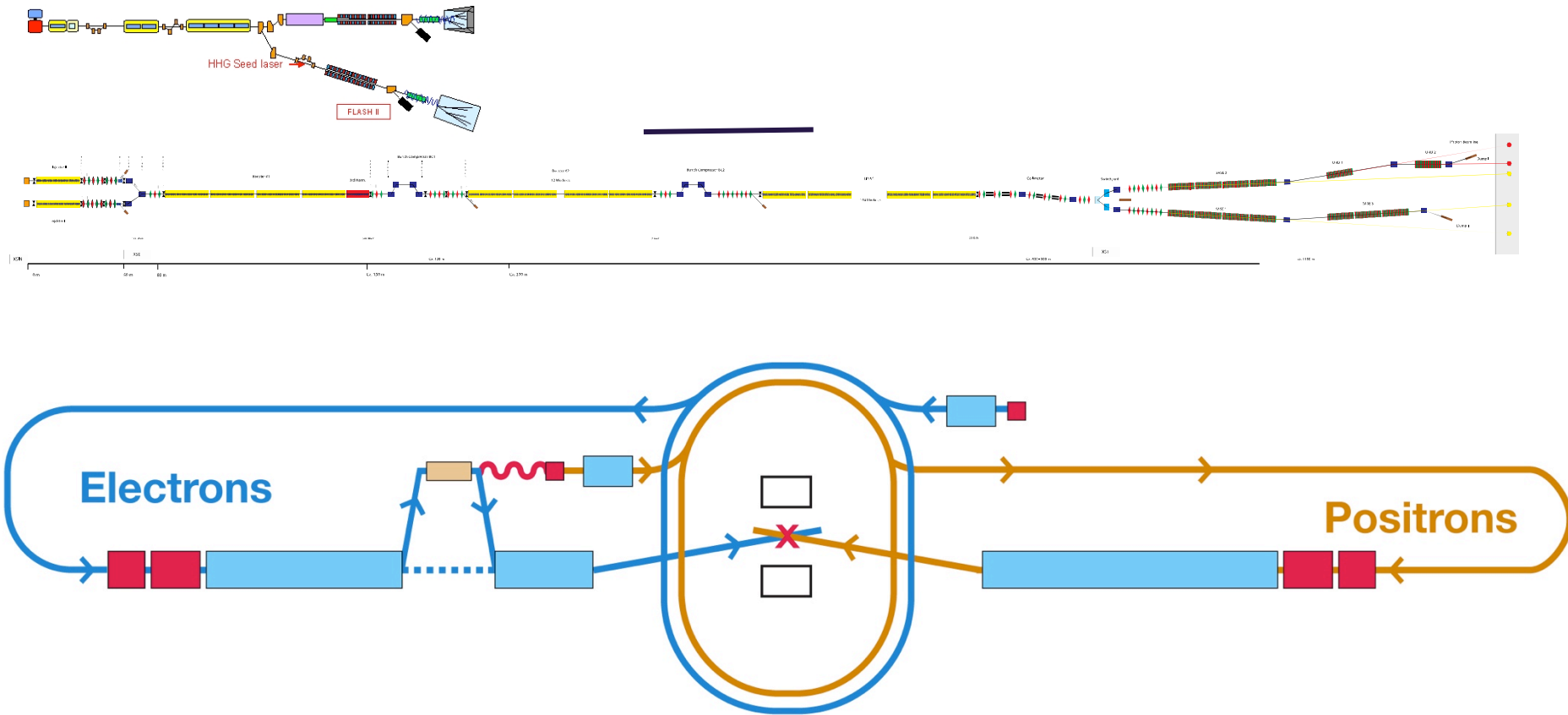


# Thank You

## scalability

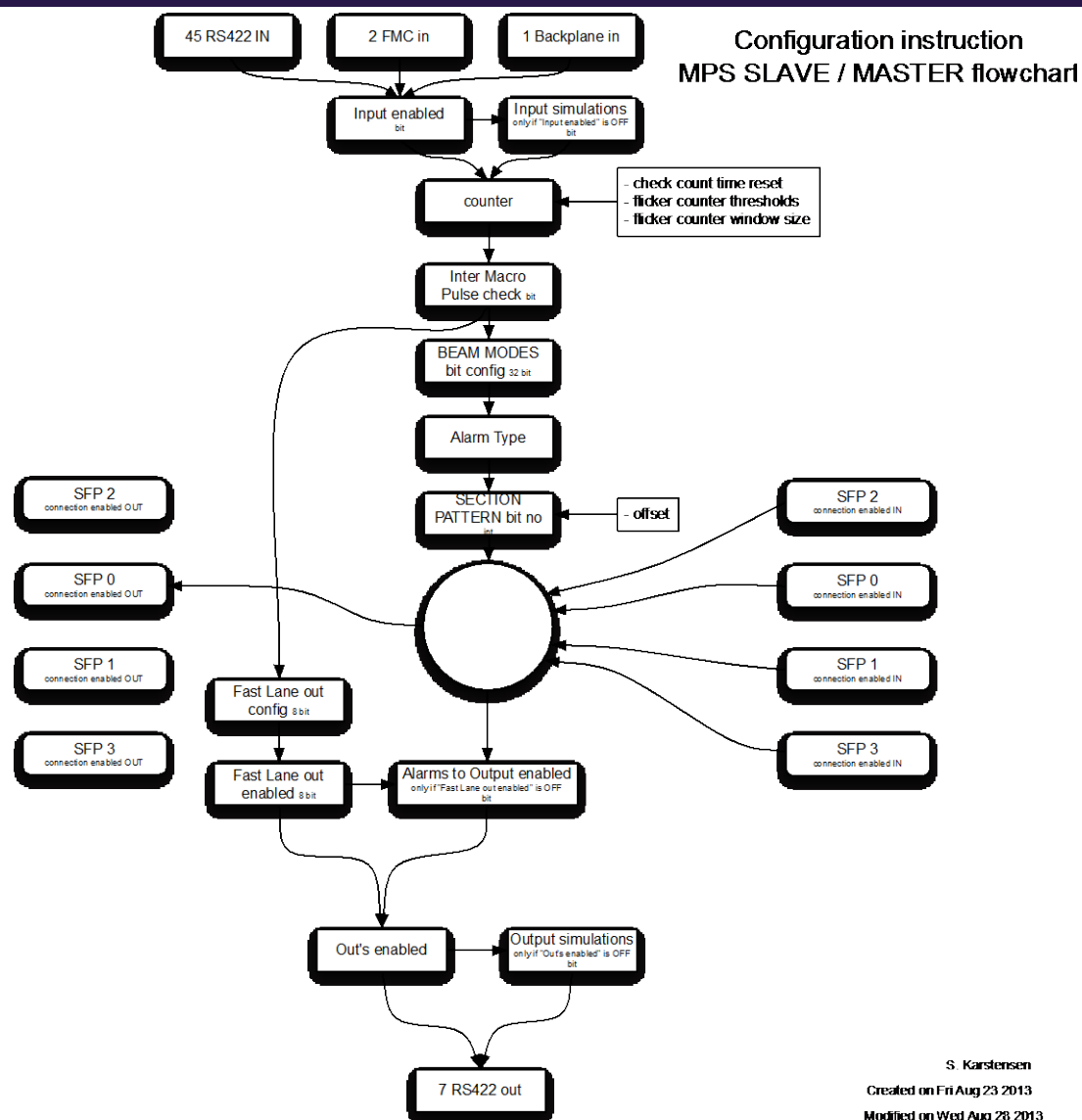


## scalability



# Configuration Instruction

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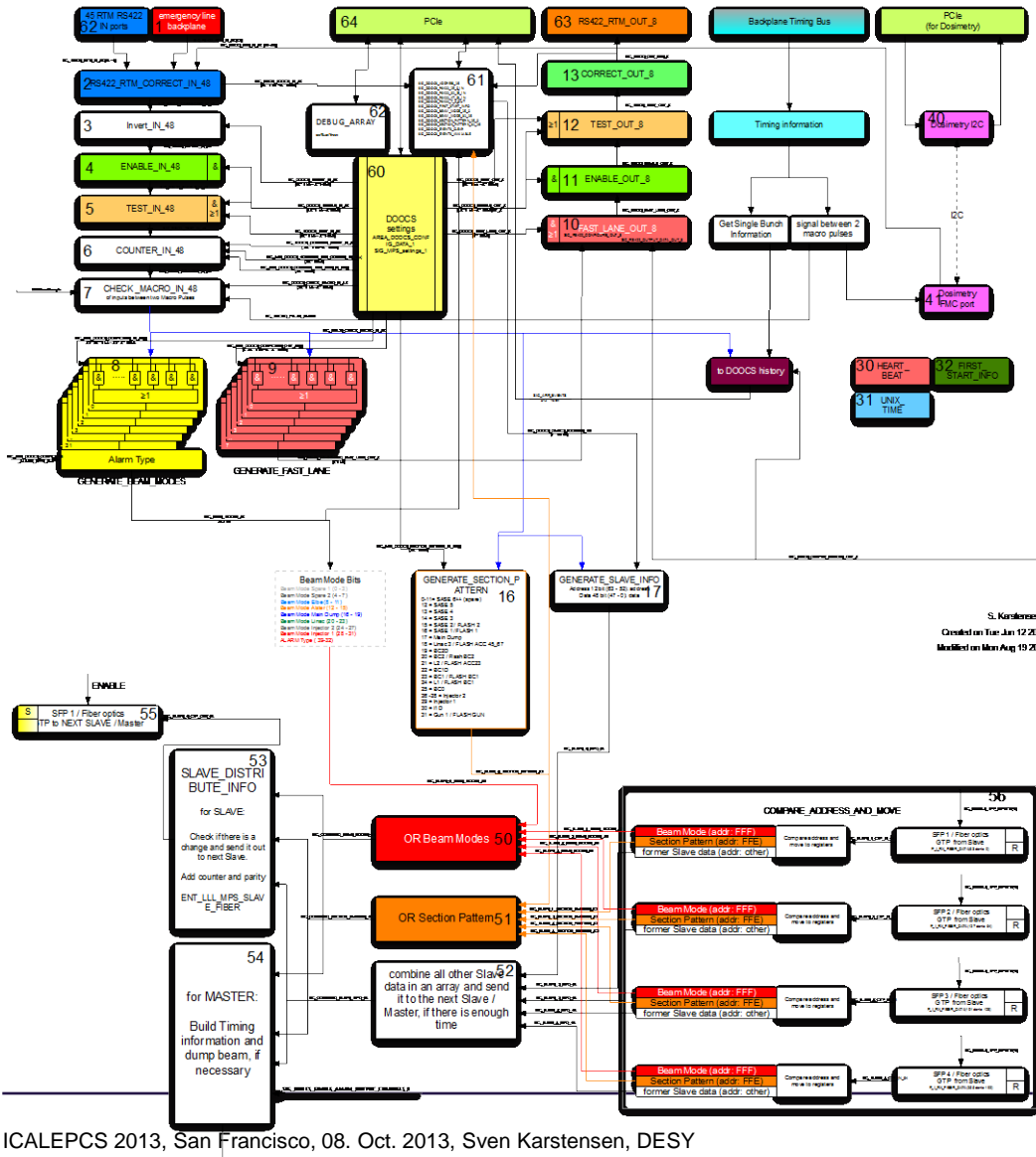


S. Karstensen

Created on Fri Aug 23 2013

Modified on Wed Aug 28 2013

### MPS SLAVE structure



- Numbers in drawing corresponding to numbers in FPGA code
- Excel Sheet includes all addresses