



中國科學院高能物理研究所

Institute of High Energy Physics, Chinese Academy of Sciences

Development a Single Cavity Regulation Based on MicroTCA.4 for SAPS-TP

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Project group of domestic MTCA.4 platform

ICALEPCS 2021, Shanghai 2021.10



China Spallation Neutron Source

CHINESE ACADEMY OF SCIENCES

Introduction

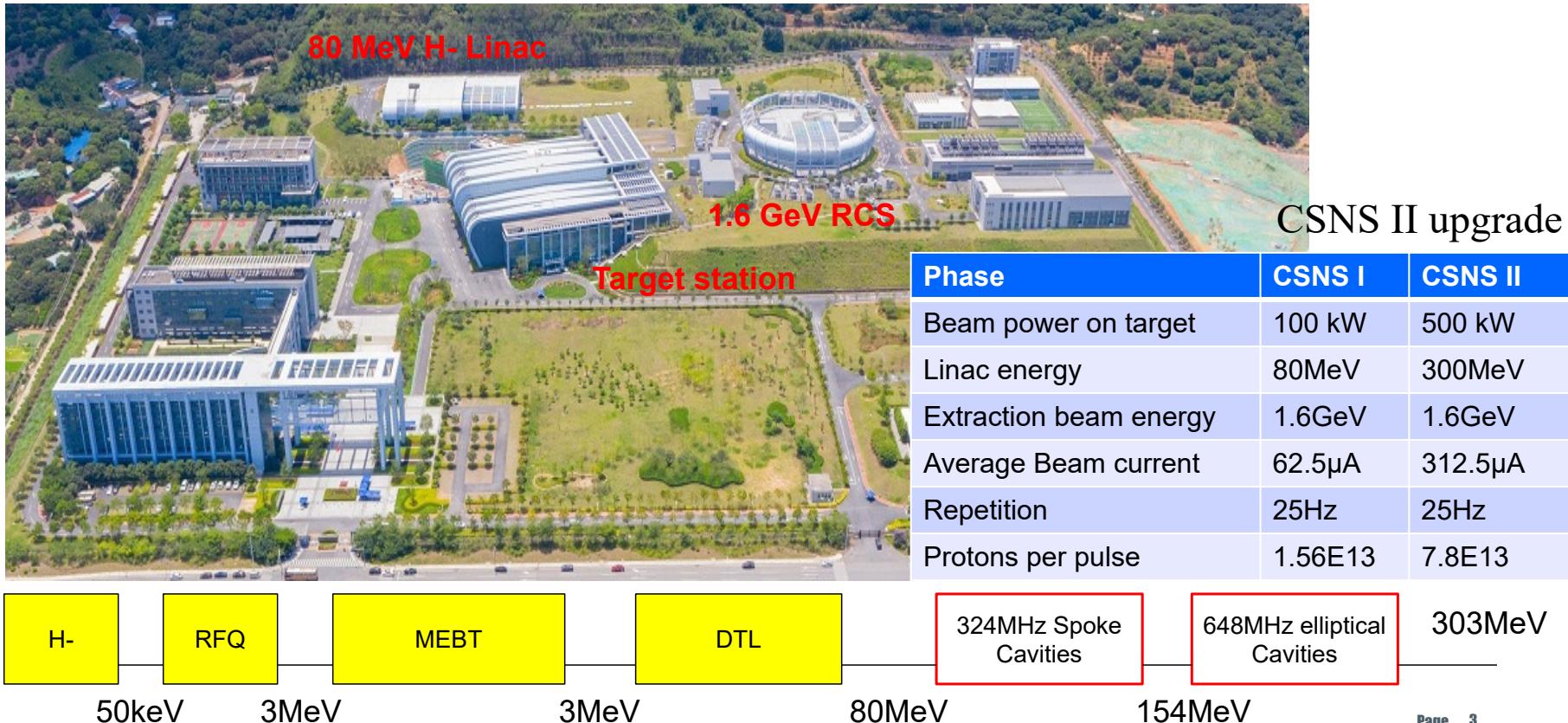
Introduction to our facilities.



Dongguan City, Guangdong Province, China

Introduction

CSNS (China Spallation Neutron Source) – China's first pulsed neutron source.



Introduction

SAPS Southern Advanced Photon Source

- 4th generation medium energy synchrotron radiation source

SAPS-TP Southern Advanced Photon Source Test platform



SAPS

Storage ring	3.5GeV
Beam energy	
emittance	31.7pm·rad
circumference	1080m
RF frequency	166.6MHz

SAPS-TP

- Superconducting RF Hall
- optical experiment Hall
- low temperature Hall
- High-accuracy measurement Hall
- Comprehensive laboratory

Introduction



2 vertical test pits

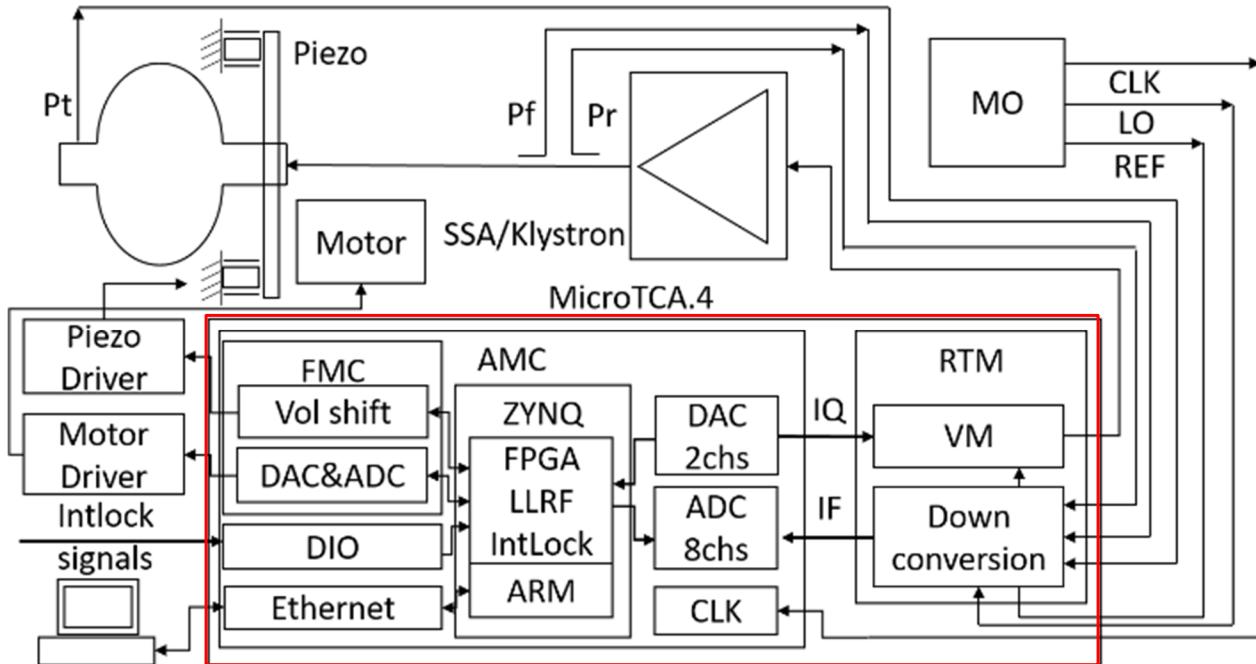


a horizon test station

Can be applied:

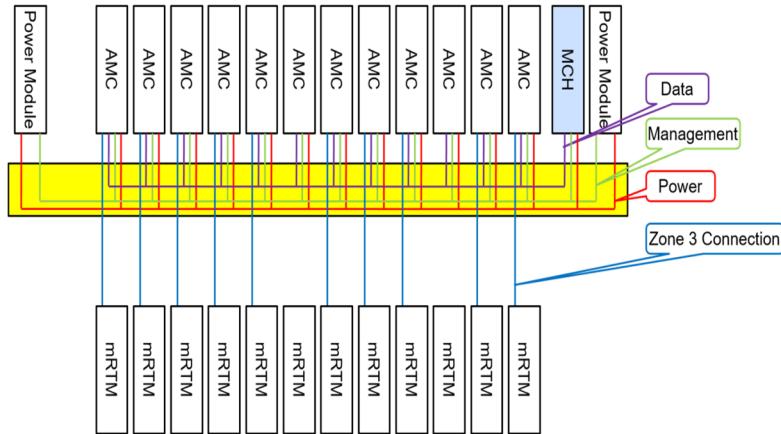
- 324 MHz spoke cavity
- 648 MHz elliptical cavity
- 500 MHz elliptical cavity
- 1.3GHz elliptical cavity
- ...

single cavity regulation - system architecture



The single cavity regulation system based on MTCA.4 for SAPS-TP

Hardware platform



A domestic MTCA.4 chassis including:

- 2 1.6kW power modules (one for redundancy)
- 2 Cooling Unit (CU) modules.



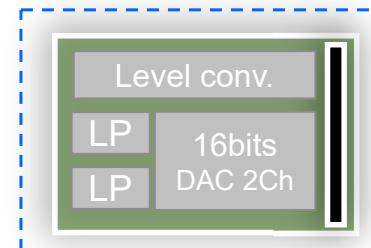
MMC mezzanine Card



A domestic multifunction digital AMC module



down-conversion and up-conversion RTM module.



tuning control FMC card
Under development

Hardware platform

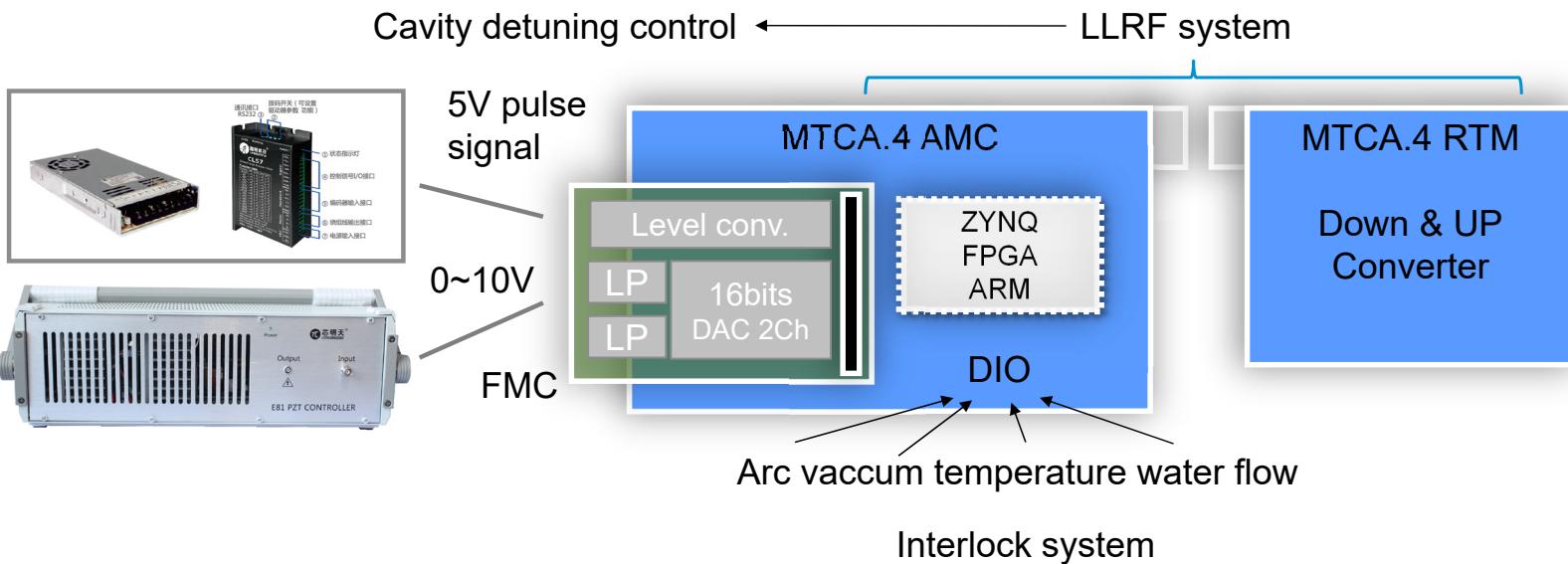
SAPS-TP 648MHz Elliptical Cavities Single Cavity Regulation based on MicroTCA.4



Motor Driver

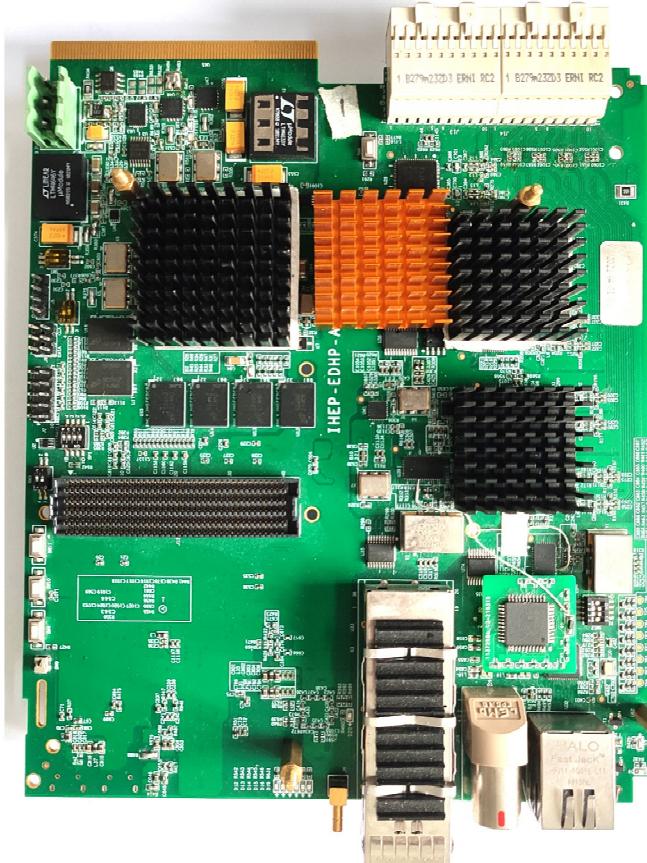


Piezo Driver



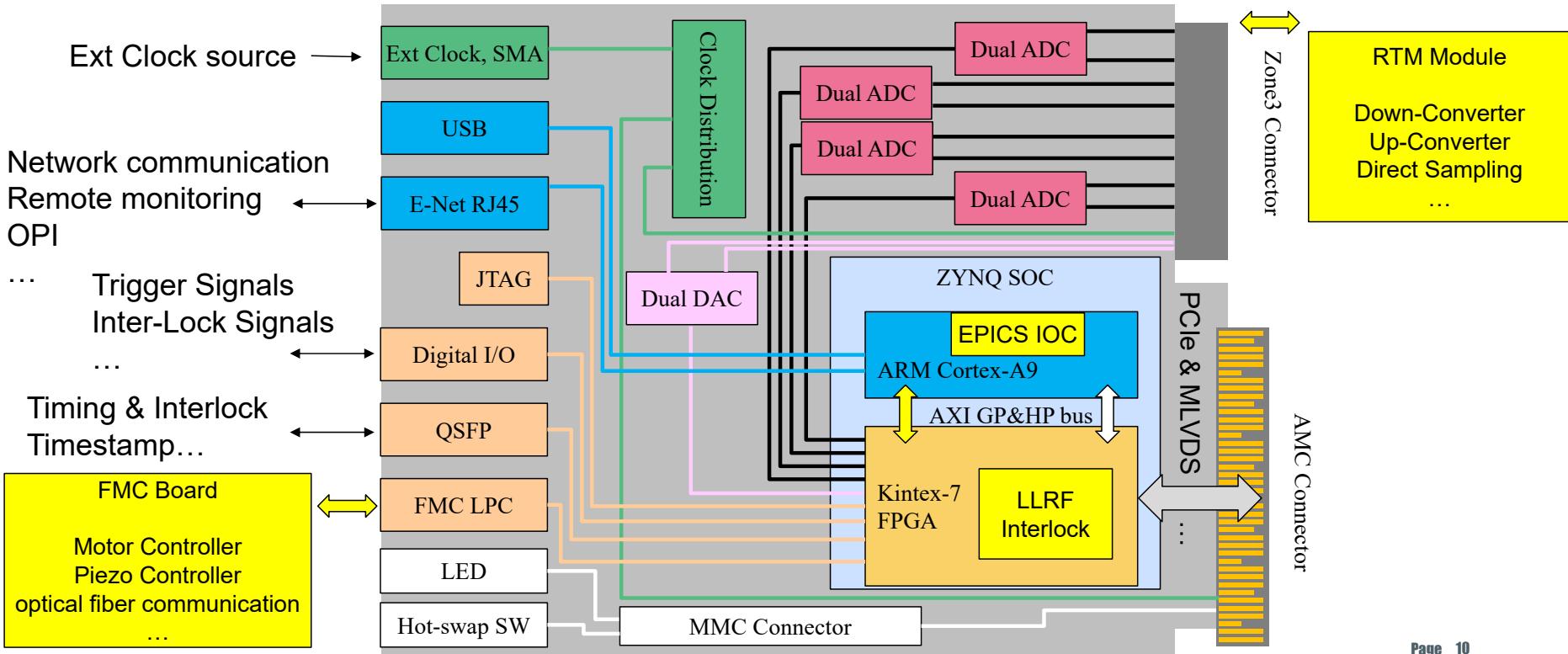
multifunction digital AMC module

- MTCA.4 standard & μRTM ZONE3 Class A1.1CO
- Double-width mid-size
- 8 Channels 125 MSPS 16-bit ADC
- 2 Channels 500 MSPS 16-bit DAC
- XC7Z045 Zynq-7000 SoC
- 2GBytes DDR3 memory size
- 1 FMC LPC Slot (VITA 57.1)
- A 4 lanes QSFP cage
- Front panel digital I/O (10 pins LVTTL)
- A Gigabit Ethernet interface
- Front panel Clock input
- A front-panel USB provides console DisplayPort



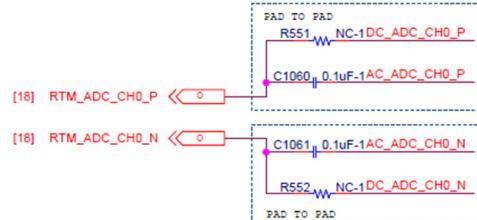
multifunction digital AMC module

A goal: one AMC board can constitute a complete system and can implement complete project applications.



multifunction digital AMC module

- AD: Analog Devices AD9268
 - 125MSPS 16bit
 - Bandwidth: 650MHz
 - Output Interface: DDR LVDS
- DA: Analog Devices AD9783
 - 500MSPS 16bit
 - Output Interface: DDR LVDS
- Compatible analog front-end circuit design
 - Intermediate frequency range: 5-100MHz
 - Direct Sampling: 5-400MHz (650MHz? Try)
 - DC coupled

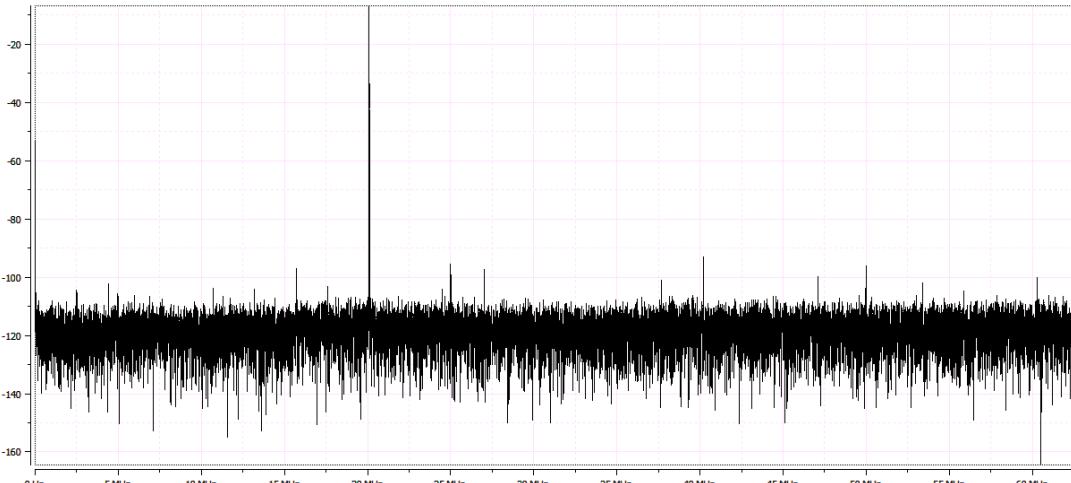


DC/AC coupled is optional

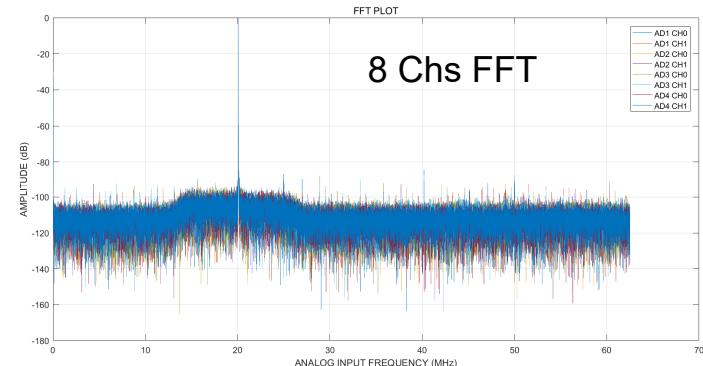
J31	1 CH9_PA+	CH9_PA-	DAC0+	DAC0-	CH9_TF+	CH9_TF-
Analog signals	2 CH8_TF+	CH8_TF-	and	and	CH8_PA+	CH8_PA-
	3 CH7_PA+	CH7_PA-	DAC1+	DAC1-	CH7_TF+	CH7_TF-
	4 CH6_TF+	CH6_TF-	gnd	gnd	CH6_PA+	CH6_PA-
	5 CH5_PA+	CH5_PA-	DAC2+	DAC2-	CH5_TF+	CH5_TF-
	6 CH4_TF+	CH4_TF-	gnd	gnd	CH4_PA+	CH4_PA-
	7 CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
	8 CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
	9 CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
	10 CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-

2 channels DA 8 channels AD

multifunction digital AMC module



- AD Test
 - IHEP-EDHP-AMC + SIS8900 RTM
 - Signal Source: 20MHz 3dBm
 - 125MSPS

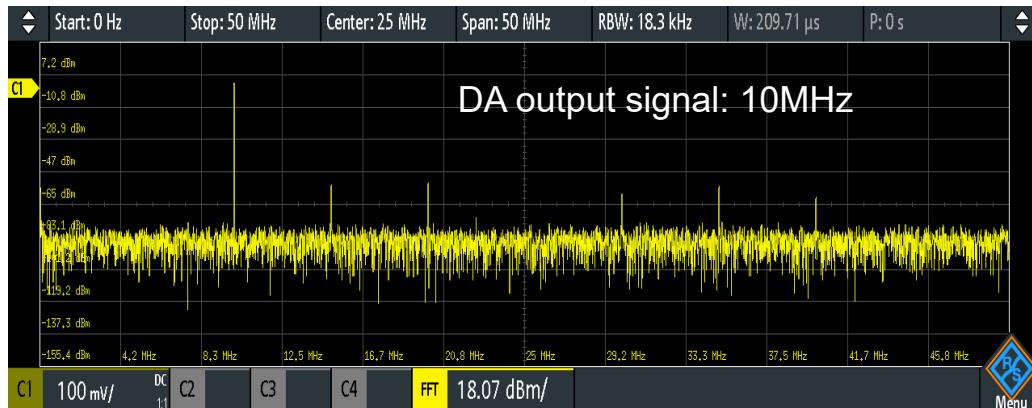


multifunction digital AMC module

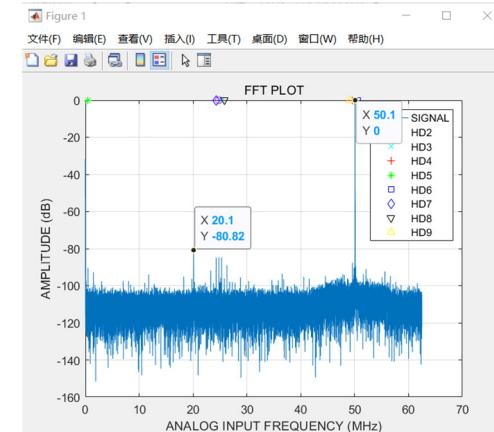
- Channel isolation

	AD1_CH 0	AD1_CH 1	AD2_CH 0	AD2_CH 1	AD3_CH 0	AD3_CH 1	AD4_CH 0	AD4_CH 1
AD1_CH0		74.95						
AD1_CH1	84.32		80.89					
AD2_CH0		75.22		77.1				
AD2_CH1			82.16		80.82			
AD3_CH0				87.3		79.46		
AD3_CH1	Isolation of adjacent channels				78.89		85.59	
AD4_CH0						94.8		85.13
AD4_CH1							78.1	

- DA Spectrum



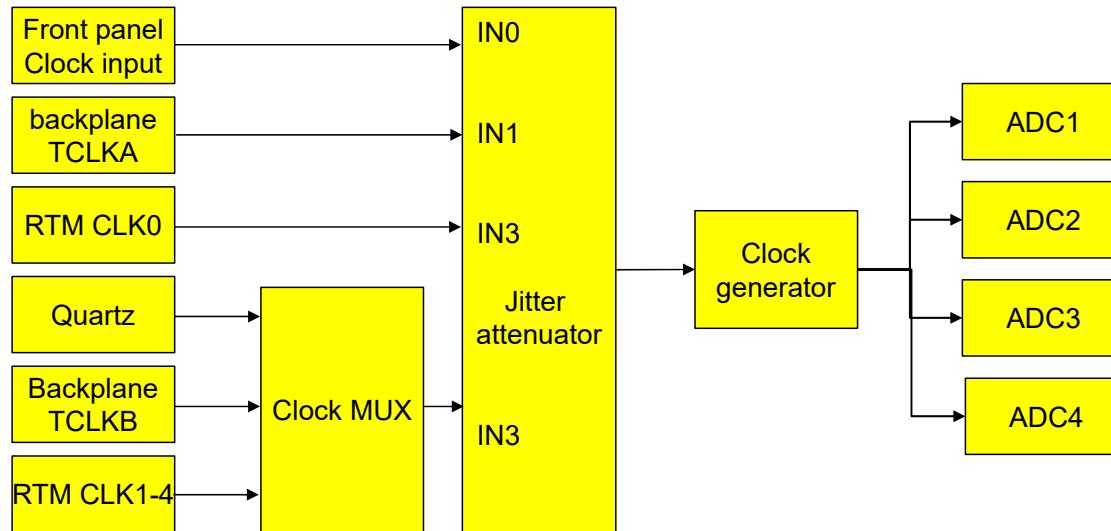
- + Adaptor RTM
SNR: 78.1 dB
some larger harmonic component



Isolation Test

multifunction digital AMC module-Clock Distribution

- ultra-low clock jitter
 - 648MHz direct sampling LLRF 0.1° jitter (<423fs pp)
 - Jitter attenuator + Low phase noise clock generator
 - Theoretical clock jitter $\approx 240\text{fs pp}$ (170fs RMS)



multifunction digital AMC module-FMC Slot

- Compatible with FMC LPC standard & 4 high-speed serial transceiver pairs.

DFMC-MD22



DFMC-AD16



DFMC-UNI-IO



DFMC-SFP4



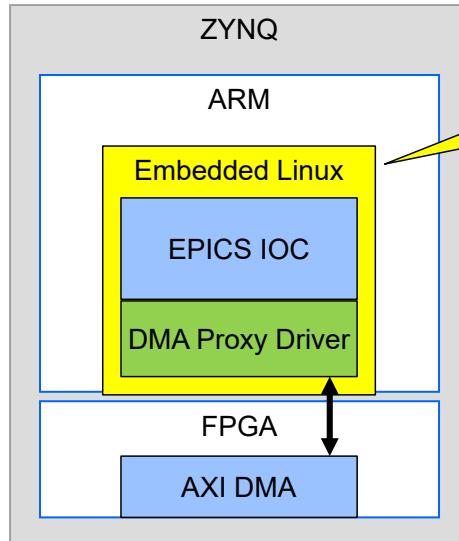
Compatible commercial FMC cards

K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC
2	NC	NC	PRSNL_M2C_L	CLK0_C2M_P	NC	NC	GND	DP0_C2M_P	DP1_M2C_P
3	NC	NC	GND	CLK0_C2M_N	NC	NC	GND	DP0_C2M_N	DP1_M2C_N
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	GND
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	DP2_M2C_P
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	DP2_M2C_N
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	GND
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	DP3_M2C_P
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	DP3_M2C_N
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	GND
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	DP3_M2C_P
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	DP3_M2C_N
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	GND
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	GND
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	GBTCLK1_M2C_P
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	GBTCLK1_M2C_N
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	GND
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	DP1_C2M_P
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	DP1_C2M_N
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	GND
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	GND
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	DP2_C2M_P
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	DP2_C2M_N
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	GND
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	DP3_C2M_P
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	DP3_C2M_N
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	GND
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	GA1
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	12P0V
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC

FMC LPC引脚

Software development

- Embedded Linux Development for ZYNQ chip

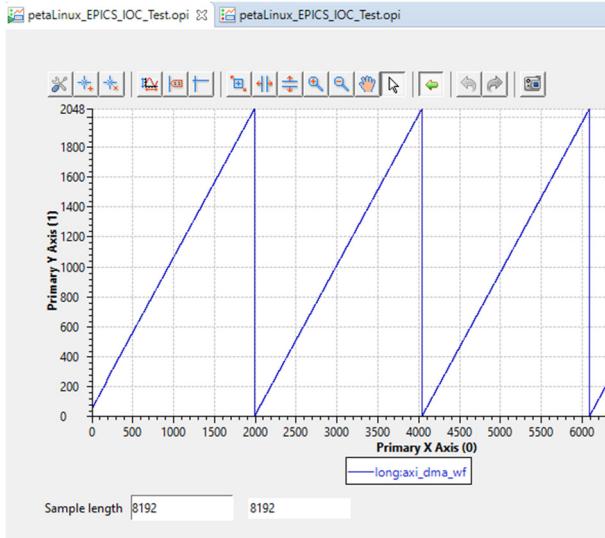


EPICS IOC Demon

PV: AI AO Waveform

Open source Linux kernel

Tool: Xilinx petalinux

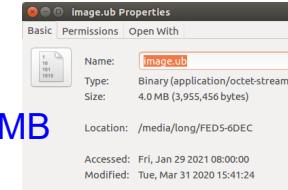


Linux Boot Image



23MB

Linux Kernel Image



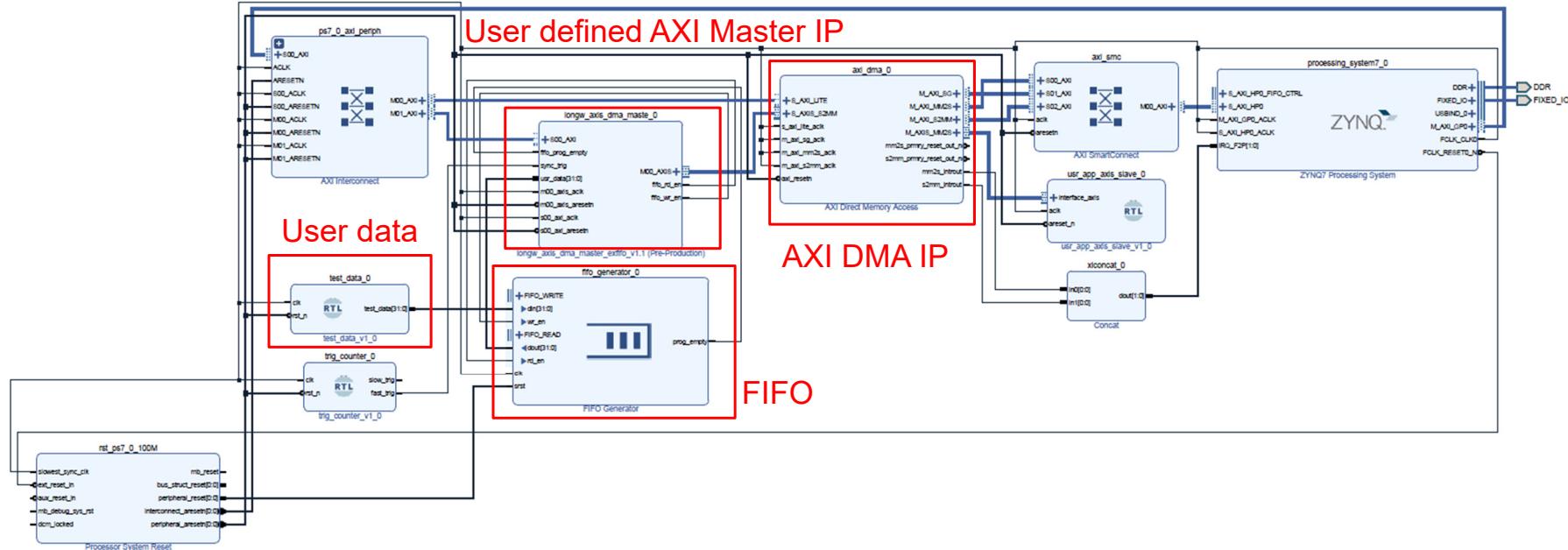
Accessed: Fri, Jan 29 2021 08:00:00
Modified: Tue, Mar 31 2020 15:41:24

45MB

```
COM3 - PuTTY
epics> dbl
long:aiExample
long:aiExample1
long:ai1
long:aiExample2
long:ai2
long:aiExample3
long:ai3
long:axi_dma_wf
long:compressExample
long:aSubExample
long:calcExample
long:calcExample1
long:calc1
long:calcExample2
long:calc2
long:calcExample3
long:calc3
long:xxxExample
long:subExample
epics> dbgf long:axi_dma_wf
DBR_FLOAT[100]: 1
4 5
8 9
```

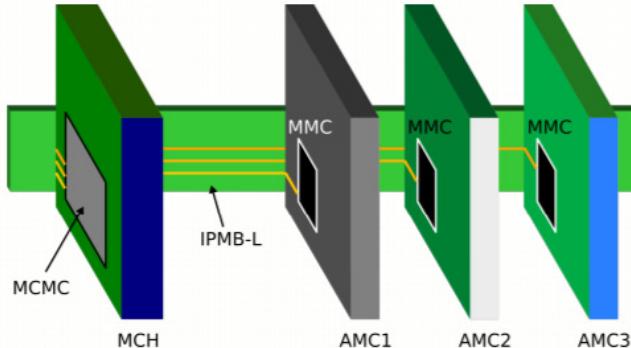
Software development

- Embedded Linux Development for ZYNQ chip



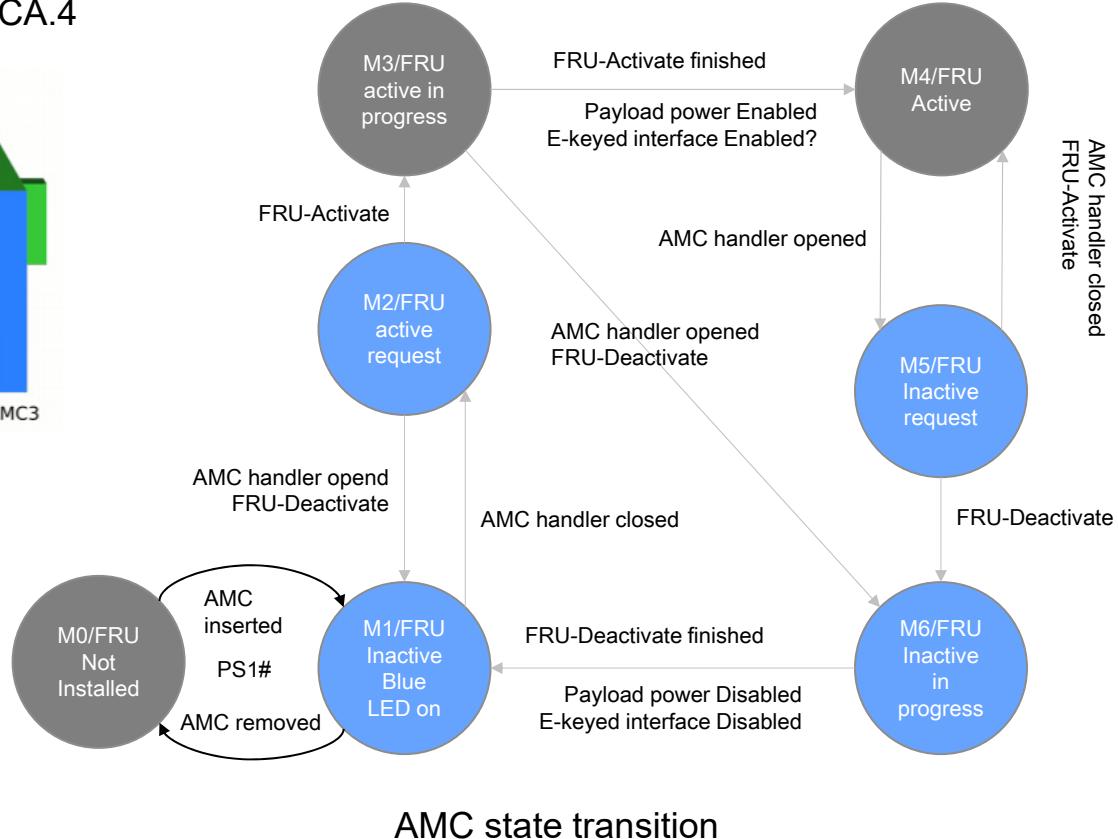
MMC controller mezzanine Card

Management subsystem of MicroTCA.4



Functions:

- AMC state management
- Hot swap management
- Sensor monitoring (Voltage, temperature, handler, ...)
- LED management
- Threshold event management
- ...



MMC controller mezzanine Card

Test environment:

Commercial nVent MTCA.4 chassis

N.A.T NAT-MCH-PHYS80 MCH card



MMC Controller in AMC

FRU	Device	State	Name
0	MCH	M4	NAT-MCH-CM
3	mcmc1	M4	NAT-MCH-MCMC
9	AMC5	M4	IHEP-AMC-V1.0
40	CU1	M4	Schroff uTCA CU
51	PM2	M4	NAT-PM-AC1000
60	Clock1	M4	MCH-Clock
61	HubMod1	M4	MCH-PCIe

Module operational state management

Hot swap management works well.



MMC Controller Testbench

```
nat> show_sensorinfo 9
```

Sensor Information for FRU 9 / AMCs

#	SDR	Type	Sensor Entity	Inst	Value	State	Name
-	MDevLoc		0xc1	0x65			IHEP-AMC-V1.0
1	Full	Temp	0xc1	0x65	30 C	ok	Temp PCB1
2	Full	Temp	0xc1	0x65	32 C	ok	Temp PCB2
3	Full	Temp	0xc1	0x65	33 C	ok	Temp PCB3
4	Full	Voltage	0xc1	0x65	1.00 V	ok	1V0
5	Full	Voltage	0xc1	0x65	1.20 V	ok	1V2
6	Full	Voltage	0xc1	0x65	1.50 V	ok	1V5
7	Full	Voltage	0xc1	0x65	1.80 V	ok	1V8
8	Full	Voltage	0xc1	0x65	2.50 V	ok	2V5
9	Full	Voltage	0xc1	0x65	3.30 V	ok	3V3PP
10	Full	Voltage	0xc1	0x65	3.45 V	ok	3V3MP

Software layers

IPMI communication

protocol packet parse

protocol packet build

Sensors monitor

Threshold event manage

LED manage

Hot swap manage

AMC State machine

Sensors drivers

I2C driver

Temperature threshold event Test

```
[00:00:00:30:0463] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper non-critical go high' - assertion  
82°C  
[00:00:00:30:0473] LSHM(0): temperature exceeded - increase fan level  
Fan speed increase  
[00:00:00:30:0479] LSHM(0): CU0 set fan to level 100%  
[00:00:00:30:0485] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper critical go high' - assertion  
[00:00:00:30:0695] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper non-recoverable go high' - assertion  
[00:00:00:30:0705] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper non-recoverable go high' - assertion  
30°C  
[00:00:00:55:0127] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper non-recoverable go low' - assertion  
[00:00:00:55:0137] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper critical go low' - assertion  
[00:00:00:55:0147] LSHM(0): FRU 5 sensor 16 LUN 0 'Temp PCB1'  
temperature 'upper non-critical go low' - assertion  
[00:00:01:10:0765] LSHM(0): temperature in range - decrease fan level  
Fan speed decrease  
[00:00:01:10:0771] LSHM(0): CU0 set fan to level 80%
```

Tuning control FMC



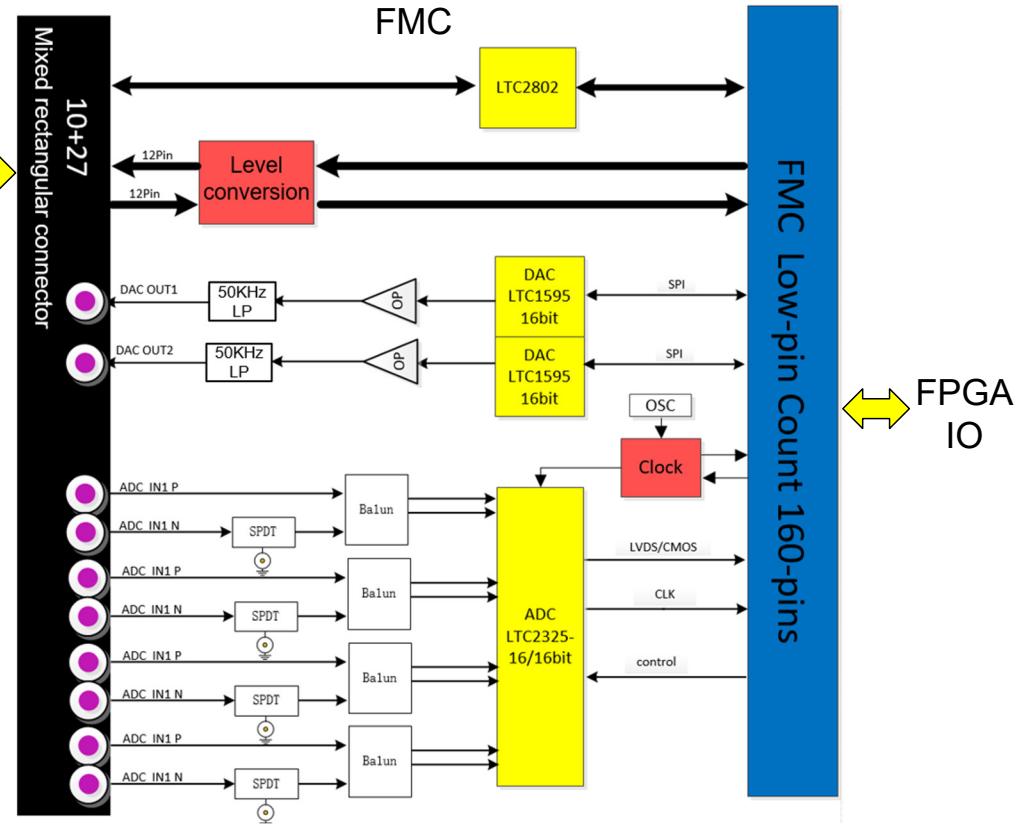
Motor Driver



Piezo Driver



Piezo1 position sensor
Piezo2 position sensor
pressure sensor
Step motor position
(rotary transformer)



Others

- The domestic Down and up converter RTM and Direct sampling RTM is developed by the colleagues in the project group.
 - Based on the requirement of SAPS and CSNS II.
 - Down-conversion RF: 300MHz~4GHz IF: 5~100MHz Up-conversion RF 200MHz~4GHz
 - Direct sampling RTM (RF: DC~650MHz)



Provided by: Dr. Ma X P, and Dr. Gan N



Demostic MTCA.4 chassis
Provided by: Yzitech

Thanks for your attention!