

Baseband Digital Network Analyzer for LLRF Controllers

Samson Mai*, A. Singh, G. Narayan, F. Severino, K. Mernick, M. McCooley, K. Fahey

*smai@bnl.gov

Brookhaven National Laboratory, Upton, NY 11973

"This work was supported by the EIC Project and the U.S. Department of Energy, Contract DE-SC0012704."

Digital Network Analyzers (DNA) have been implemented in many LLRF systems, notably NSLS-II [1] and CERN [2], to help tune feedback loops. DNA characterize feedback loops by measuring the frequency-dependent magnitude and phase transfer functions. It enables the measurement of open loop gain, gain/phase margin, and loop delay to help fine-tune feedback loops. The DNA has been developed on FPGA and integrated into the current RHIC LLRF infrastructure [3]. It has been tested with an implementation of one-turn delay feedback (OTFB) on the bench to maximize gain and stability. The DNA performance has been used to characterize a RHIC 28MHz cavity in the Accelerator Physics Experiment (APEX) to test transient beam loading compensation strategies.

What is a Network Analyzer?

A Network Analyzer is an instrument that characterizes the electrical properties of circuits. It sends a stimulus to a system and records the data coming back to calculate the magnitude and phase response.

Digital Network Analyzer

- ✓ Can be integrated into every LLRF chassis with 1 DAC and 1 ADC
- ✓ Initial labor costs for development
- ✗ Only measures transmission
- ✓ Python for Digital Signal Processing analysis
- ✓ Flexible Injection/Capture wrt. digital loop

Vector Network Analyzer

- ✗ Physical piece of equipment, need splitters, cables, adapters, etc.
- ✗ Expensive
- ✓ Measures transmission and reflection
- ✓ Integrated post-processing software
- ✗ External Injection/Capture wrt. digital loop



Figure 1: Current RHIC LLRF Controller containing DAC, ADC, Motor Control daughtercards.



Figure 2: Rohde Schwarz ZVA40 Vector Network Analyzer

Stimulus/ADC Capture

The stimulus for the DNA is generated in firmware using numerically-controlled oscillators (NCOs). The NCO contains a frequency tuning word as input, a phase accumulator, and a quarter-sine look up table (LuT). The frequency tuning word is programmed to be linearly increasing to create a chirp – a sine-wave whose frequency is changing over time. A second LuT at a 90° offset is used to create the quadrature component. The stimulus operates at baseband, and gets IQ modulated to RF frequency. The chirp is flexible with programmable start/end frequency, duration, and power. Currently, the chirp can be injected into 3 different points shown in Fig. 6 to measure different transfer functions.

An ADC on the LLRF controller is used to capture the system response to the stimulus. The incoming data gets IQ demodulated to baseband, low-pass filtered, and stored into DDR2 memory.

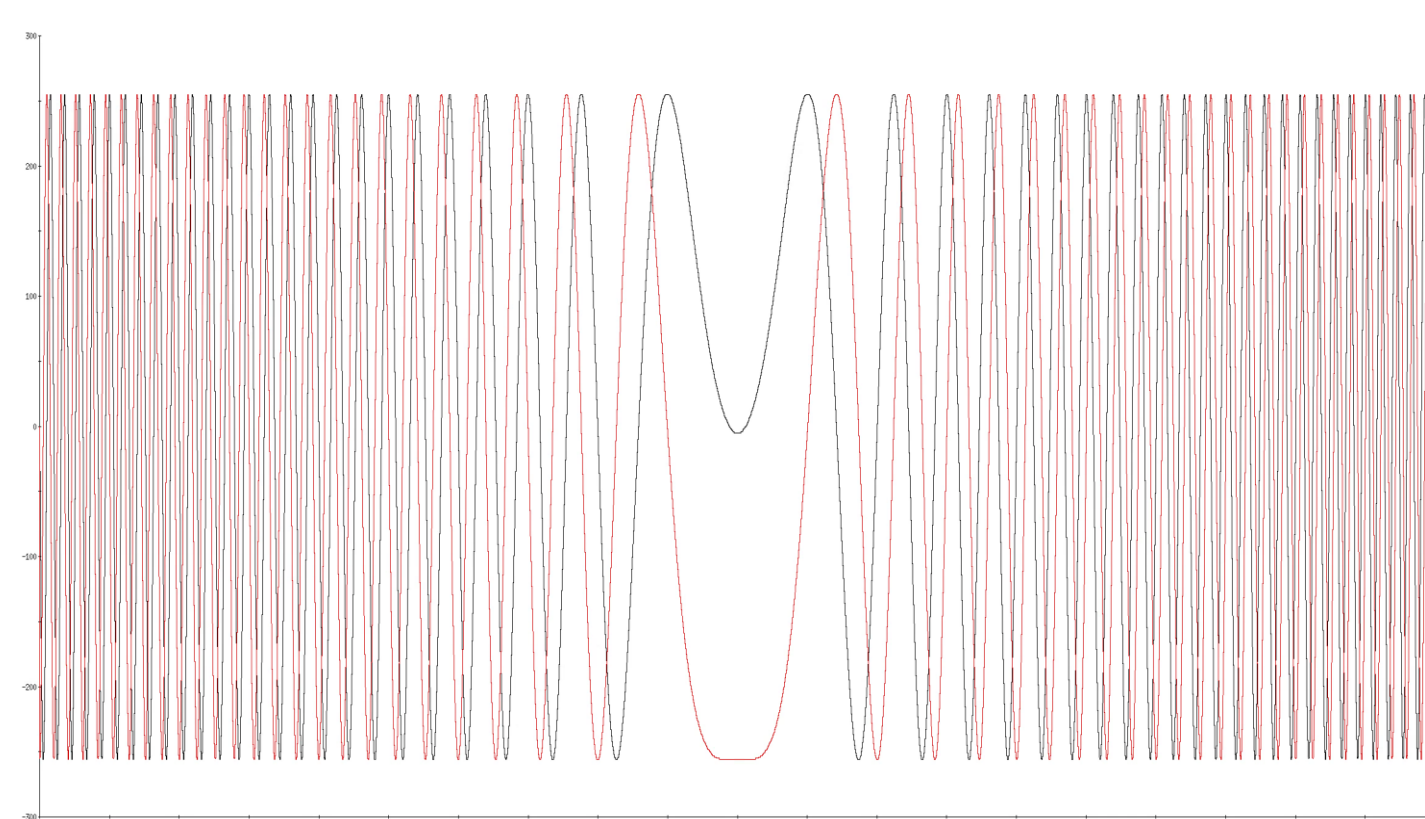


Figure 3: Baseband IQ chirp sweeping from negative frequency to positive frequency. In-phase components (black) and quadrature components (red).

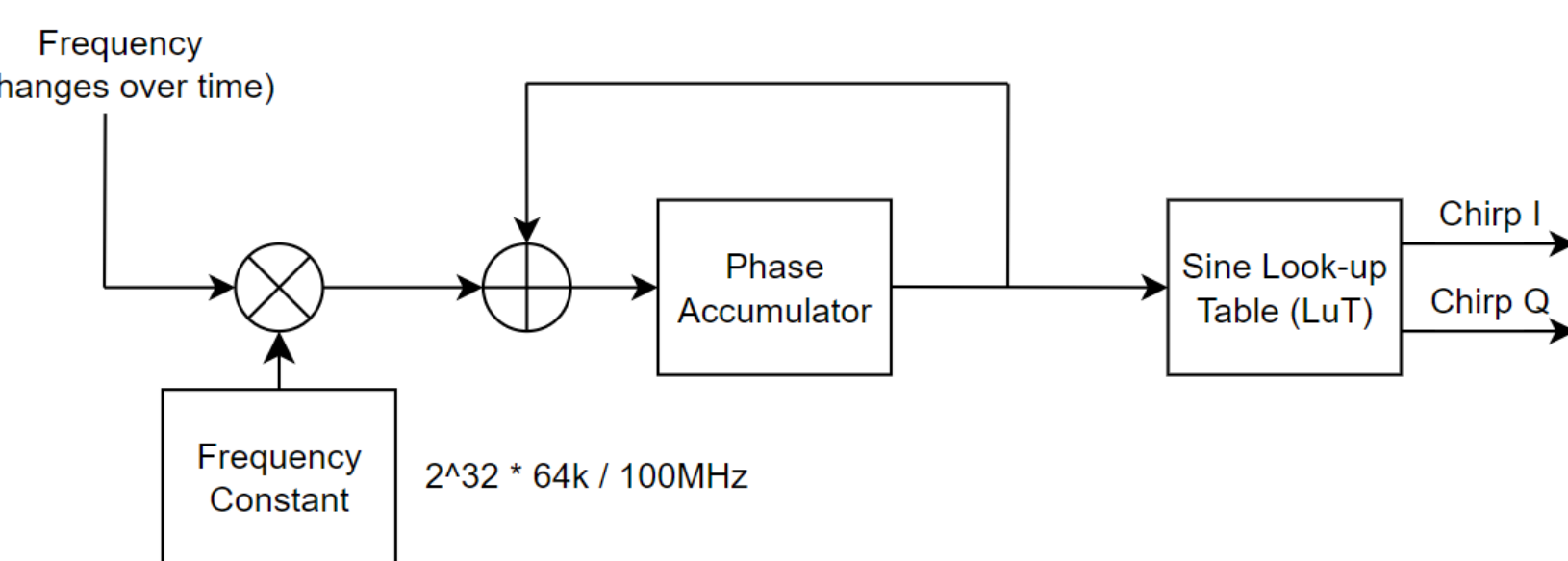


Figure 4: Simplified block diagram of chirp. The frequency is linearly swept and added to the phase accumulator every clock cycle. The BRAM LuT uses the phase index to create the IQ sweep.

Digital vs Vector Network Analyzer

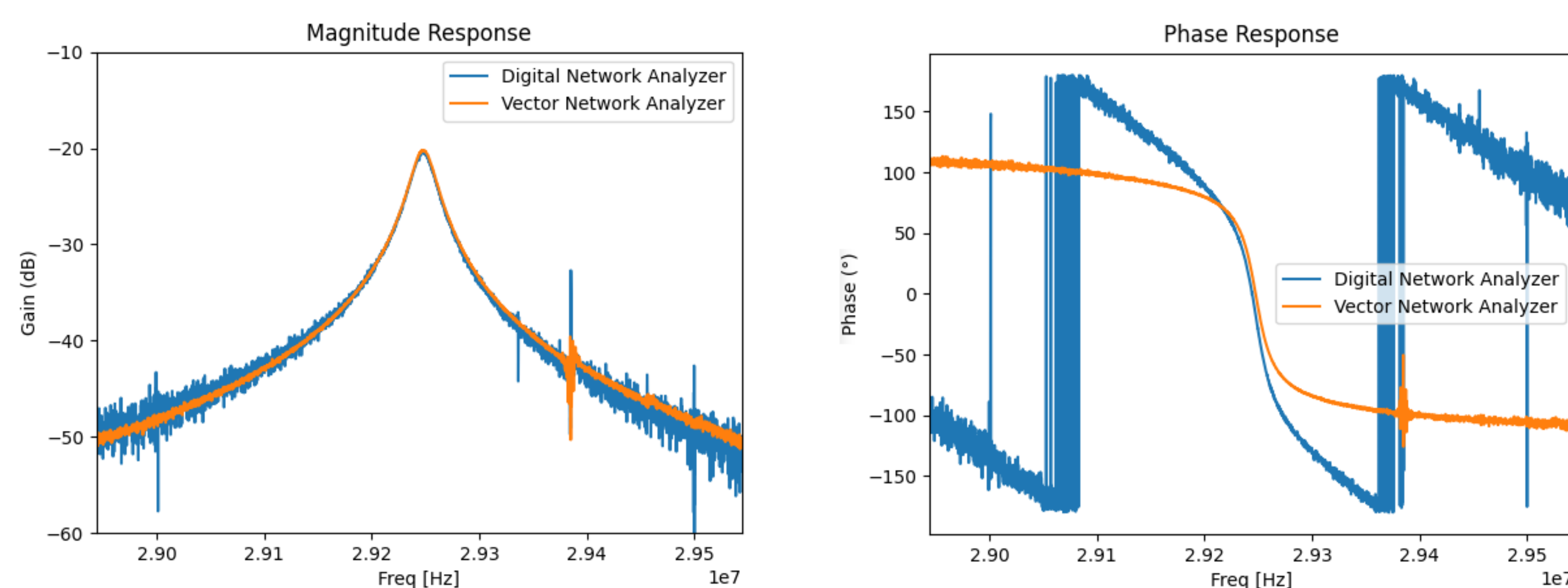


Figure 5: Direct comparison of the Digital and Vector Network Analyzers. Both closed loop measurements were performed with the same PID settings on a cavity simulator. The differences in phase response can be attributed to different loop delays.

Post-processing

Python scripting is used to trigger sweeps and extract captured data from DDR2 memory. Complex Fast Fourier Transforms (FFT) are performed on IQ data to calculate magnitude and phase responses. Eq. (1) and (2) shows the calculations for the magnitude and phase response. $X(s)$ represents the FFT of the complex chirp while $Y(s)$ represents the FFT of the complex output. The magnitude response is estimated to be the cross spectral density divided by the power spectral density [4].

$$\text{Mag} = 20 * \log_{10} \left| \frac{Y(s) * X(s)^*}{X(s) * X(s)^*} \right| \quad (1)$$
$$\text{Phase} = \arctan \left(\frac{Y(s) * X(s)^*}{X(s) * X(s)^*} \right) \quad (2)$$

Figure 6: Diagram shows a negative feedback control loop with a controller and plant. In each operating mode, a chirp injection is summed into a different point in the LLRF control loop.

Eq. (1) and (2): Calculation for magnitude and phase response.

APEX Test on RHIC 28MHz Cavity

The Digital Network Analyzer has been verified on a RHIC 28MHz cavity. During an APEX, the DNA was used to take a measurement of a cavity with the analog direct RF feedback loop closed. We noticed an asymmetrical peak 200kHz offset from the carrier frequency, so we used a VNA to cross-check the results. Upon further analysis, we found that the fast feedback phase margins were off by 40°. 2.5 ns of cable delay was added to the RF amplifier chain to bring the system back closer to optimal phase margins. Fig. 7 shows that after adding the delay, the peak disappears.

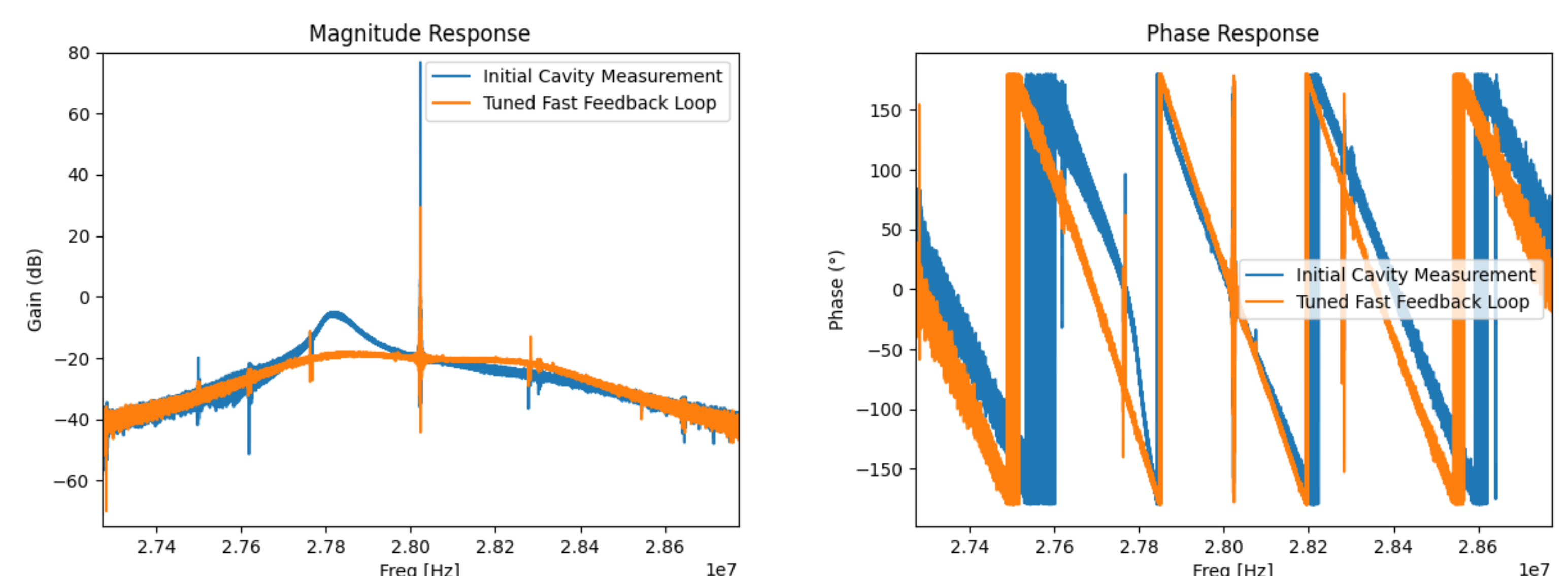


Figure 7: Magnitude (left) and phase (right) response before (blue) and after (orange) tuning the fast feedback loop.

One-Turn Feedback Tuning

The OTFB has been recently been developed at BNL to combat higher transient beam loading in EIC [5]. To tune the OTFB, Python scripting was used to compare ideal models of the system to DNA measurements. The script runs optimization functions to fit the model to the measurement. From the model, we can get the loop delay to tune the feedback loop.

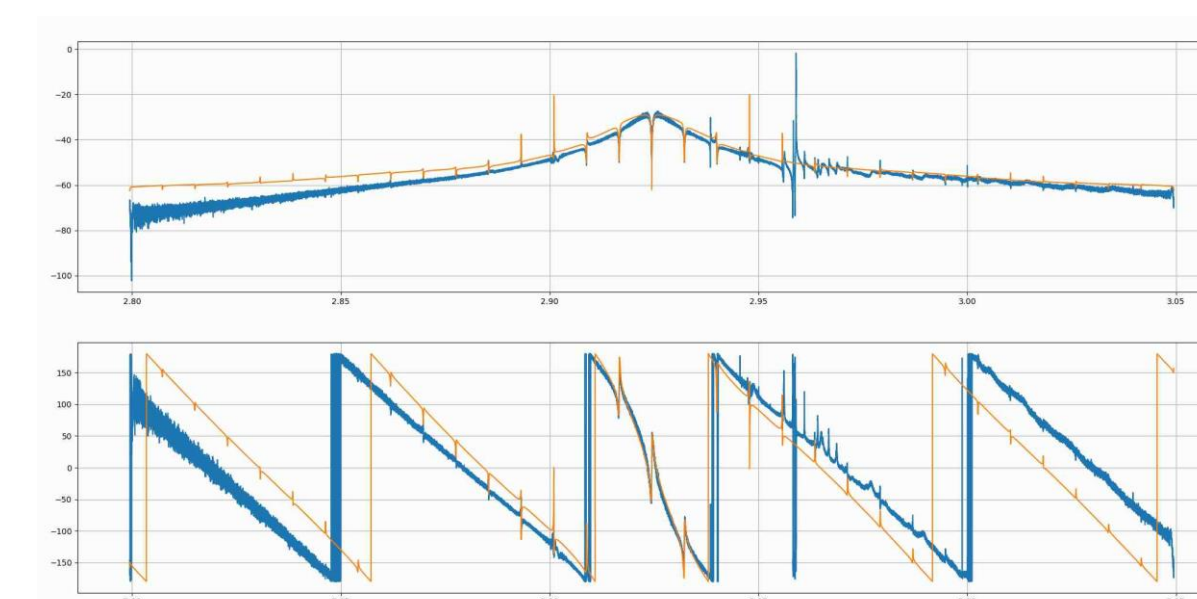


Figure 8: Untuned OTFB measurement. Measurement (blue) vs Model (orange)

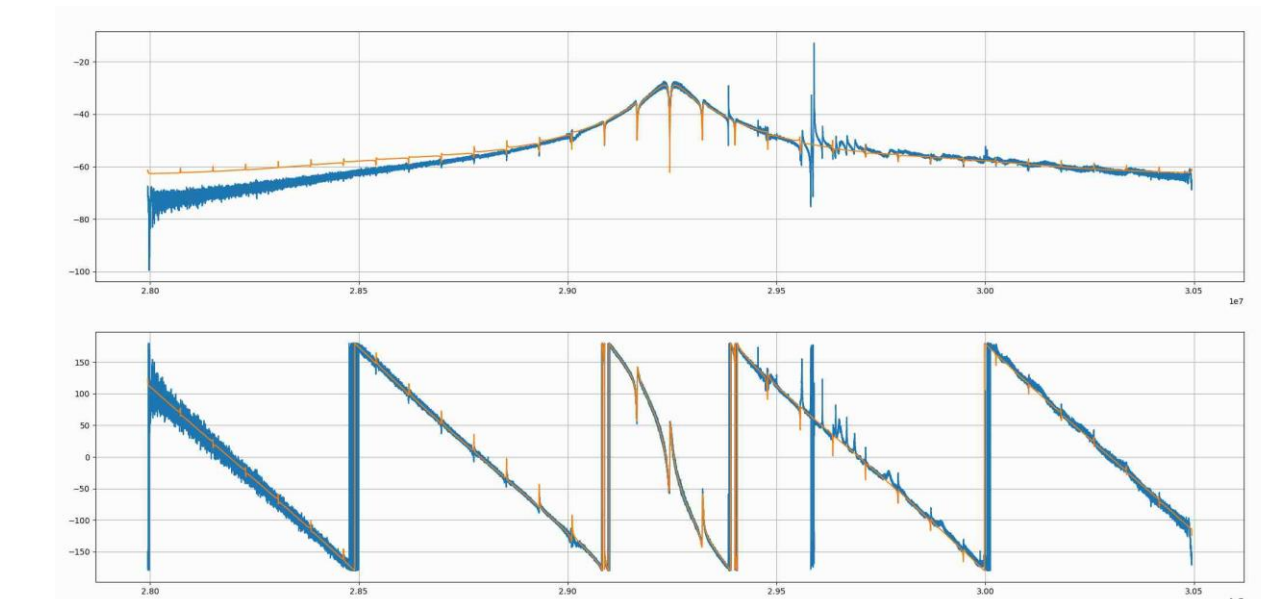


Figure 9: After tuning of OTFB by applying phase equalizer and correct OTFB delay, measurements match signal more closely.

Future Work

The Digital Network Analyzer will be implemented and integrated into the EIC Common Hardware Platform in the future. Additional work includes adding Nyquist plots to determine stability and improving scripts for a better UI.

References

- [1] C. Marques et al., "Status of the NSLS-II LLRF System", proceedings of PCaPAC2016, Campinas, Brazil.
- [2] J. C. Molendijk, "An Extended Base-band Network Analyzer in the Digital LLRF", proceedings of the LLRF11 Workshop, Hamburg, Germany.
- [3] S. Mai et al., "Baseband Digital Network Analyzer Upgrade for LLRF Controllers," 2025, BNL.
- [4] Brüel & Kjær, "Technical Review No. 2, 1984. Dual Channel FFT Analysis (Part I)"
- [5] A. Singh et al., "LLRF Upgrades For Studying Transient Beam-Loading For RHIC 28MHz Accelerator Cavity at Brookhaven National Laboratory (BNL)," to be published at the 2025 LLRF Conference