

The Development of an Ultra-Low Phase Noise Source for Electron-Ion Collider (EIC) Crab Cavities

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Abstract

The Electron-Ion Collider (EIC) is a long-term project to design and construct a facility to collide high energy polarized electron beams with polarized proton and heavy ion beams at center of mass energies from 20 to 140 GeV with luminosity up to $10^{34} \text{ cm}^{-2}\text{s}^{-1}$. This facility will be built on top of the Relativistic Heavy Ion Collider (RHIC), Brookhaven National Laboratory's current operational high energy collider. In order to achieve the high luminosity outlined in the EIC's design, Crab Cavities will be used around Interaction Points to correct for geometric effects due to crossing angles. These cavities have extremely strict RF phase noise requirements that are challenging to achieve ($< -151 \text{ dBc/Hz}$ at a 10 kHz offset from a 197 MHz Carrier). In order to meet these requirements, a low noise 2 GHz clock was designed using a 100 MHz OCXO. The 100 MHz OCXO was then locked to a separate low noise 100 MHz clock using an analog PLL to further reduce low-offset phase noise. This clock was then used with a low noise DAC (AD9164) to generate an RF drive signal at various frequencies of interest.

Clocking Scheme

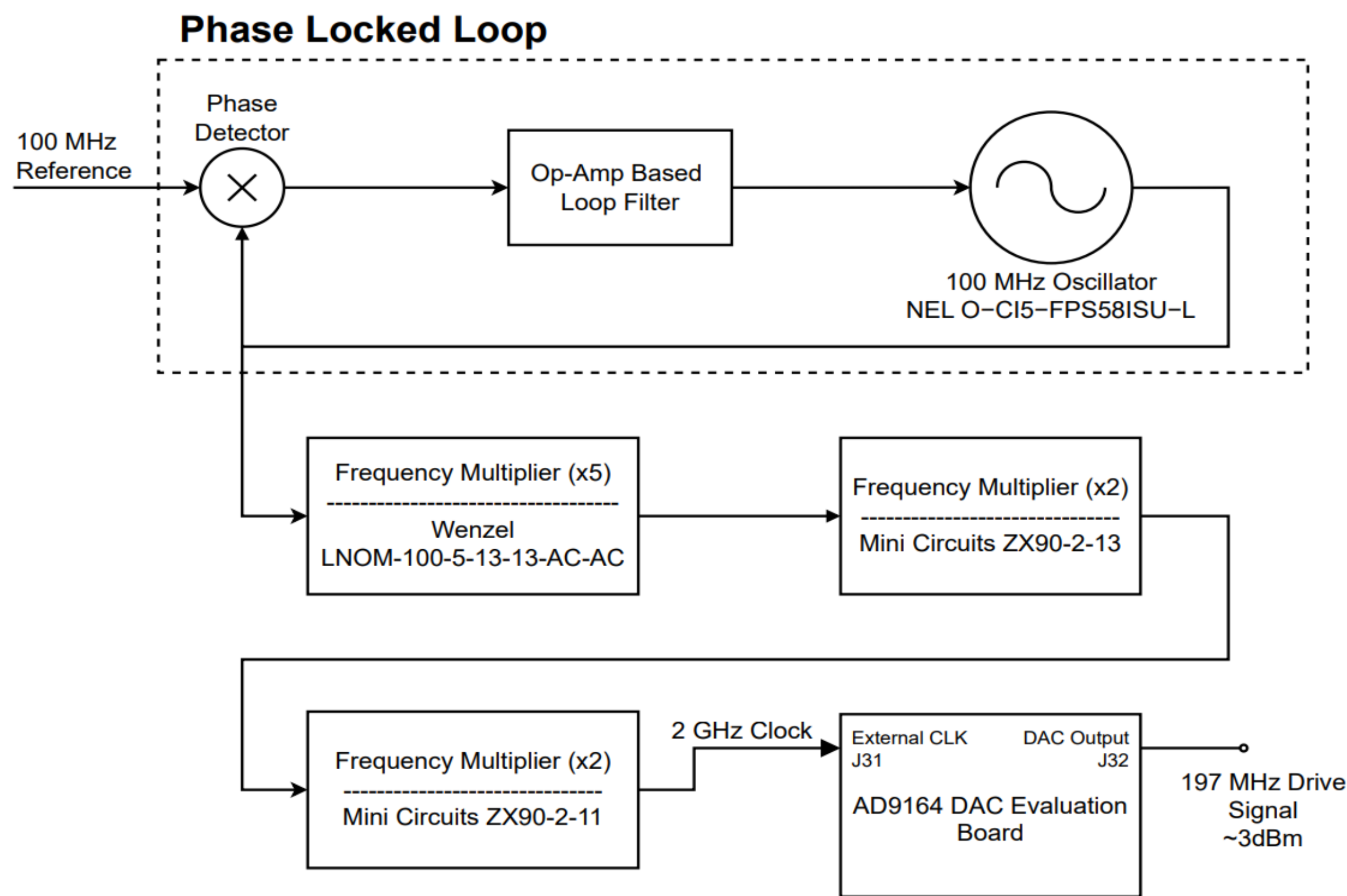


Figure 1 – Developmental EIC Clock Receiver Chassis

To clock the AD9164, a clock with a frequency above 1.5 GHz must be supplied. To keep this clock synchronous with the 100 MHz site-wide clock, an analog PLL including 100 MHz OCXO is used, which subsequently gets multiplied up to 2 GHz. This has an added bonus of reducing the phase noise at low frequency offsets, as the reference performs much better at these offsets.

System Architecture

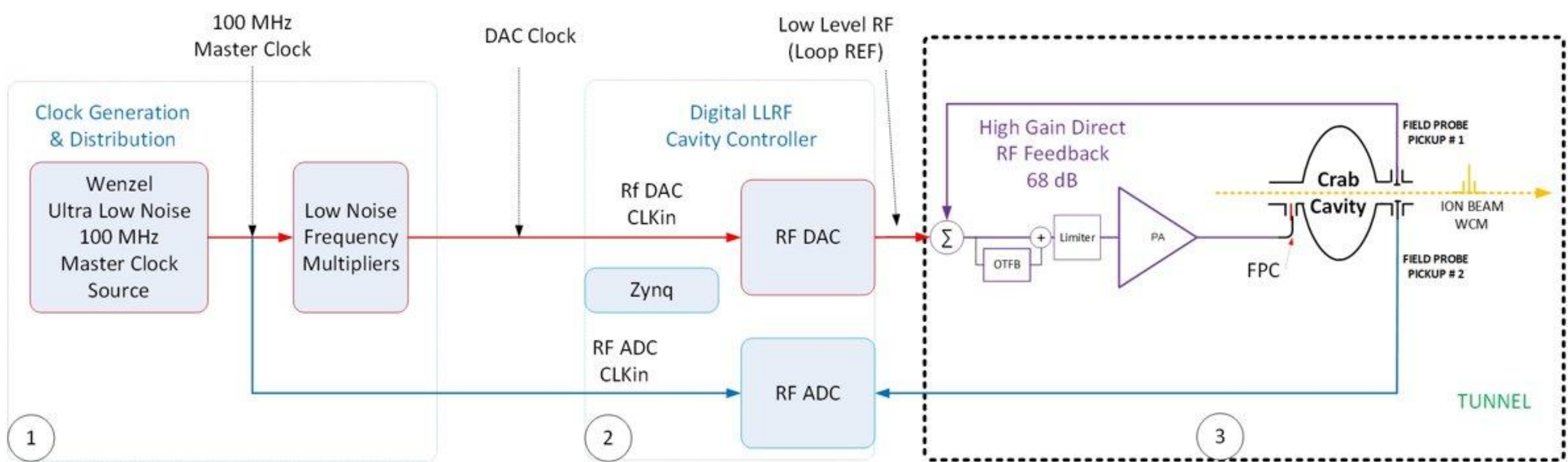


Figure 2 – Proposed Feedback Loops for Controlling EIC Crab Cavities

To control the field in Crab Cavities properly, a high gain fast RF feedback loop, extra control loops in the One-Turn Feedback Loop, and an ultra-low noise Low Level RF Drive (to prevent excessive transverse beam emittance growth)¹ are employed. Crab cavities are included in the design of the EIC to increase luminosity by reducing the geometric effect of the crossing angle.

Results

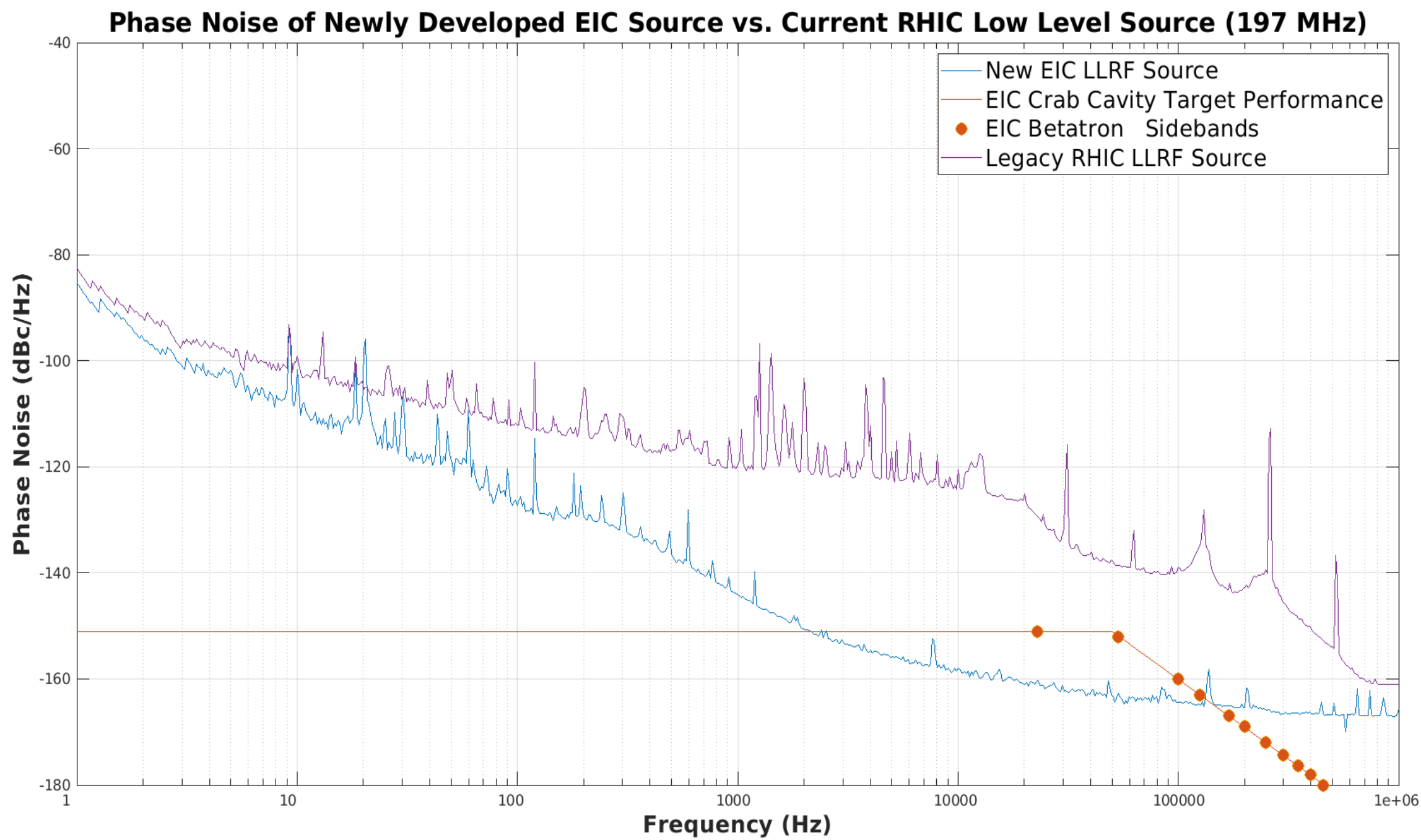


Figure 6 – Phase Noise of RHIC 197 MHz Drive vs. Newly Developed 197 MHz Drive

Compared to the noise seen on the standard low level drive signal for RHIC cavities, this developmental source is quieter or as quiet at all frequency offsets. In the bandwidth of 1 – 10,000 Hz, this new source has 268.892 fs less jitter.

Frequency Source	Integrated Jitter, 1 Hz – 10 kHz BW
RHIC 197 MHz Low Level Source	318.557 fs
Newly Developed 197 MHz Low Level Source	49.665 fs

The frequencies of interest for controlling the field in the crab cavities are shown in orange in Figure 6. These are the expected noise levels needed to limit transverse beam emittance growth to a manageable level. Noise power is critical at the betatron sideband frequencies, where RF noise will have a coherent effect on the beam.¹ The -30 dB/dec slope observed at $\sim 50 \text{ kHz}$ in the estimate is due to the assumption that the Fast-RF Feedback Loop (shown in Figure 2) will have a bandwidth of 50 kHz. Out of band, the filtering effect from the high-Q SRF cavity will effectively reduce the noise seen by the beam. This effect is not seen on the LLRF Drive being measured in Figure 6.

Citations and Future Work

Although preliminary results are promising, additional noise sources stemming from the inclusion of other necessary control loops (ADC noise from OTFB Loop, Amplifier noise from Fast RF Feedback Loop) must be understood to ensure that the level of noise on the cavity remains manageable.

1. Smith, K., Mastoridis, T., Fuller, P., Mahri, P., & Matsumura, Y. (2022). EIC Transverse emittance growth due to crab cavity RF noise: Estimates and mitigation. <https://doi.org/10.2172/1846026>

PLL Design

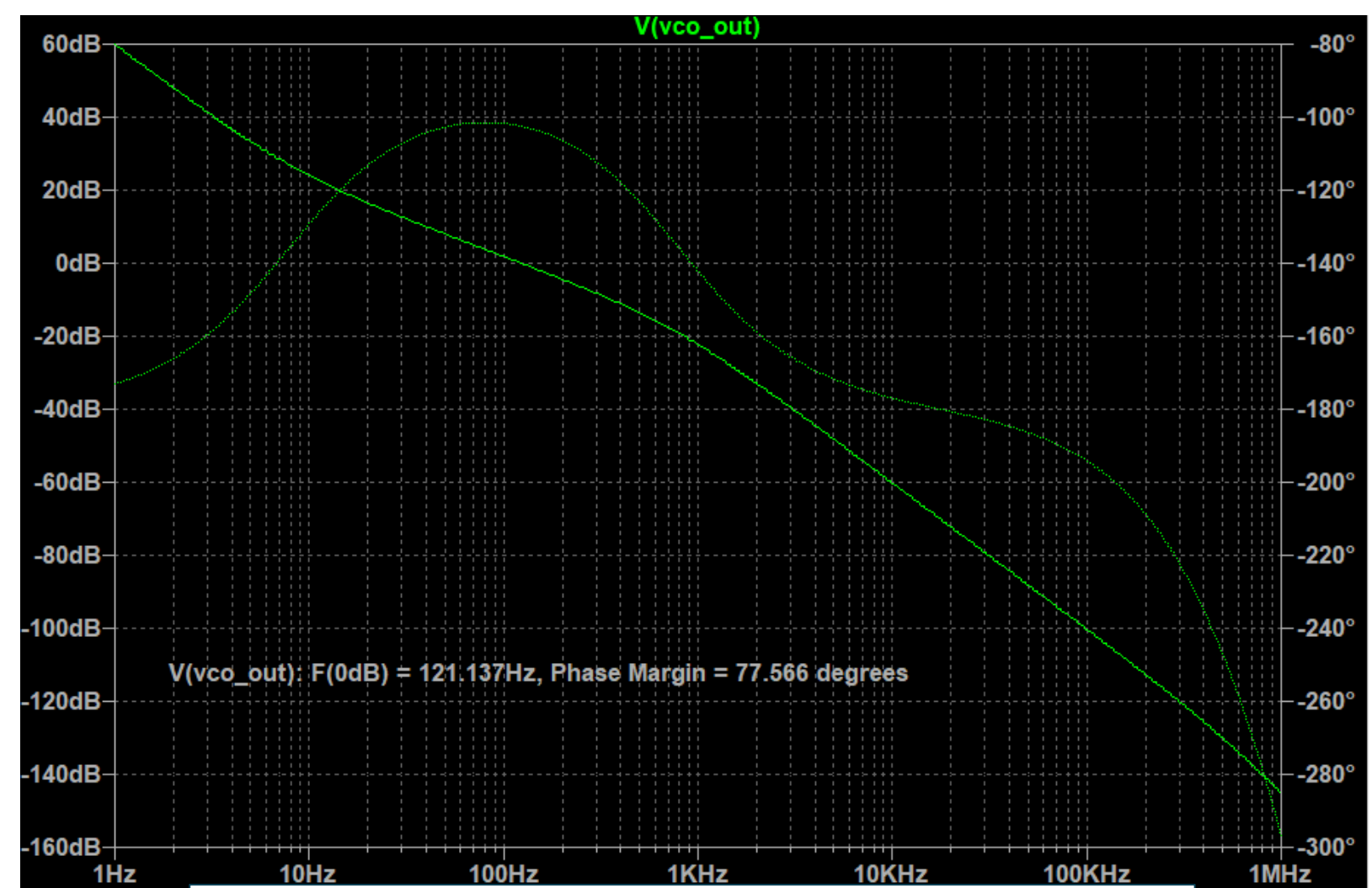


Figure 3 – Open Loop PLL Bode Plot

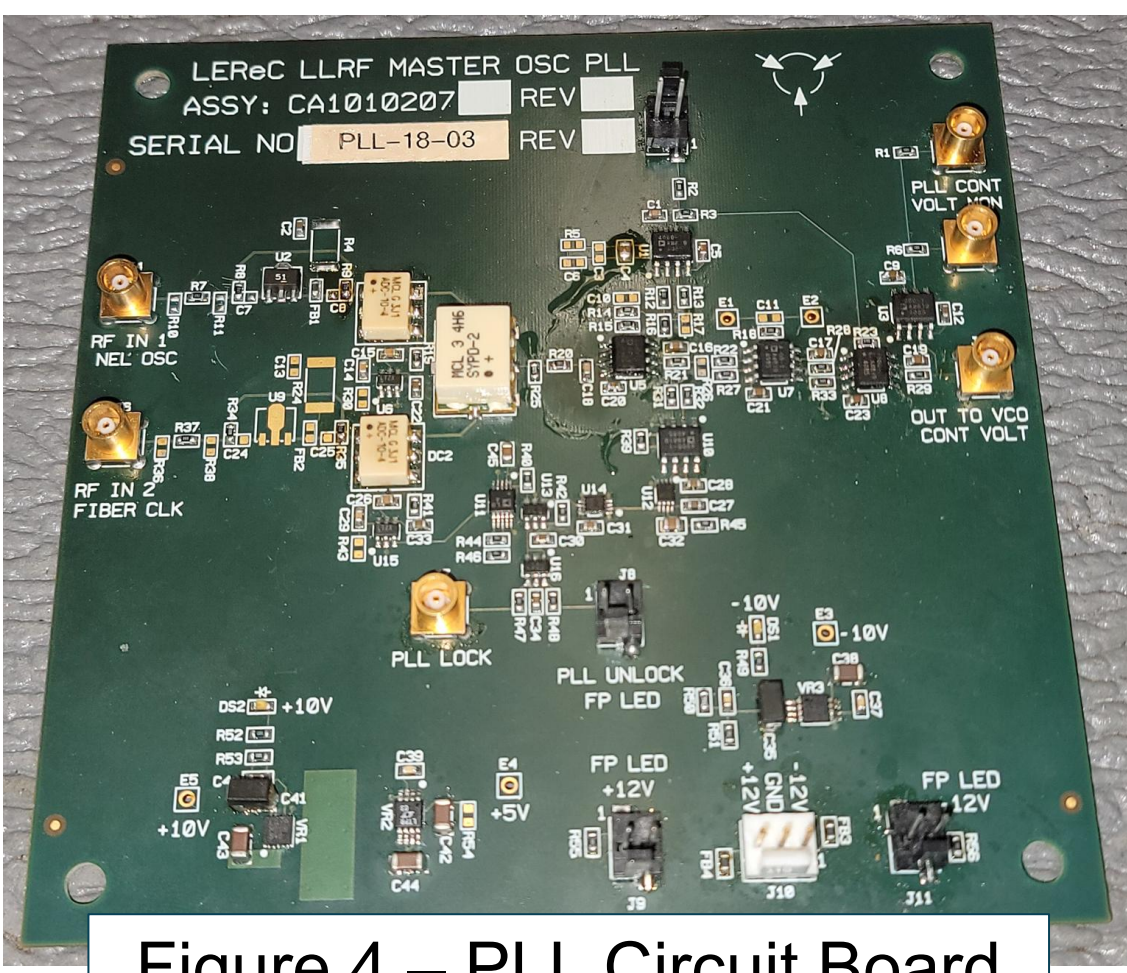


Figure 4 – PLL Circuit Board

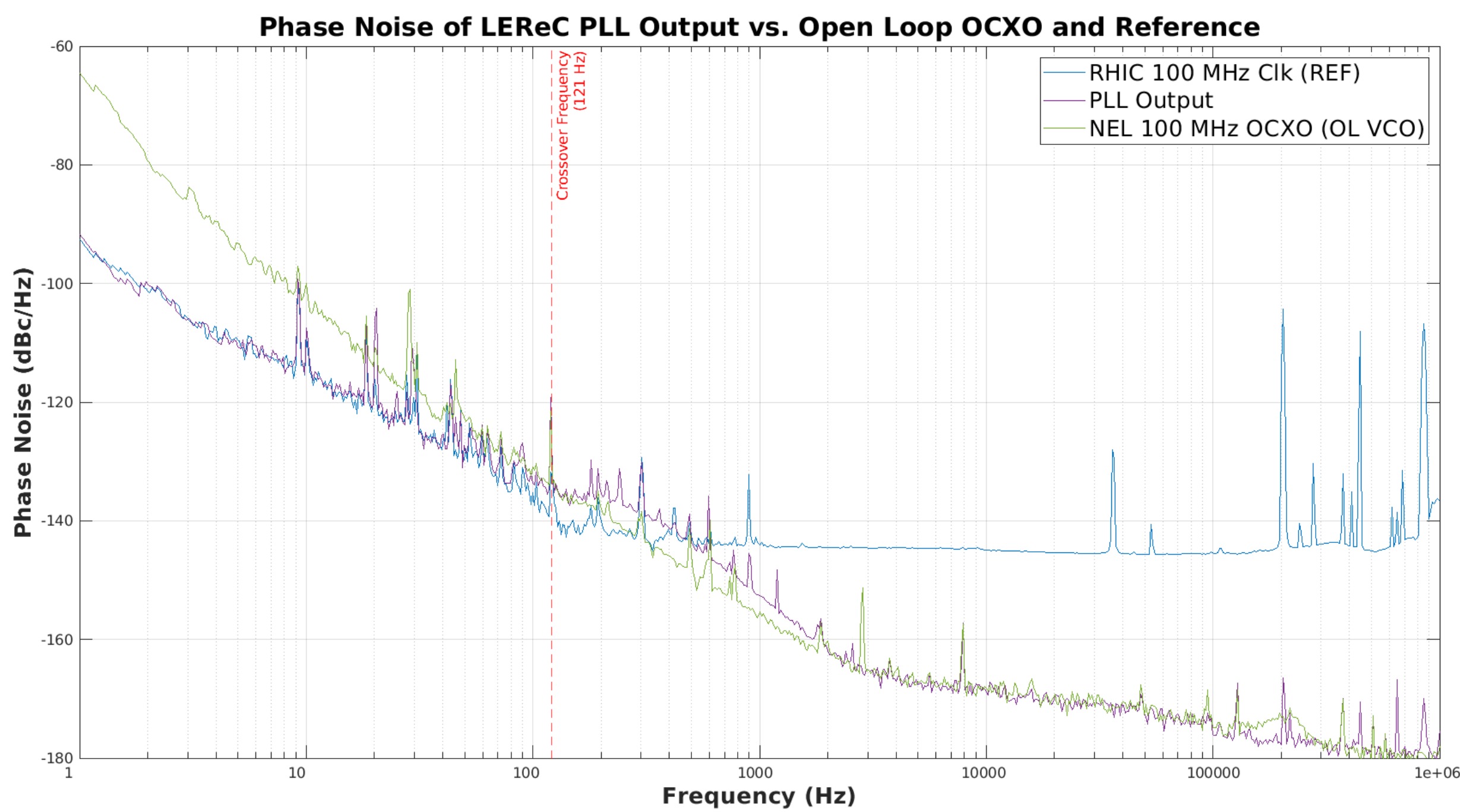


Figure 5 – Noise Improvement Due to PLL Usage

Frequency Source	Integrated Jitter, 1 Hz – 1 MHz BW
RHIC 100 MHz System Clock	2062.87 fs
Closed Loop NEL OCXO, 100 MHz	48.785 fs

To further improve phase noise performance, a PLL was used to lock the NEL oscillator to a low noise 100 MHz reference. This makes up for the oscillator's poor performance at low frequency offsets, where the low noise reference excels.