LEMP LLRF Firmware and Software

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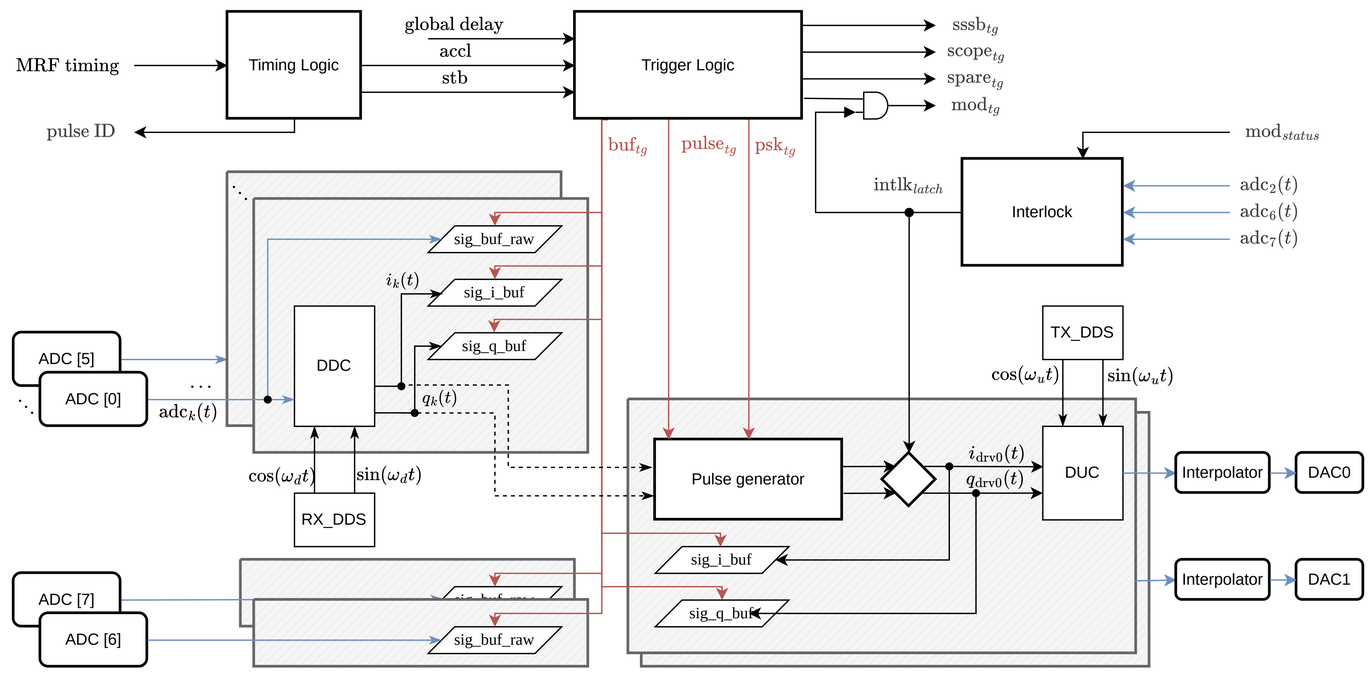
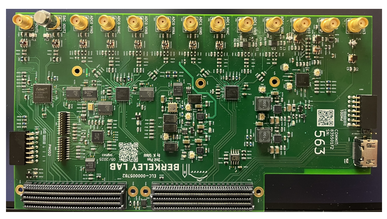
Abstract

The LCLS began operations in 2009, utilizing SLAC's normal-conducting LINAC, which features control equipment dating back to the 1960s and 1980s. The **Linac Electronics Modernization Plan (LEMP)** aims to replace the legacy control equipment with a system based on the open-source Marble carrier board and a modified version of the Zest digitizer board, both of which are used in the LCLS-II HE LLRF system. Adaptation of the LLRF system from the CW SRF LCLS-II to the short RF pulse NC LCLS includes leveraging the knowledge and experience gained from recent LLRF projects at SLAC and efficiently reusing the core functionality of the code base developed at LBNL. Here, we describe the firmware and software infrastructure, highlight key features, and present preliminary prototype results.

LLRF DSP Structure

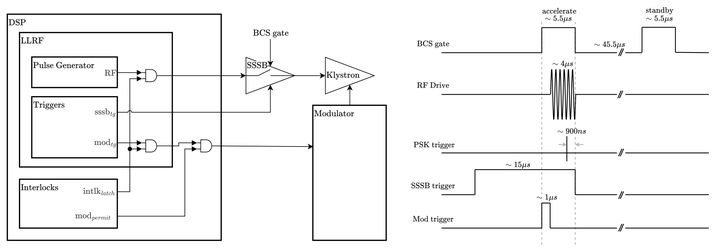


Marble and Zest+



The new LEMP system is built on the open-source **Marble** FPGA carrier [1] and a modified version of the **Zest** digitizer [2] with a custom RF front-end.

System Overview

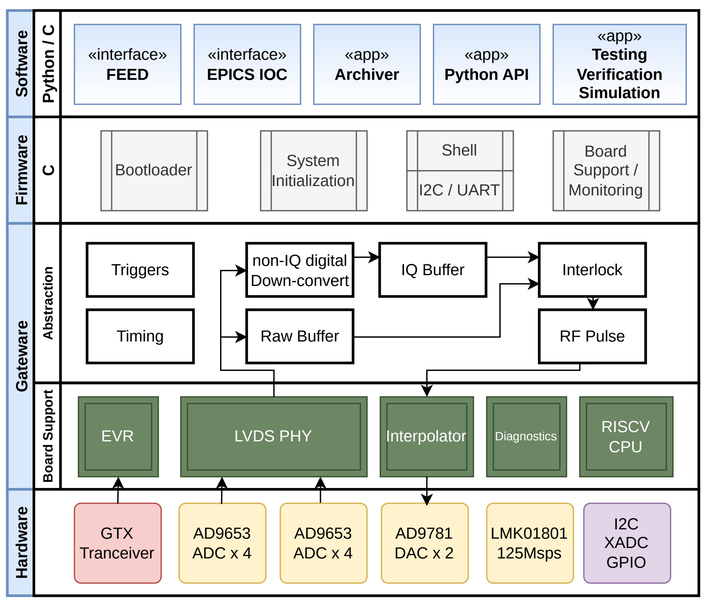


Simplified diagram of connections between the Solid State Sub Booster (SSSB), the 5045 Klystron, the modulator and the LEMP LLRF system (left), and time synchronization of LLRF triggers with the RF pulse and the **accelerate** and **standby** buckets (right).

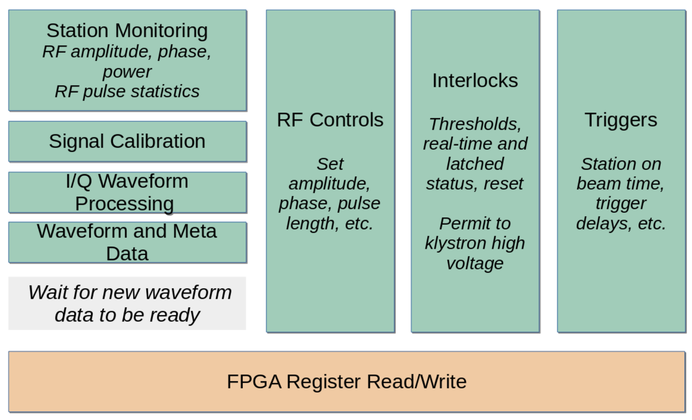
	Generation	Relationship	f [MHz]
RF			2856
MO			2856
ADC_{clk}	LMK01801	$\frac{1}{24}$ MO	119
DAC_{clk}	LMK01801	$\frac{1}{12}$ MO	238
LO_{dwn}	MO - $\frac{MO}{112}$		2830.5
LO_{up}	LO_{dwn} + ADC_{clk}		2949.5
IF_{dwn}	RF - LO_{dwn}	$\frac{3}{14}ADC_{clk}$	25.5
IF_{up}	Zest+	$\frac{11}{28}DAC_{clk}$	93.5

All frequencies are phase-locked to the 2856-MHz MO. Independent up/down-conversion LOs are synthesized using single-sideband modulation derived from the MO, with separate ADC and DAC clock domains to reduce cross-talk. The 2.856-GHz RF is down-converted to 25.5 MHz (LO_{dwn} at 2830.5 MHz) and digitized at 119 MHz. The DAC runs at 238 MHz, generating a 93.5-MHz IF up-converted with a 2949.5-MHz LO_{up}. No distributed LO or VCXO is used.

Firmware and Software Design

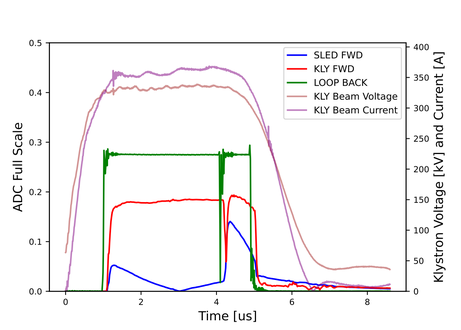


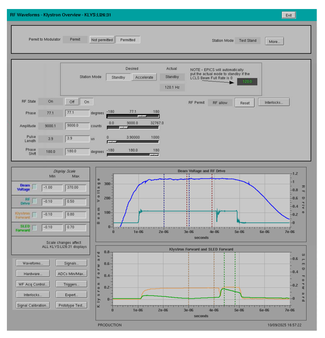
System architecture design utilizing the BSD-licensed open-source LLRF library Bedrock [3]. The board support layer interacts with the hardware to gather ADC data and timing information, and to transmit output to the DAC. The RISC-V CPU PicoRV32 [4] manages boot-time self-initialization and testing, system configuration, and status monitoring. The abstraction layer enables flexible configuration of sampling frequencies, clocks, DSP, and EVR settings. System simulation and verification are available with a virtual cavity model.



An **EPICS IOC** is used to provide high-level monitoring and control of the system. It includes software originally developed for the LCLS-II LLRF system to facilitate communication with the FPGA and for waveform data processing. New functionality is being added to support the pulsed operation of the LCLS stations and for integration into the larger LCLS control system.

Prototype Test





The prototype chassis was deployed at **station 26-3** (sector 26, klystron #3), and its main functionality was verified. According to the standard NC linac operation, the RF pulse was set to 5 μs long and the SLED control 180° phase change occurs after 3 μs of the start of the pulse. These RF parameters are configurable from EPICS displays in order to optimize the RF performance based on local linac considerations. The system was set to trigger at the standby event, but after successful verification, the station was aligned to the accelerate event and the phase set point was optimized to increase the beam energy for a user program that allows a beam-based evaluation of the RF performance. At this time, **the prototype chassis has been in operation at the klystron station 26-3 for hundreds of hours**, though most often in standby, which enables testing of new development.

Summary

A prototype chassis for the LEMP project has been designed, tested and deployed at station 26-3, based on previous LLRF projects. After successful verification of the main functionality, the station was aligned to the accelerate event and the phase set-point was optimized. The system has been in operation for hundreds of hours, mostly in standby mode. Future work includes finalizing the design and building more chassis to upgrade more stations.

References

[1] LBNL. *Marble board*, https://github.com/BerkeleyLab/Marble, 2020-2025.

[2] LBNL. *Zest board*, https://github.com/BerkeleyLab/Zest, 2021.

[3] LBNL. *Bedrock: Open source llrf fpga firmware library*, https : / / github . com / BerkeleyLab / Bedrock, 2019- 2025.

[4] YosysHQ. *PicoRV32 – a size–optimized RISC–V CPU*, https://github.com/YosysHQ/picorv32, 2015.